Infineon Technologies - SAF-XC164LM-16F40F BA Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164lm-16f40f-ba

XC164LM
Revision History: V1.2, 2007-03

Previous Version(s):
V1.1, 2006-08
V1.0, 2005-11

Page	Subjects (major changes since last revision)
6	Design steps of the derivatives differentiated.
47	Power consumption of the derivatives differentiated.
48	Figure 9 adapted.
49	Figure 11 adapted.
56	Packages of the derivatives differentiated.
57	Thermal resistances of the derivatives differentiated.
all	“Preliminary” removed

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Table 2 Pin Definitions and Functions

Sym-bol	Pin Num.	Input Outp.	Function
$\overline{\text{RSTIN}}$	63	I	Reset Input with Schmitt-Trigger characteristics. A low-level at this pin while the oscillator is running resets the XC164LM. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle. External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
$\overline{\text{NMI}}$	64	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the XC164LM into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
Port 9	43-48	IO	Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions: CC16IO: (CAPCOM2) CC16 Capture Inp./Compare Outp.,
P9.0	43	I/O I	EX5IN: (Fast External Interrupt 5) Input (alternate pin A) CC17IO: (CAPCOM2) CC17 Capture Inp./Compare Outp.,
P9.1	44	I/O	CC18IO: (CAPCOM2) CC18 Capture Inp./Compare Outp.,
P9.2	45	I/O I	EX4IN: (Fast External Interrupt 4) Input (alternate pin A) CC19IO: (CAPCOM2) CC19 Capture Inp./Compare Outp.,
P9.3	46	I/O	CC20IO: (CAPCOM2) CC20 Capture Inp./Compare Outp.
P9.4	47	I/O	CC21IO: (CAPCOM2) CC21 Capture Inp./Compare Outp.
P9.5	48	I/O	*Note: At the end of an external reset P9.4 and P9.5 also may input startup configuration values*

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
Port 5	9-18, 21-24	I	Port 5 is a 14-bit input-only port. Some pins of Port 5 also serve as timer inputs:
P5.10	15	I	T6EUD: GPT2 Timer T6 Ext. Up/Down Control Input
P5.11	16	I	T5EUD: GPT2 Timer T5 Ext. Up/Down Control Input
P5.12	21	I	T6IN: GPT2 Timer T6 Count/Gate Input
P5.13	22	I	T5IN: GPT2 Timer T5 Count/Gate Input
P5.14	23	I	T4EUD: GPT1 Timer T4 Ext. Up/Down Control Input
P5.15	24	I	T2EUD: GPT1 Timer T2 Ext. Up/Down Control Input
$\overline{\text{TRST}}$	62	I	Test-System Reset Input. For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{RSTIN}}$ enables the hardware configuration and activates the XC164LM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.

3.1 Memory Subsystem and Organization

The memory space of the XC164LM is configured in a von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed byte wise or word wise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory or code or data is written to the PSRAM. The system bus allows concurrent two-way communication for maximum transfer performance.

32/64/128 Kbytes of on-chip Flash memory[1] store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors and up to three 32-Kbyte sectors. Each sector can be separately write protected[2], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
Programming typically takes 2 ms per 128-byte block (5 ms max.), erasing a sector typically takes 200 ms (500 ms max.).

2 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

0/2/4 Kbytes[1] of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses. DSRAM is not available in the XC164LM-4F derivatives.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks. A register bank

1) Depends on the respective derivative. See **Table 1 "XC164LM Derivative Synopsis" on Page 6**.

2) Each two 8-Kbyte sectors are combined for write-protection purposes.

Table 4 XC164LM Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
Unassigned node	–	xx'0080$_H$	20$_H$ / 32$_D$
Unassigned node	–	xx'0084$_H$	21$_H$ / 33$_D$
Unassigned node	–	xx'00A0$_H$	28$_H$ / 40$_D$
Unassigned node	–	xx'00A4$_H$	29$_H$ / 41$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0100$_H$	40$_H$ / 64$_D$
Unassigned node	–	xx'0104$_H$	41$_H$ / 65$_D$
Unassigned node	–	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	–	xx'0134$_H$	4D$_H$ / 77$_D$
Unassigned node	–	xx'0138$_H$	4E$_H$ / 78$_D$
Unassigned node	–	xx'013C$_H$	4F$_H$ / 79$_D$
Unassigned node	–	xx'0140$_H$	50$_H$ / 80$_D$
Unassigned node	–	xx'0150$_H$	54$_H$ / 84$_D$
Unassigned node	–	xx'0154$_H$	55$_H$ / 85$_D$
Unassigned node	–	xx'0158$_H$	56$_H$ / 86$_D$
Unassigned node	–	xx'015C$_H$	57$_H$ / 87$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$
Unassigned node	–	xx'0164$_H$	59$_H$ / 89$_D$
Unassigned node	–	xx'0168$_H$	5A$_H$ / 90$_D$
Unassigned node	–	xx'016C$_H$	5B$_H$ / 91$_D$
Unassigned node	–	xx'0170$_H$	5C$_H$ / 92$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

The XC164LM also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions:	–				
• Hardware Reset		RESET	xx’0000$_H$	00$_H$	III
• Software Reset		RESET	xx’0000$_H$	00$_H$	III
• W-dog Timer Overflow		RESET	xx’0000$_H$	00$_H$	III
Class A Hardware Traps:					
• Non-Maskable Interrupt	NMI	NMITRAP	xx’0008$_H$	02$_H$	II
• Stack Overflow	STKOF	STOTRAP	xx’0010$_H$	04$_H$	II
• Stack Underflow	STKUF	STUTRAP	xx’0018$_H$	06$_H$	II
• Software Break	SOFTBRK	SBRKTRAP	xx’0020$_H$	08$_H$	II
Class B Hardware Traps:					
• Undefined Opcode	UNDOPC	BTRAP	xx’0028$_H$	0A$_H$	I
• PMI Access Error	PACER	BTRAP	xx’0028$_H$	0A$_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx’0028$_H$	0A$_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx’0028$_H$	0A$_H$	I
Reserved	–	–	[2C$_H$ - 3C$_H$]	[0B$_H$ - 0F$_H$]	–
Software Traps • TRAP Instruction	–	–	Any [xx’0000$_H$ - xx’01FC$_H$] in steps of 4$_H$	Any [00$_H$ - 7F$_H$]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

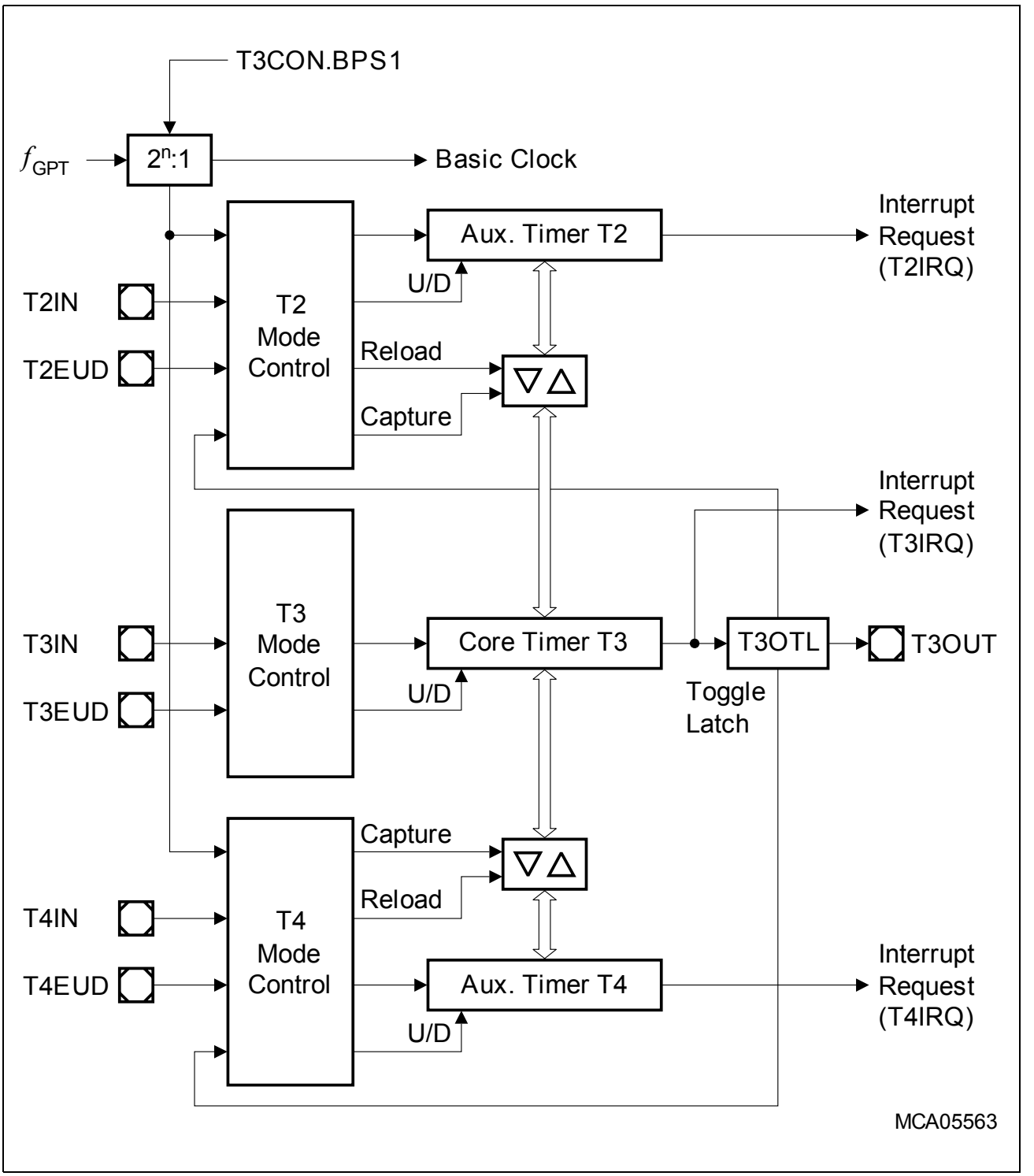

Figure 6 Block Diagram of GPT1

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The

count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC164LM to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

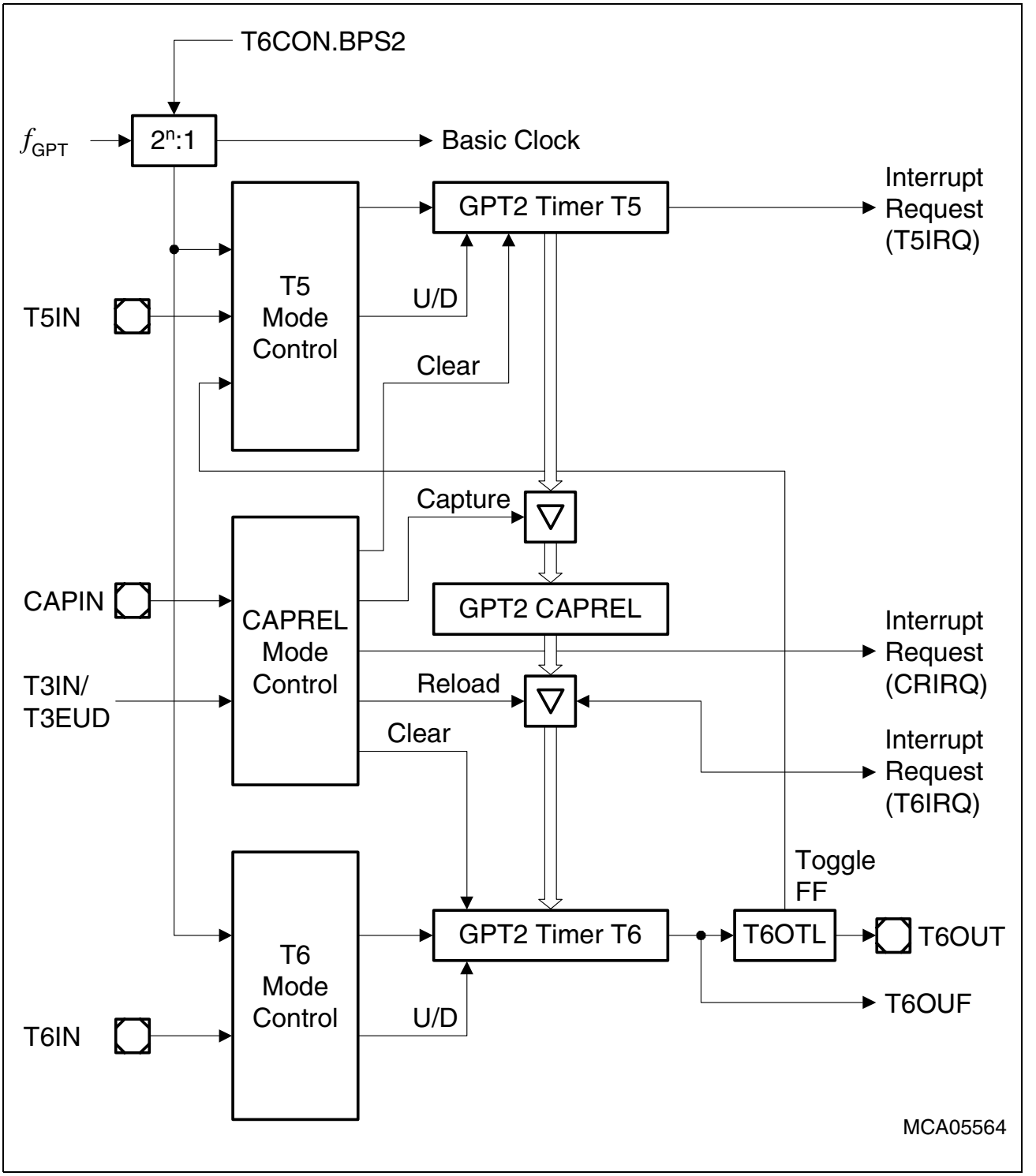

Figure 7 Block Diagram of GPT2

3.7 Real Time Clock

The Real Time Clock (RTC) module of the XC164LM is directly clocked via a separate clock driver with the prescaled on-chip main oscillator frequency ($f_{RTC} = f_{OSCm}/32$). It is therefore independent from the selected clock generation mode of the XC164LM.

The RTC basically consists of a chain of divider blocks:

- A selectable 8:1 divider (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL), made of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

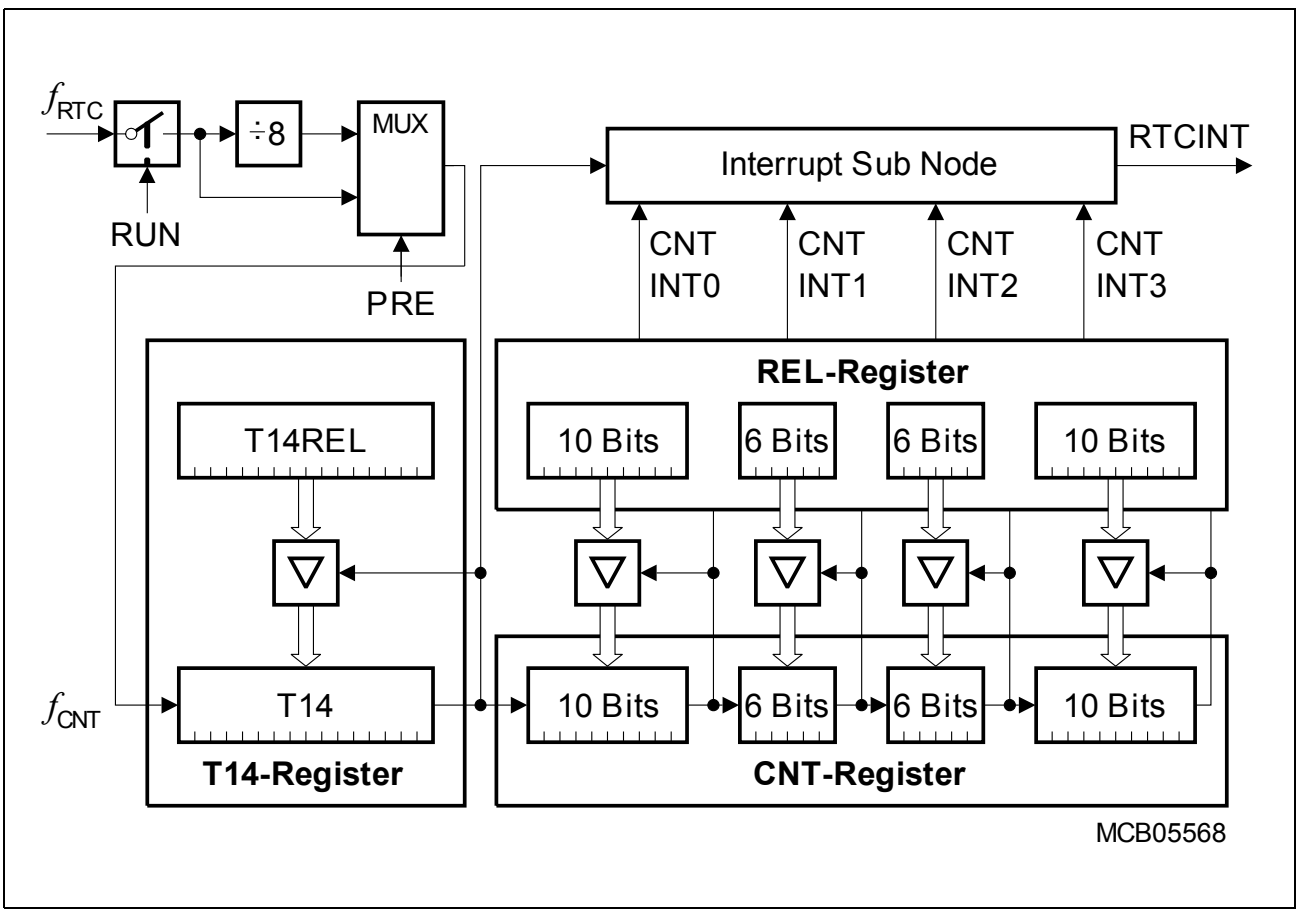

Figure 8 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

3.12 Parallel Ports

The XC164LM provides up to 47 I/O lines which are organized into three input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

Table 7 Summary of the XC164LM's Parallel Ports

Port	Control	Alternate Functions
PORT1	Pad drivers	Capture inputs or compare outputs, Serial interface lines
Port 3	Pad drivers, Open drain, Input threshold	Timer control signals, serial interface lines, System clock output CLKOUT (or FOUT)
Port 5	–	Timer control signals
Port 9	Pad drivers, Open drain, Input threshold	Capture inputs or compare outputs

3.13 Power Management

The XC164LM provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the XC164LM into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC164LM's CPU clock frequency which drastically reduces the consumed power.
  External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3). Each peripheral can separately be disabled/enabled.

The on-chip RTC supports intermittent operation of the XC164LM by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

3.14 Instruction Set Summary

Table 8 lists the instructions of the XC164LM in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164LM. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}$ 1)
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode 2)3)
Supply Voltage Difference	ΔV_{DD}	-0.5	–	V	$V_{DDP} - V_{DDI}$ 4)
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin 5)6)
Overload current coupling factor for digital I/O pins 7)	K_{OVD}	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma\lvert I_{OV}\rvert$	–	50	mA	6)
External Load Capacitance	C_L	–	50	pF	Pin drivers in **default** mode 8)
Ambient temperature	T_A	0	70	°C	SAB-XC164…
		-40	85	°C	SAF-XC164…
		-40	125	°C	SAK-XC164…

1) f_{CPUmax} = 40 MHz for devices marked … 40F, f_{CPUmax} = 20 MHz for devices marked … 20F.

2) External circuitry must guarantee low-level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of V_{DDP} = 4.75 V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP}$ + 0.5 V ($I_{OV} > 0$) or $V_{OV} < V_{SS}$ - 0.5 V ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.
Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1.

6) Not subject to production test - verified by design/characterization.

Table 13 Power Consumption XC164LM (Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DDI}	–	15 + 2.6 × f_{CPU}	mA	f_{CPU} in [MHz][1)2)], -16F derivatives
		–	10 + 2.6 × f_{CPU}	mA	f_{CPU} in [MHz][1)2)], -4F/8F derivatives
Pad supply current	I_{DDP}	–	5	mA	[3)]
Idle mode supply current with all peripherals active	I_{IDX}	–	15 + 1.2 × f_{CPU}	mA	f_{CPU} in [MHz][2)], -16F derivatives
		–	10 + 1.2 × f_{CPU}	mA	f_{CPU} in [MHz][2)], -4F/8F derivatives
Sleep and Power down mode supply current caused by leakage[4)]	I_{PDL}[5)]	–	84,000 × $e^{-\alpha}$	mA	V_{DDI} = V_{DDImax}[6)] T_J in [°C] α = 4380 / (273 + T_J) -16F derivatives
		–	128,000 × $e^{-\alpha}$	mA	α = 4670 / (273 + T_J) -4F/8F derivatives
Sleep and Power down mode supply current caused by leakage and the RTC running, clocked by the main oscillator[4)]	I_{PDM}[7)]	–	0.6 + 0.02 × f_{OSC} + I_{PDL}	mA	V_{DDI} = V_{DDImax} f_{OSC} in [MHz]

1) During Flash programming or erase operations the supply current is increased by max. 5 mA.

2) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 9**. These parameters are tested at V_{DDImax} and maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

3) The pad supply voltage pins (V_{DDP}) mainly provides the current consumed by the pin output drivers. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the V_{DDP} supply.

4) The total supply current in Sleep and Power down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator.

5) This parameter is determined mainly by the transistor leakage currents. This current heavily depends on the junction temperature (see **Figure 11**). The junction temperature T_J is the same as the ambient temperature T_A if no current flows through the port output drivers. Otherwise, the resulting temperature difference must be taken into account.

6) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq$ 25 °C.

7) This parameter is determined mainly by the current consumed by the oscillator switched to low gain mode (see **Figure 10**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The given values refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

4.3 AC Parameters

These parameters describe the dynamic behavior of the XC164LM.

4.3.1 Definition of Internal Timing

The internal operation of the XC164LM is controlled by the internal master clock f_{MC}.

The master clock signal f_{MC} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{MC}. This influence must be regarded when calculating the timings for the XC164LM.

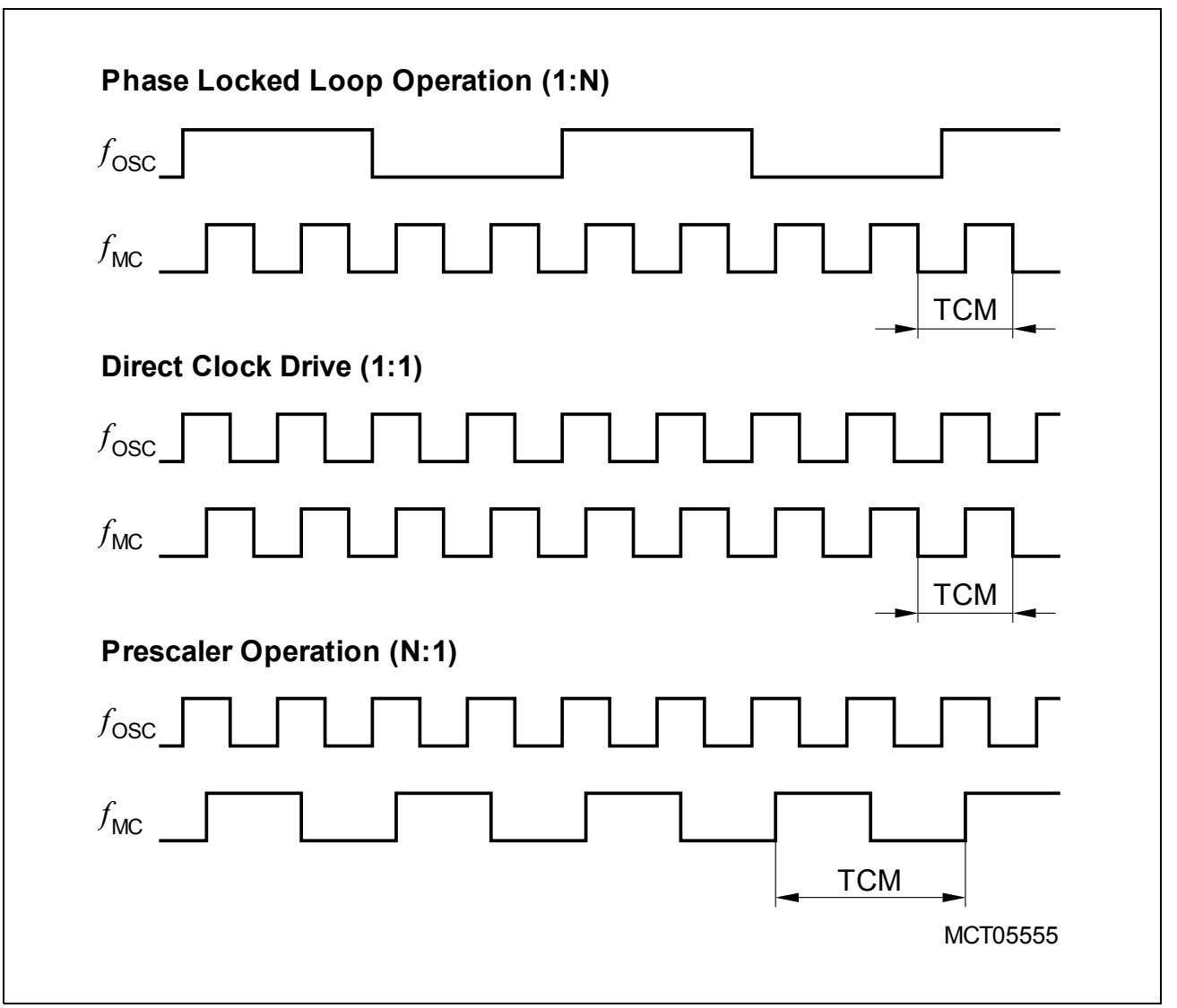

Figure 12 Generation Mechanisms for the Master Clock

*Note: The example for PLL operation shown in **Figure 12** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

4.3.2 On-chip Flash Operation

The XC164LM's Flash module delivers data within a fixed access time (see **Table 15**).

Accesses to the Flash module are controlled by the PMI and take 1+WS clock cycles, where WS is the number of Flash access waitstates selected via bitfield WSFLASH in register IMBCTRL. The resulting duration of the access phase must cover the access time t_{ACC} of the Flash array. The required Flash waitstates depend on the actual system frequency.

The Flash access waitstates only affect non-sequential accesses. Due to prefetching mechanisms, the performance for sequential accesses (depending on the software structure) is only partially influenced by waitstates.
In typical applications, eliminating one waitstate increases the average performance by 5% … 15%.

Table 15 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
Flash module access time	t_{ACC}	CC	–	–	50[1)]	ns
Programming time per 128-byte block	t_{PR}	CC	–	2[2)]	5	ms
Erase time per sector	t_{ER}	CC	–	200[2)]	500	ms

1) The actual access time is influenced by the system frequency, see **Table 16**.

2) Programming and erase time depends on the system frequency. Typical values are valid for 40 MHz.

Example: For an operating frequency of 40 MHz (clock cycle = 25 ns), the Flash accesses must be executed with 1 waitstate: ((1+1) × 25 ns) ≥ 50 ns.

Table 16 indicates the interrelation of waitstates and system frequency.

Table 16 Flash Access Waitstates

Required Waitstates	Frequency Range
0 WS (WSFLASH = 00_B)	$f_{CPU} \leq 20$ MHz
1 WS (WSFLASH = 01_B)	$f_{CPU} \leq 40$ MHz

Note: The maximum achievable system frequency is limited by the properties of the respective derivative, i.e. 40 MHz (or 20 MHz for XC164LM-xF20F devices).

4.3.3 External Clock Drive XTAL1

These parameters define the external clock supply for the XC164LM.

Table 17 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Oscillator period	t_{OSC}	SR	25	250[1]	ns
High time[2]	t_1	SR	6	–	ns
Low time[2]	t_2	SR	6	–	ns
Rise time[2]	t_3	SR	–	8	ns
Fall time[2]	t_4	SR	–	8	ns

1) The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

2) The clock input signal must reach the defined levels V_{ILC} and V_{IHC}.

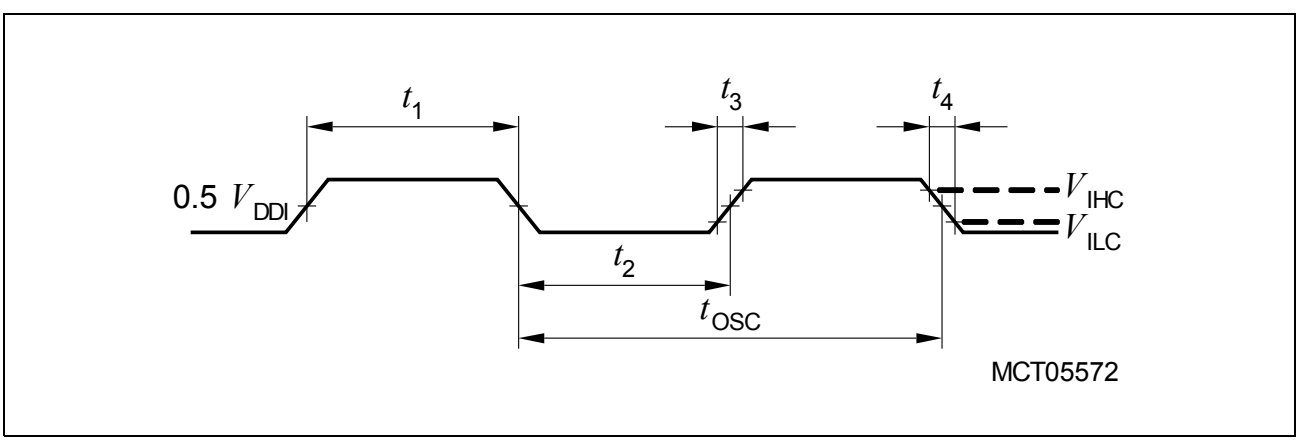

Figure 14 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).

5.2 Flash Memory Parameters

The data retention time of the XC164LM's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 19 Flash Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Data retention time	t_{RET}	15	–	years	10^3 erase/program cycles
Flash Erase Endurance	N_{ER}	20×10^3	–	cycles	Data retention time 5 years