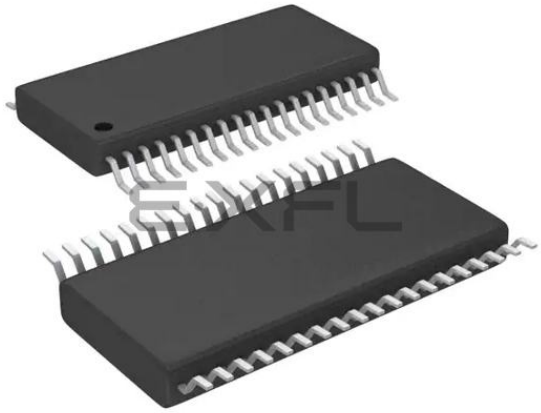
# Infineon Technologies - XMC1200T038F0200AAXUMA1 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 200KB (200K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 38-TFSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-38-9 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1200t038f0200aaxuma1 |

**XMC1200 Data Sheet**

**Revision History: V1.4 2014-05**

| Previous Version: V1.3 | |
|---|---|
| Page | Subjects |
| **Page 11** | ADC channels of Table 2 is updated. Table 3 is added. |
| **Page 12** | Description for Chip Identification Number of Section 1.4 is updated. |
| **Page 10** | A new variant XMC1200-T038 is included in Table 1, Table 2 and Table 4. |
| **Page 20** | The pad type is corrected for P1.6 in Table 6. |
| **Page 32** | The $t_{C12}$ , $f_{C12}$, $t_{C10}$, $f_{C10}$, $t_{C8}$ and $f_{C8}$ parameters are updated in Table 12. |
| **Page 35** | Figure 9 is added. |
| **Page 38** | The $t_{SR}$ and $t_{TSAL}$ parameters are updated in Table 15. |
| **Page 41** | Parameter name for $t_{PSER}$ is updated. The $N_{WSFLASH}$ parameter and test condition for $t_{RET}$ are added to Table 18. |
| **Page 44** | The min value for $V_{DDPBO}$ parameter is added to Table 20. Footnote 1 is updated. |
| **Page 46** | The $\Delta f_{LTT}$ parameter is added to Table 21. |
| **Page 47** | Figure 15 is added. |

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# About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1200 series devices.

The document describes the characteristics of a superset of the XMC1200 series devices. For simplicity, the various device types are referred to by the collective term XMC1200 throughout this document.

### XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

***Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.***

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

- Push/pull or open drain output mode
- Configurable pad hysteresis

**On-Chip Debug Support**

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

## 1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1200 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1200 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1200** is used for all derivatives throughout this document.

## 1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

**Table 1 Synopsis of** XMC1200 **Device Types**

| Derivative | Package | Flash Kbytes | SRAM Kbytes |
|---|---|---|---|
| XMC1201-T038F0016 | PG-TSSOP-38-9 | 16 | 16 |
| XMC1201-T038F0032 | PG-TSSOP-38-9 | 32 | 16 |
| XMC1201-T038F0064 | PG-TSSOP-38-9 | 64 | 16 |
| XMC1201-T038F0128 | PG-TSSOP-38-9 | 128 | 16 |
| XMC1201-T038F0200 | PG-TSSOP-38-9 | 200 | 16 |

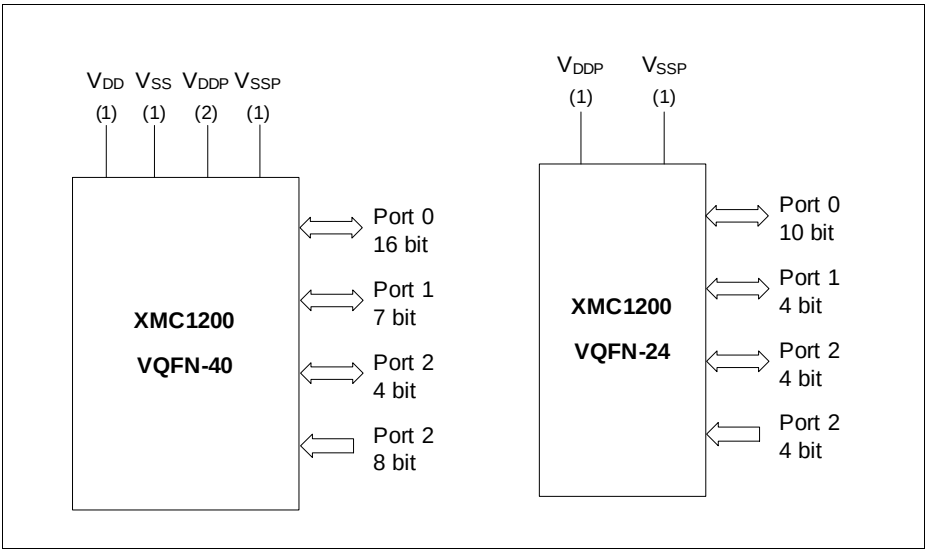


**Figure 3 XMC1200 Logic Symbol for VQFN-24 and VQFN-40**

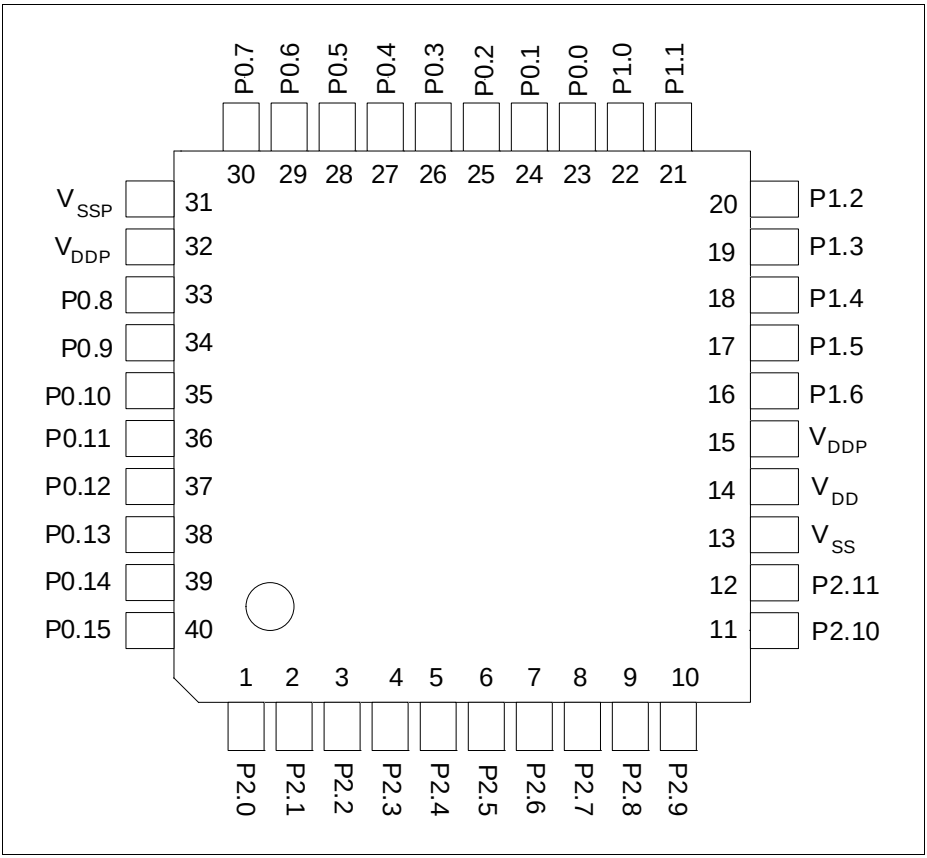


**Figure 8 XMC1200 PG-VQFN-40 Pin Configuration** (top view)

### 2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

**Table 7 Port I/O Function Description**

| Function | Outputs | | | Inputs | | |
|---|---|---|---|---|---|---|
| | ALT1 | ALTn | HWO0 | HWI0 | Input | Input |
| P0.0 | | MODA.OUT | MODB.OUT | MODB.INA | MODC.INA | |
| Pn.y | MODA.OUT | | | | MODA.INA | MODC.INB |

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

**Table 11 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Maximum current into $V_{DDP}$ (TSSOP28/16, VQFN24) | $I_{MVDD1}$ | SR | – | 130 | mA | 3) |
| Maximum current into $V_{DDP}$ (TSSOP38, VQFN40) | $I_{MVDD2}$ | SR | – | 260 | mA | 3) |
| Maximum current out of $V_{SS}$ (TSSOP28/16, VQFN24) | $I_{MVSS1}$ | SR | – | 130 | mA | 3) |
| Maximum current out of $V_{SS}$ (TSSOP38, VQFN40) | $I_{MVSS2}$ | SR | – | 260 | mA | 3) |

1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin.

3) Not subject to production test, verified by design/characterization.

4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when $V_{DDP}$ is powered off.

**Table 12 ADC Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum sample rate in 8-bit mode [3] | $f_{C8}$ CC | – | – | $f_{ADC}$ / 38.5 | – | 1 sample pending |
| | | – | – | $f_{ADC}$ / 54.5 | – | 2 samples pending |
| DNL error | $EA_{DNL}$ CC | – | ±2.0 | – | LSB 12 | |
| INL error | $EA_{INL}$ CC | – | ±4.0 | – | LSB 12 | |
| Gain error with external reference | $EA_{GAIN}$ CC | – | ±0.5 | – | % | SHSCFG.AREF = $00_B$ (calibrated) |
| Gain error with internal reference | $EA_{GAIN}$ CC | – | ±3.6 | – | % | SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C |
| | | – | ±2.0 | – | % | SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C |
| Offset error | $EA_{OFF}$ CC | – | ±6.0 | – | LSB 12 | Calibrated |

1) Not subject to production test, verified by design/characterization.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

### 3.2.4 Analog Comparator Characteristics

Table 14 below shows the Analog Comparator characteristics.

**Table 14 Analog Comparator Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Notes/ Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input Voltage | $V_{CMP}$ | SR | -0.05 | – | $V_{DDP}$ + 0.05 | V | |
| Input Offset | $V_{CMPOFF}$ | CC | – | +/-3 | – | mV | High power mode $\Delta V_{CMP}$ < 200 mV |
| | | | – | +/-20 | – | mV | Low power mode[2] $\Delta V_{CMP}$ < 200 mV |
| Propagation Delay[1][2] | $t_{PDELAY}$ | CC | – | 25 | – | ns | High power mode, $\Delta V_{CMP}$ = 100 mV |
| | | | – | 80 | – | ns | High power mode, $\Delta V_{CMP}$ = 25 mV |
| | | | – | 250 | – | ns | Low power mode, $\Delta V_{CMP}$ = 100 mV |
| | | | – | 700 | – | ns | Low power mode, $\Delta V_{CMP}$ = 25 mV |
| Current Consumption[2] | $I_{ACMP}$ | CC | – | 100 | – | µA | First active ACMP in high power mode, $\Delta V_{CMP}$ > 30 mV |
| | | | – | 66 | – | µA | Each additional ACMP in high power mode, $\Delta V_{CMP}$ > 30 mV |
| | | | – | 10 | – | µA | First active ACMP in low power mode |
| | | | – | 6 | – | µA | Each additional ACMP in low power mode |
| Input Hysteresis[2] | $V_{HYS}$ | CC | – | 15 | – | mV | |
| Filter Delay[1][2] | $t_{FDELAY}$ | CC | – | 5 | – | ns | |

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

2) Not subject to production test, verified by design.

### 3.2.7 Flash Memory Parameters

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 18 Flash Memory Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Erase Time per page | $t_{ERASE}$ CC | 6.8 | 7.1 | 7.6 | ms | |
| Program time per block | $t_{PSER}$ CC | 102 | 152 | 204 | µs | |
| Wake-Up time | $t_{WU}$ CC | – | 32.2 | – | µs | |
| Read time per word | $t_a$ CC | – | 50 | – | ns | |
| Data Retention Time | $t_{RET}$ CC | 10 | – | – | years | Max. 100 erase / program cycles |
| Flash Wait States [1] | $N_{WSFLASH}$ CC | 0 | 0.5 | – | | $f_{MCLK}$ = 8 MHz |
| | | 0 | 1.4 | – | | $f_{MCLK}$ = 16 MHz |
| | | 1 | 1.9 | – | | $f_{MCLK}$ = 32 MHz |
| Erase Cycles per page | $N_{ECYC}$ CC | – | – | $5*10^4$ | cycles | |
| Total Erase Cycles | $N_{TECYC}$ CC | – | – | $2*10^6$ | cycles | |

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

### 3.3.2 Output Rise/Fall Times

**Table 19** provides the characteristics of the output rise/fall times in the XMC1200. **Figure 11** describes the rise time and fall time parameters.

**Table 19 Output Rise/Fall Times Parameters (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Rise/fall times on High Current Pad[1)2)] | $t_{HCPR}$, $t_{HCPF}$ | – | 9 | ns | 50 pF @ 5 V[3)] |
| | | – | 12 | ns | 50 pF @ 3.3 V[4)] |
| | | – | 25 | ns | 50 pF @ 1.8 V[5)] |
| Rise/fall times on Standard Pad[1)2)] | $t_R$, $t_F$ | – | 12 | ns | 50 pF @ 5 V[6)] |
| | | – | 15 | ns | 50 pF @ 3.3 V[7)]. |
| | | – | 31 | ns | 50 pF @ 1.8 V[8)]. |

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
3) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
4) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
5) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
6) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
7) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
8) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

**Figure 15** shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

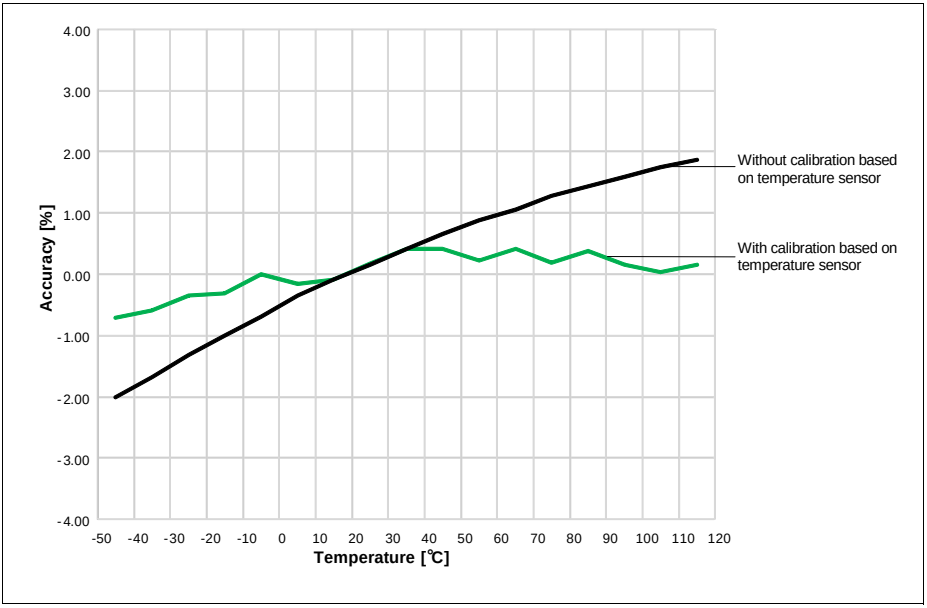


**Figure 15 Typical DCO1 accuracy over temperature**

**Table 22** provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1200.

**Table 22 32 kHz DCO2 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | 32.5 | 32.75 | 33 | kHz | under nominal conditions[1] after trimming |
| Accuracy | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature (0 °C to 85 °C)[2] |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature (-40 °C to 105 °C)[2] |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

### 3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 23 SWD Interface Timing Parameters**(Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SWDCLK high time | $t_1$ SR | 50 | – | 500000 | ns | – |
| SWDCLK low time | $t_2$ SR | 50 | – | 500000 | ns | – |
| SWDIO input setup to SWDCLK rising edge | $t_3$ SR | 10 | – | – | ns | – |
| SWDIO input hold after SWDCLK rising edge | $t_4$ SR | 10 | – | – | ns | – |
| SWDIO output valid time after SWDCLK rising edge | $t_5$ CC | – | – | 68 | ns | $C_L$ = 50 pF |
| | | – | – | 62 | ns | $C_L$ = 30 pF |
| SWDIO output hold time from SWDCLK rising edge | $t_6$ CC | 4 | – | – | ns | |

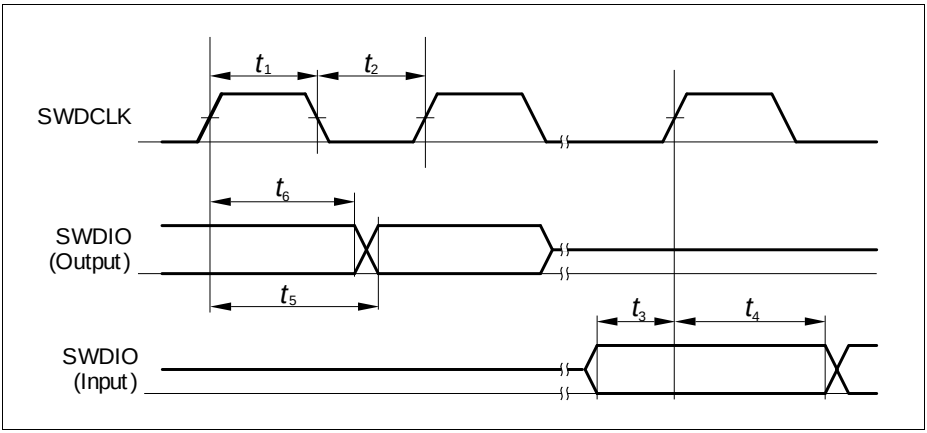


**Figure 16 SWD Timing**

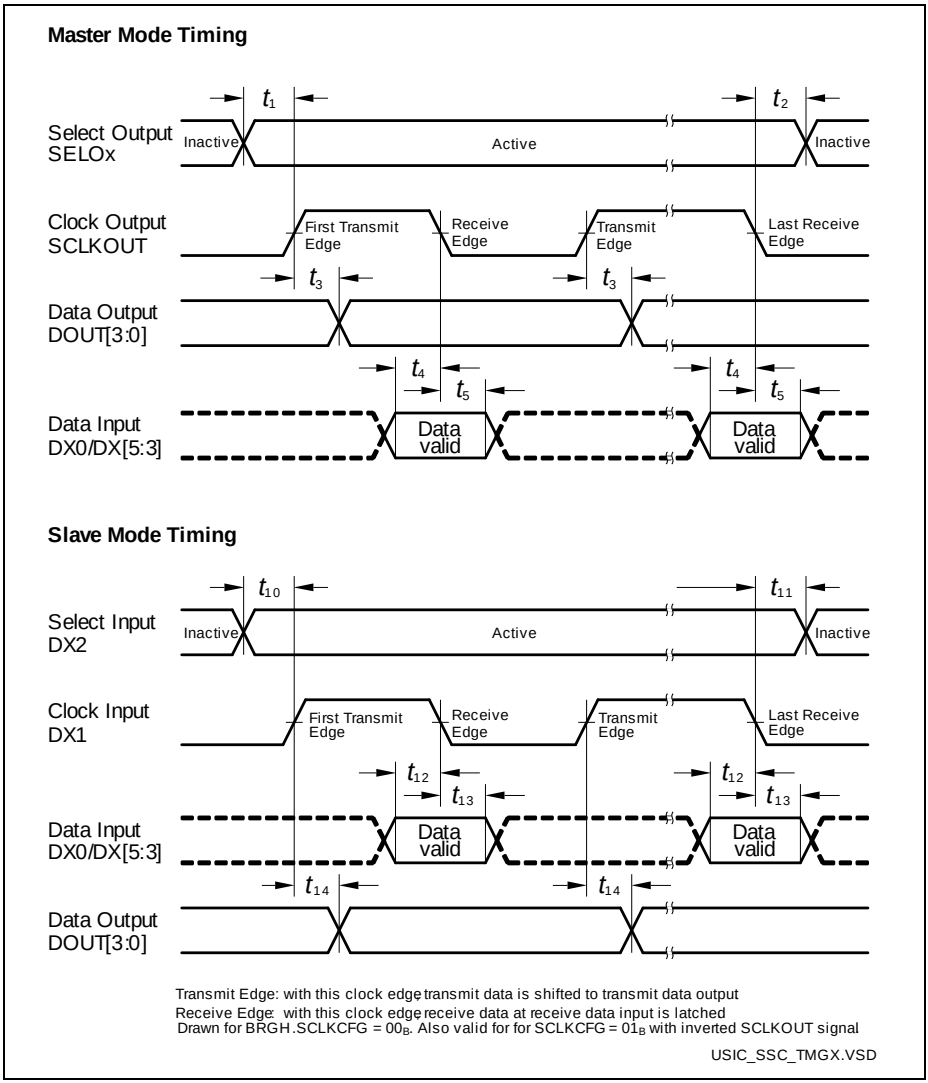


**Figure 17 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

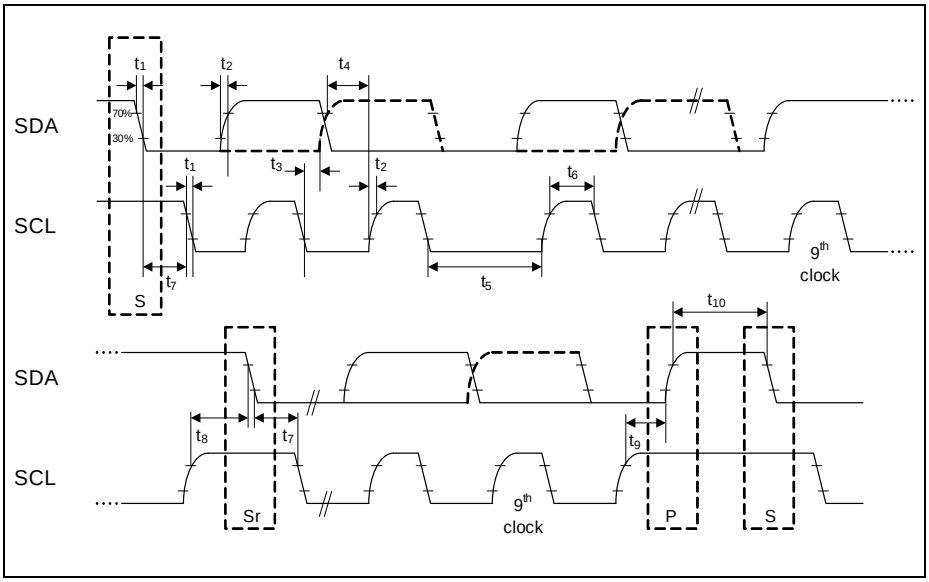


**Figure 18 USIC IIC Stand and Fast Mode Timing**

### 3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 29 USIC IIS Master Transmitter Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_1$ CC | $2/f_{MCLK}$ | - | - | ns | $V_{DDP} \geq 3$ V |
| | | $4/f_{MCLK}$ | - | - | ns | $V_{DDP} < 3$ V |
| Clock HIGH | $t_2$ CC | 0.35 x $t_{1min}$ | - | - | ns | |
| Clock Low | $t_3$ CC | 0.35 x $t_{1min}$ | - | - | ns | |
| Hold time | $t_4$ CC | 0 | - | - | ns | |
| Clock rise time | $t_5$ CC | - | - | 0.15 x $t_{1min}$ | ns | |

## 4.2 Package Outlines

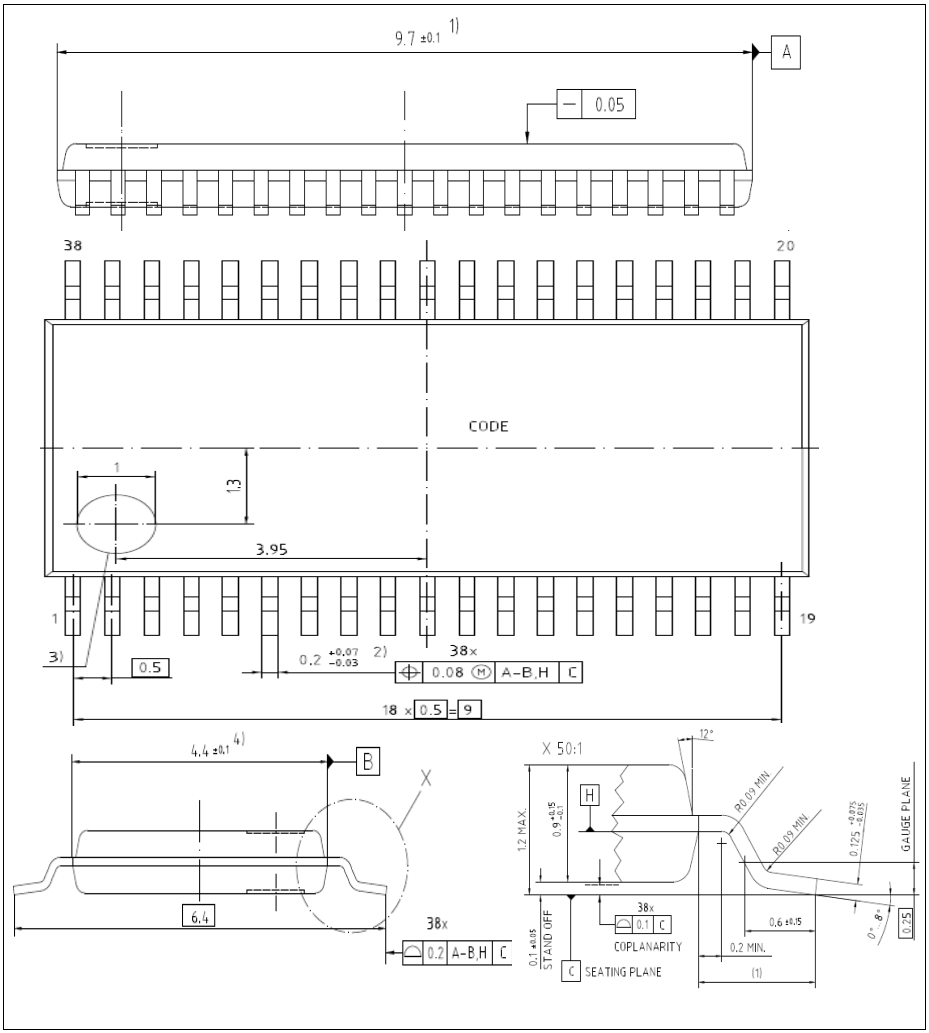


**Figure 21 PG-TSSOP-38-9**

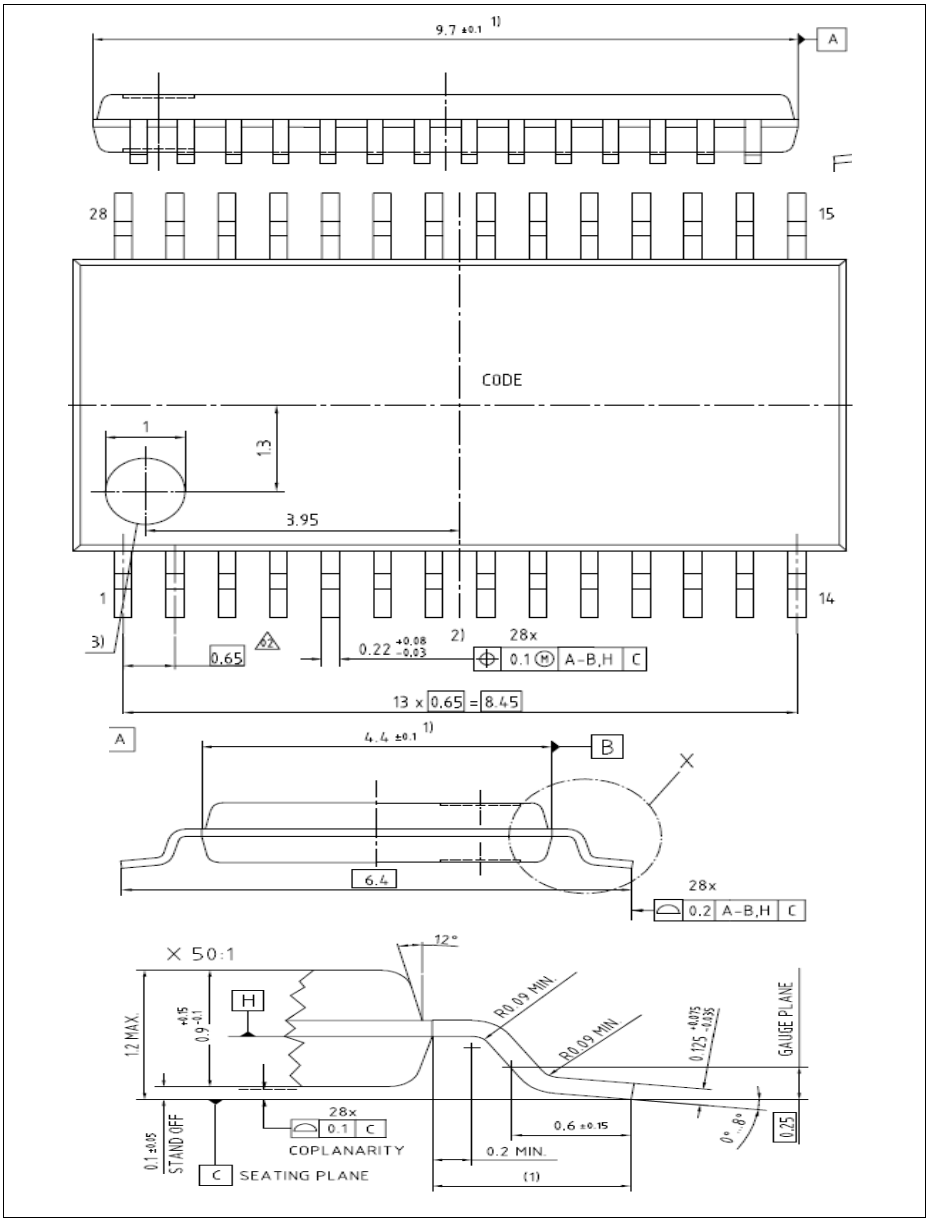


**Figure 22 PG-TSSOP-28-16**

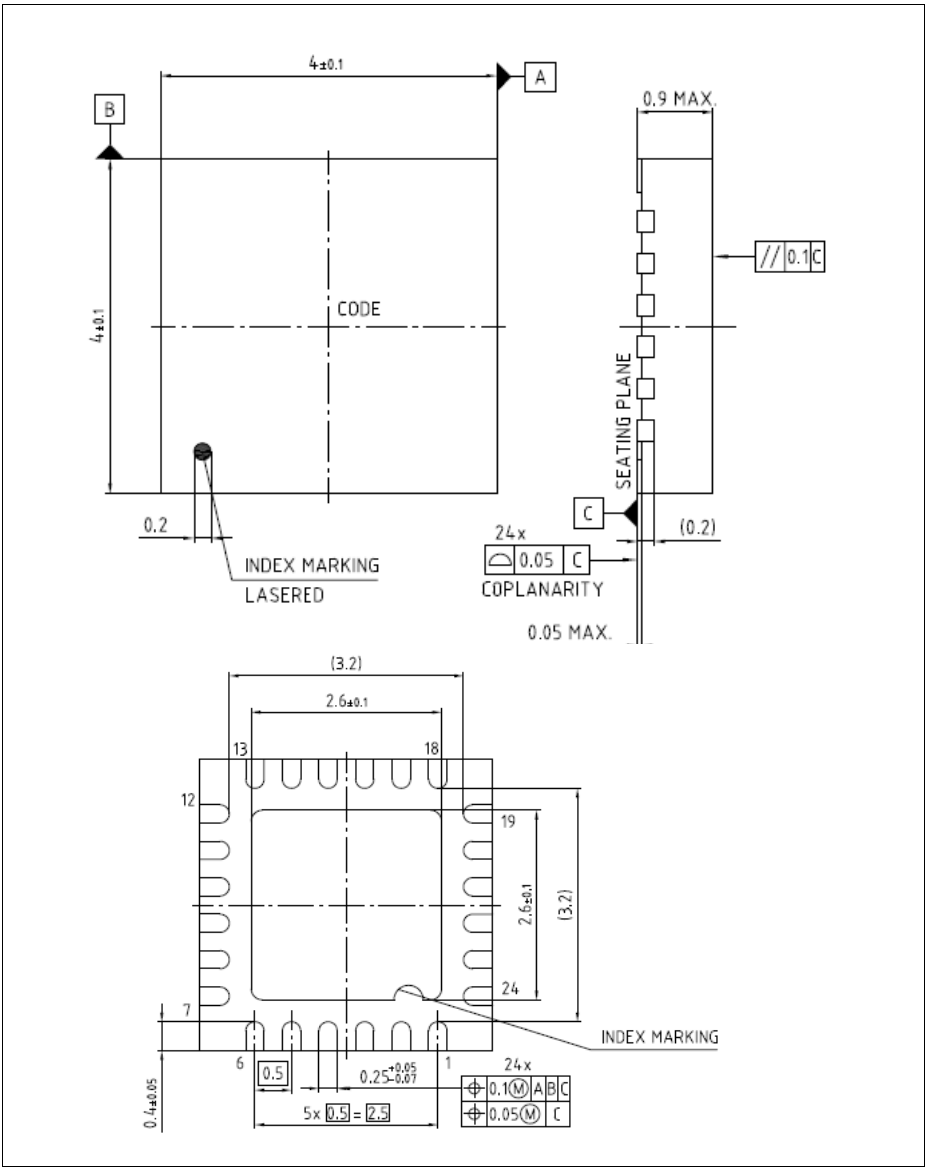


**Figure 24 PG-VQFN-24-19**

# 5 Quality Declaration

Table 32 shows the characteristics of the quality parameters in the XMC1200.

**Table 32 Quality Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | - | 2000 | V | Conforming to EIA/JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) pins | $V_{CDM}$ SR | - | 500 | V | Conforming to JESD22-C101-C |
| Moisture sensitivity level | $MSL$ CC | - | 3 | - | JEDEC J-STD-020C |

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