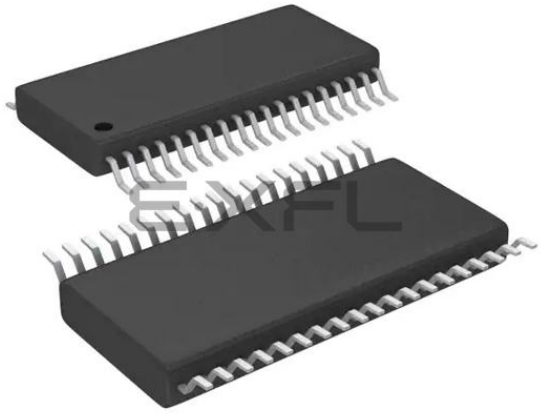
Infineon Technologies - XMC1201T038F0064AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1201t038f0064aaxuma1

1 Summary of Features

The XMC1200 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1200 series devices are optimized for LED Lighting and Human-Machine interface (HMI) applications.

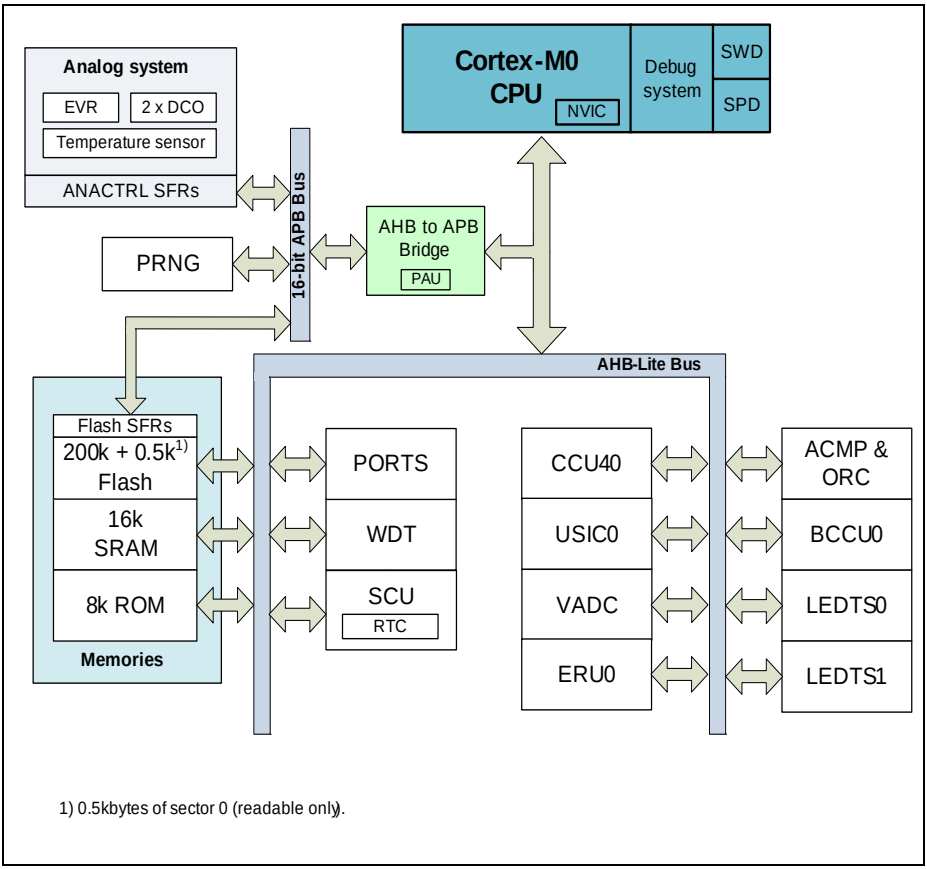

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M0 CPU
  - Most of 16-bit Thumb instruction set
  - Subset of 32-bit Thumb2 instruction set

Table 1 Synopsis of XMC1200 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1200-T038F0200	PG-TSSOP-38-9	200	16
XMC1202-T028X0016	PG-TSSOP-28-16	16	16
XMC1202-T028X0032	PG-TSSOP-28-16	32	16
XMC1202-T016X0016	PG-TSSOP-16-8	16	16
XMC1202-T016X0032	PG-TSSOP-16-8	32	16
XMC1202-Q024X0016	PG-VQFN-24-19	16	16
XMC1202-Q024X0032	PG-VQFN-24-19	32	16
XMC1201-Q040F0016	PG-VQFN-40-13	16	16
XMC1201-Q040F0032	PG-VQFN-40-13	32	16
XMC1201-Q040F0064	PG-VQFN-40-13	64	16
XMC1201-Q040F0128	PG-VQFN-40-13	128	16
XMC1201-Q040F0200	PG-VQFN-40-13	200	16
XMC1202-Q040X0016	PG-VQFN-40-13	16	16
XMC1202-Q040X0032	PG-VQFN-40-13	32	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1200 Device Types[1)]

Derivative	ADC channel	ACMP	BCCU	LEDTS
XMC1200-T038	16	3	1	2
XMC1201-T038	16	-	-	2
XMC1202-T028	14	3	1	-
XMC1202-T016	11	2	1	-
XMC1202-Q024	13	3	1	-
XMC1201-Q040	16	-	-	2
XMC1202-Q040	16	3	1	-

1) Features that are not included in this table are available in all the derivatives

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	13	15	7	STD_INOUT	
P0.1	24	18	-	-	-	STD_INOUT	
P0.2	25	19	-	-	-	STD_INOUT	
P0.3	26	20	-	-	-	STD_INOUT	
P0.4	27	21	14	-	-	STD_INOUT	
P0.5	28	22	15	16	8	STD_INOUT	
P0.6	29	23	16	17	9	STD_INOUT	
P0.7	30	24	17	18	10	STD_INOUT	
P0.8	33	27	18	19	11	STD_INOUT	
P0.9	34	28	19	20	12	STD_INOUT	
P0.10	35	29	20	-	-	STD_INOUT	
P0.11	36	30	-	-	-	STD_INOUT	
P0.12	37	31	21	21	-	STD_INOUT	

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.13	38	32	22	22	-	STD_INOUT	
P0.14	39	33	23	23	13	STD_INOUT	
P0.15	40	34	24	24	14	STD_INOUT	
P1.0	22	16	12	14	-	High Current	
P1.1	21	15	11	13	-	High Current	
P1.2	20	14	10	12	-	High Current	
P1.3	19	13	9	11	-	High Current	
P1.4	18	12	-	-	-	High Current	
P1.5	17	11	-	-	-	High Current	
P1.6	16	-	-	-	-	STD_INOUT	
P2.0	1	35	25	1	15	STD_INOUT /AN	
P2.1	2	36	26	2	-	STD_INOUT /AN	
P2.2	3	37	27	3	-	STD_IN/AN	
P2.3	4	38	-	-	-	STD_IN/AN	
P2.4	5	1	-	-	-	STD_IN/AN	
P2.5	6	2	28	-	-	STD_IN/AN	
P2.6	7	3	1	4	16	STD_IN/AN	
P2.7	8	4	2	5	1	STD_IN/AN	
P2.8	9	5	3	5	1	STD_IN/AN	
P2.9	10	6	4	6	2	STD_IN/AN	
P2.10	11	7	5	7	3	STD_INOUT /AN	
P2.11	12	8	6	8	4	STD_INOUT /AN	
VSS	13	9	7	9	5	Power	Supply GND, ADC reference GND

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 8 Port I/O Functions

Function	Outputs									Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0. PDOUT0	LEDTS0. LINE7	ERU0. GOUT0	CCU40. OUT0		USIC0_CH0. SELO0	USIC0_CH1. SELO0	LEDTS0. EXTENDED7		LEDTS0. TSIN7	LEDTS0. TSIN7	BCCU0. TRAPINB	CCU40.IN0C			USIC0_CH0. DX2A	USIC0_CH1. DX2A		
P0.1	ERU0. PDOUT1	LEDTS0. LINE6	ERU0. GOUT1	CCU40. OUT1		BCCU0. OUT8	SCU. VDROP	LEDTS0. EXTENDED6		LEDTS0. TSIN6	LEDTS0. TSIN6		CCU40.IN1C						
P0.2	ERU0. PDOUT2	LEDTS0. LINE5	ERU0. GOUT2	CCU40. OUT2		VADC0. EMUX02		LEDTS0. EXTENDED5		LEDTS0. TSIN5	LEDTS0. TSIN5		CCU40.IN2C						
P0.3	ERU0. PDOUT3	LEDTS0. LINE4	ERU0. GOUT3	CCU40. OUT3		VADC0. EMUX01		LEDTS0. EXTENDED4		LEDTS0. TSIN4	LEDTS0. TSIN4		CCU40.IN3C						
P0.4	BCCU0. OUT0	LEDTS0. LINE3	LEDTS0. COL3	CCU40. OUT1		VADC0. EMUX00	WWDT. SERVICE_OUT	LEDTS0. EXTENDED3		LEDTS0. TSIN3	LEDTS0. TSIN3								
P0.5	BCCU0. OUT1	LEDTS0. LINE2	LEDTS0. COL2	CCU40. OUT0		ACMP2. OUT		LEDTS0. EXTENDED2		LEDTS0. TSIN2	LEDTS0. TSIN2								
P0.6	BCCU0. OUT2	LEDTS0. LINE1	LEDTS0. COL1	CCU40. OUT0		USIC0_CH1. MCLKOUT	USIC0_CH1. DOUT0	LEDTS0. EXTENDED1		LEDTS0. TSIN1	LEDTS0. TSIN1		CCU40.IN0B			USIC0_CH1. DX0C			
P0.7	BCCU0. OUT3	LEDTS0. LINE0	LEDTS0. COL0	CCU40. OUT1		USIC0_CH0. SCLKOUT	USIC0_CH1. DOUT0	LEDTS0. EXTENDED0		LEDTS0. TSIN0	LEDTS0. TSIN0		CCU40.IN1B			USIC0_CH0. DX1C	USIC0_CH1. DX0D	USIC0_CH1. DX1C	
P0.8	BCCU0. OUT4	LEDTS1. LINE0	LEDTS0. COLA	CCU40. OUT2		USIC0_CH0. SCLKOUT	USIC0_CH1. SCLKOUT	LEDTS1. EXTENDED0		LEDTS1. TSIN0	LEDTS1. TSIN0		CCU40.IN2B			USIC0_CH0. DX1B	USIC0_CH1. DX1B		
P0.9	BCCU0. OUT5	LEDTS1. LINE1	LEDTS0. COL6	CCU40. OUT3		USIC0_CH0. SELO0	USIC0_CH1. SELO0	LEDTS1. EXTENDED1		LEDTS1. TSIN1	LEDTS1. TSIN1		CCU40.IN3B			USIC0_CH0. DX2B	USIC0_CH1. DX2B		
P0.10	BCCU0. OUT6	LEDTS1. LINE2	LEDTS0. COL5	ACMP0. OUT		USIC0_CH0. SELO1	USIC0_CH1. SELO1	LEDTS1. EXTENDED2		LEDTS1. TSIN2	LEDTS1. TSIN2					USIC0_CH0. DX2C	USIC0_CH1. DX2C		
P0.11	BCCU0. OUT7	LEDTS1. LINE3	LEDTS0. COL4	USIC0_CH0. MCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO2	LEDTS1. EXTENDED3		LEDTS1. TSIN3	LEDTS1. TSIN3					USIC0_CH0. DX2D	USIC0_CH1. DX2D		
P0.12	BCCU0. OUT6	LEDTS1. LINE4	LEDTS0. COL3	LEDTS1. COL3		USIC0_CH0. SELO3		LEDTS1. EXTENDED4		LEDTS1. TSIN4	LEDTS1. TSIN4	BCCU0. TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0. DX2E		
P0.13	WWDT. SERVICE_OUT	LEDTS1. LINE5	LEDTS0. COL2	LEDTS1. COL2		USIC0_CH0. SELO4		LEDTS1. EXTENDED5		LEDTS1. TSIN5	LEDTS1. TSIN5					USIC0_CH0. DX2F			
P0.14	BCCU0. OUT7	LEDTS1. LINE6	LEDTS0. COL1	LEDTS1. COL1		USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT	LEDTS1. EXTENDED6		LEDTS1. TSIN6	LEDTS1. TSIN6					USIC0_CH0. DX0A	USIC0_CH0. DX1A		
P0.15	BCCU0. OUT8	LEDTS1. LINE7	LEDTS0. COL0	LEDTS1. COL0		USIC0_CH0. DOUT0	USIC0_CH1. MCLKOUT	LEDTS1. EXTENDED7		LEDTS1. TSIN7	LEDTS1. TSIN7					USIC0_CH0. DX0B			
P1.0	BCCU0. OUT0	CCU40. OUT0	LEDTS0. COL0	LEDTS1. COLA		ACMP1. OUT	USIC0_CH0. DOUT0		USIC0_CH0. DOUT0		USIC0_CH0. HWIN0					USIC0_CH0. DX0C			
P1.1	VADC0. EMUX00	CCU40. OUT1	LEDTS0. COL1	LEDTS1. COL0		USIC0_CH0. DOUT0	USIC0_CH1. SELO0		USIC0_CH0. DOUT1		USIC0_CH0. HWIN1					USIC0_CH0. DX0D	USIC0_CH0. DX1D	USIC0_CH1. DX2E	
P1.2	VADC0. EMUX01	CCU40. OUT2	LEDTS0. COL2	LEDTS1. COL1		ACMP2. OUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT2		USIC0_CH0. HWIN2					USIC0_CH1. DX0B			
P1.3	VADC0. EMUX02	CCU40. OUT3	LEDTS0. COL3	LEDTS1. COL2		USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT3		USIC0_CH0. HWIN3					USIC0_CH1. DX0A	USIC0_CH1. DX1A		
P1.4	VADC0. EMUX10	USIC0_CH1. SCLKOUT	LEDTS0. COL4	LEDTS1. COL3		USIC0_CH0. SELO0	USIC0_CH1. SELO1									USIC0_CH0. DX5E	USIC0_CH1. DX5E		
P1.5	VADC0. EMUX11	USIC0_CH0. DOUT0	LEDTS0. COLA	BCCU0. OUT1		USIC0_CH0. SELO1	USIC0_CH1. SELO2									USIC0_CH1. DX5F			

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P1.6	VADC0. EMUX12	USIC0_CH1. DOUT0	LEDTS0. COL5	USIC0_CH0. SCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO3							USIC0_CH0. DX5F					
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3	LEDTS1. COL5		USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT						VADC0. G0CH5		ERU0.0B0	USIC0_CH0. DX0E	USIC0_CH0. DX1E	USIC0_CH1. DX2F	
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2	LEDTS1. COL6		USIC0_CH0. DOUT0	USIC0_CH1. SCLKOUT					ACMP2.INP	VADC0. G0CH6		ERU0.1B0	USIC0_CH0. DX0F	USIC0_CH1. DX3A	USIC0_CH1. DX4A	
P2.2												ACMP2.INN	VADC0. G0CH7		ERU0.0B1	USIC0_CH0. DX3A	USIC0_CH0. DX4A	USIC0_CH1. DX5A	ORC0.AIN
P2.3													VADC0. G1CH5		ERU0.1B1	USIC0_CH0. DX5B	USIC0_CH1. DX3C	USIC0_CH1. DX4C	ORC1.AIN
P2.4													VADC0. G1CH6		ERU0.0A1	USIC0_CH0. DX3B	USIC0_CH0. DX4B	USIC0_CH1. DX5B	ORC2.AIN
P2.5													VADC0. G1CH7		ERU0.1A1	USIC0_CH0. DX5D	USIC0_CH1. DX3E	USIC0_CH1. DX4E	ORC3.AIN
P2.6												ACMP1.INN	VADC0. G0CH0		ERU0.2A1	USIC0_CH0. DX3E	USIC0_CH0. DX4E	USIC0_CH1. DX5D	ORC4.AIN
P2.7												ACMP1.INP	VADC0. G1CH1		ERU0.3A1	USIC0_CH0. DX5C	USIC0_CH1. DX3D	USIC0_CH1. DX4D	ORC5.AIN
P2.8												ACMP0.INN	VADC0. G0CH1	VADC0. G1CH0	ERU0.3B1	USIC0_CH0. DX3D	USIC0_CH0. DX4D	USIC0_CH1. DX5C	ORC6.AIN
P2.9												ACMP0.INP	VADC0. G0CH2	VADC0. G1CH4	ERU0.3B0	USIC0_CH0. DX5A	USIC0_CH1. DX3B	USIC0_CH1. DX4B	ORC7.AIN
P2.10	ERU0. PDOUT1	CCU40. OUT2	ERU0. GOUT1	LEDTS1. COL4		ACMP0. OUT	USIC0_CH1. DOUT0						VADC0. G0CH3	VADC0. G1CH2	ERU0.2B0	USIC0_CH0. DX3C	USIC0_CH0. DX4C	USIC0_CH1. DX0F	
P2.11	ERU0. PDOUT0	CCU40. OUT3	ERU0. GOUT0	LEDTS1. COL3		USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0					ACMP.REF	VADC0. G0CH4	VADC0. G1CH3	ERU0.2B1	USIC0_CH1. DX0E	USIC0_CH1. DX1E		

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1200.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1200 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1200 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1200 is designed in.

3.2.2 Analog to Digital Converters (ADC)

Table 12 shows the Analog to Digital Converter (ADC) characteristics.

Table 12 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	1.8	–	3.0	V	SHSCFG.AREF = 11_B
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground (SH0-CH0, SH1-CH0)	V_{REFGND} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Internal reference voltage (full scale value)	V_{REFINT} CC	4.82	5	5.18	V	-40°C - 105°C
		4.9	5	5.1	V	0°C - 85°C [1]
Switched capacitance of an analog input[1]	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	[1]
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	[1]

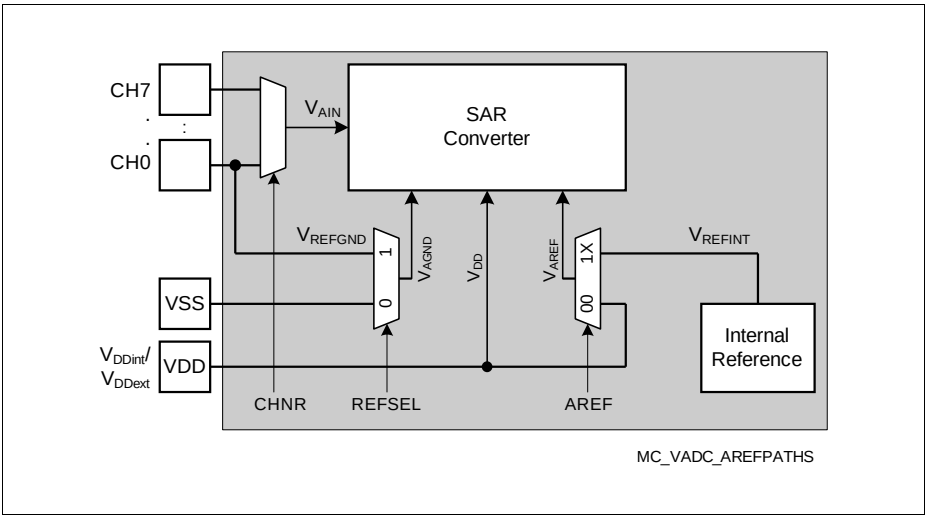

Figure 9 ADC Voltage Supply

3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

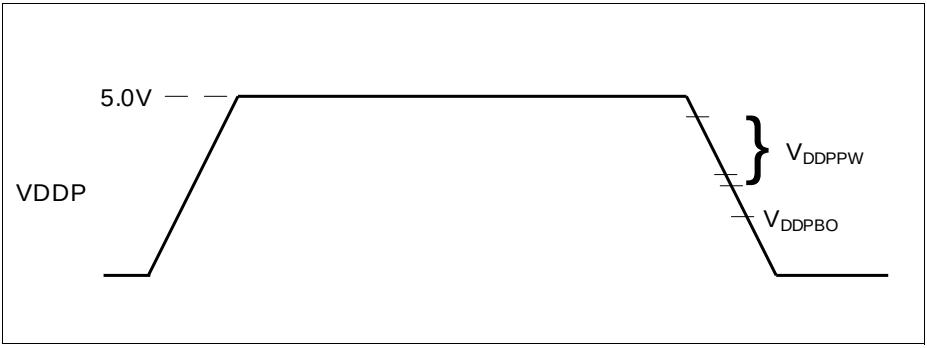

Figure 14 Supply Threshold Parameters

Figure 15 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

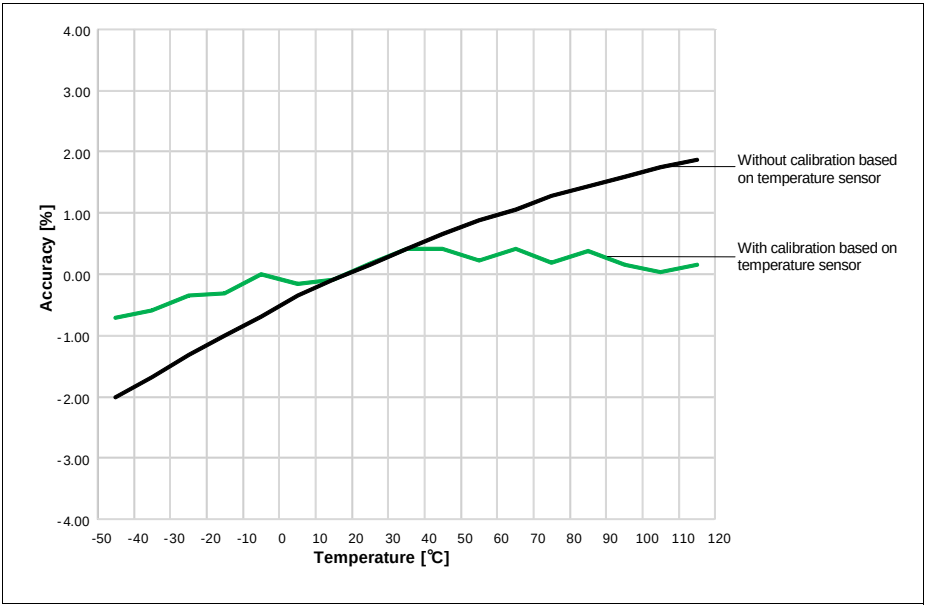

Figure 15 Typical DCO1 accuracy over temperature

Table 22 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1200.

Table 22 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	32.5	32.75	33	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

3.3.6 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 24 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

3.3.7 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.7.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 25 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	0	–	–	ns	

Table 26 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10}	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11}	SR	10	–	–	ns	

Table 26 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 28 USIC IIC Fast Mode Timing [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

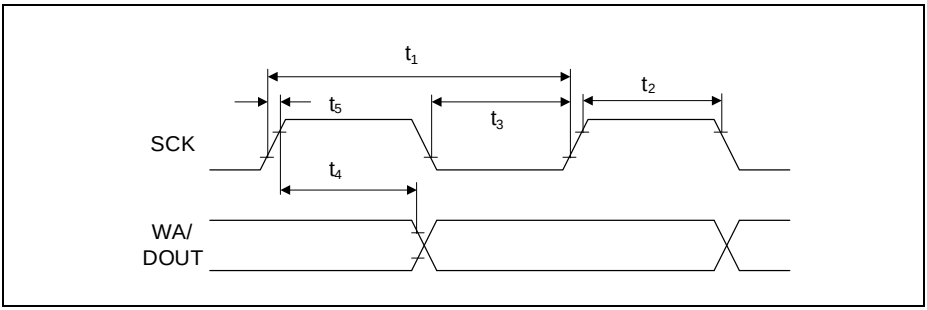

Figure 19 USIC IIS Master Transmitter Timing

Table 30 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	-	-	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

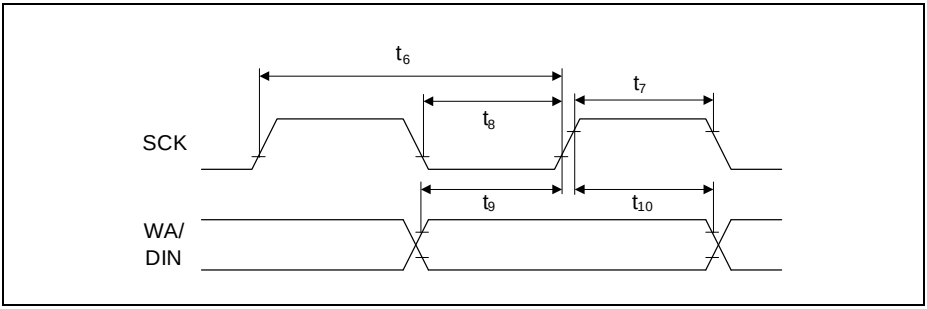

Figure 20 USIC IIS Slave Receiver Timing

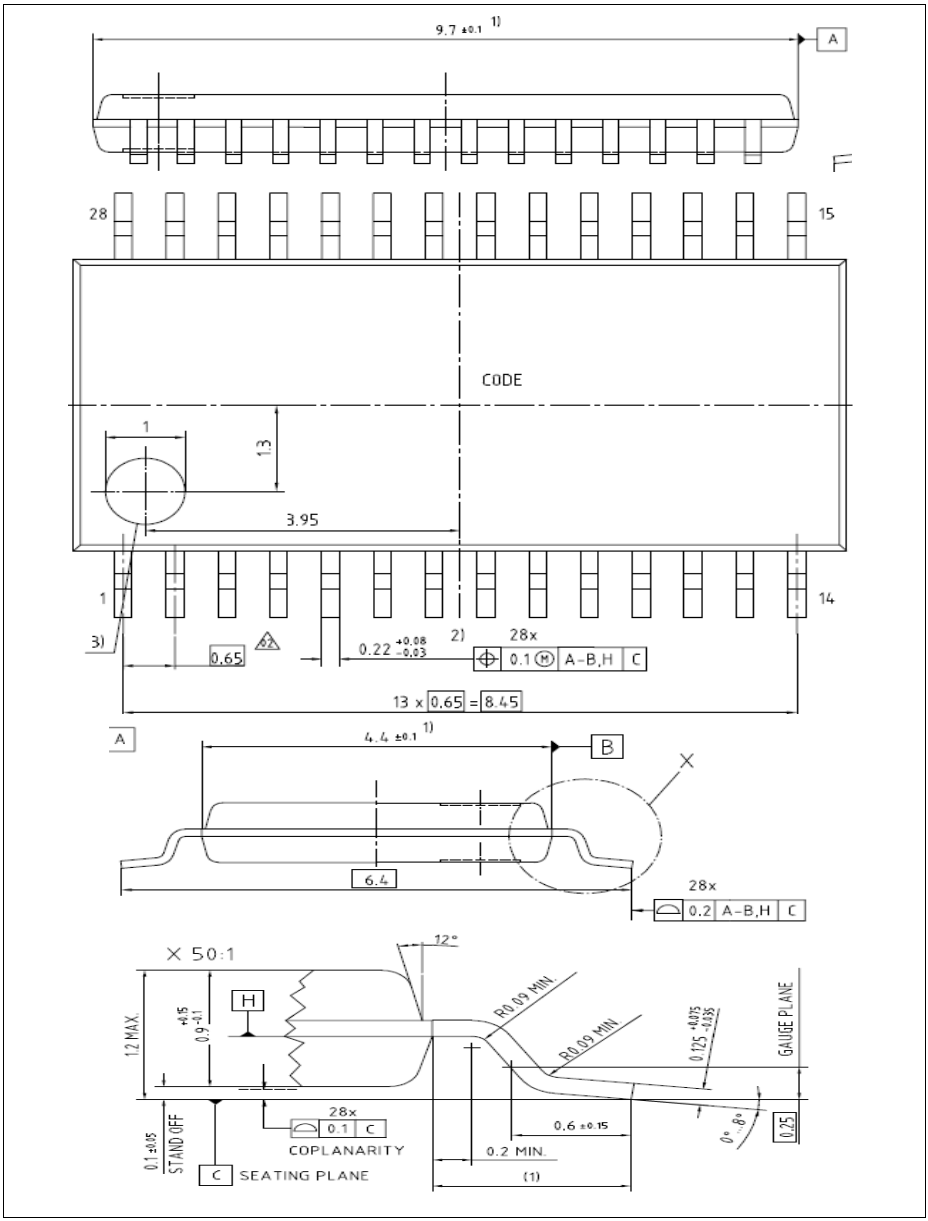

Figure 22 PG-TSSOP-28-16

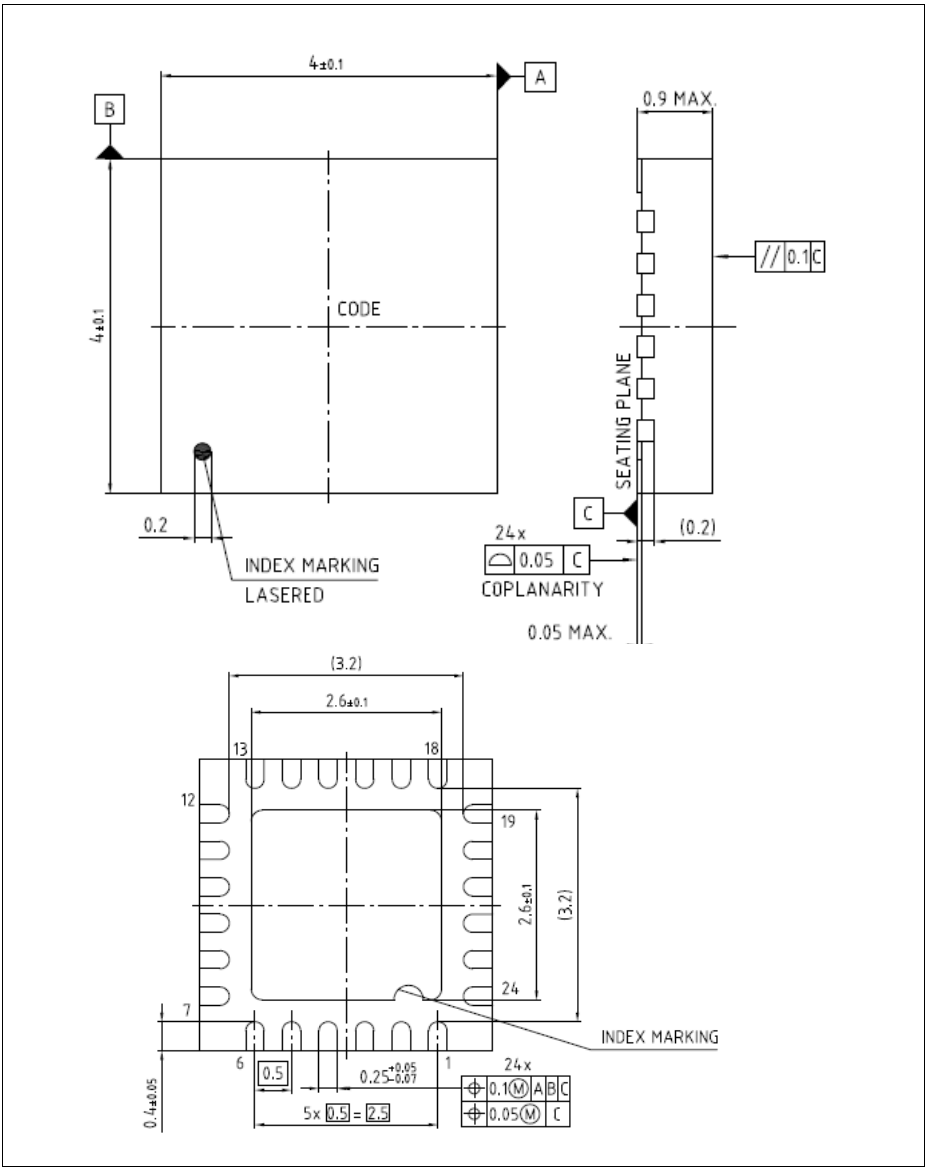

Figure 24 PG-VQFN-24-19

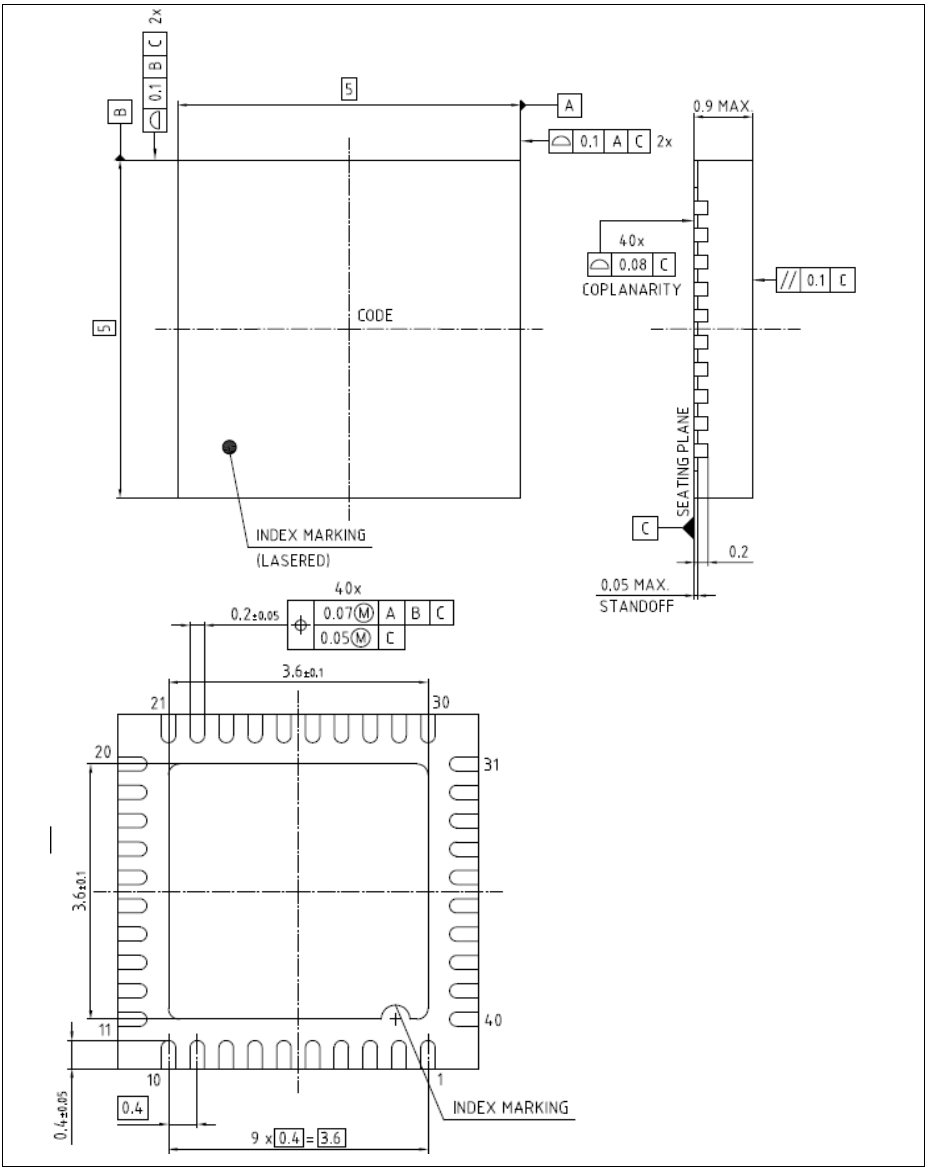

Figure 25 PG-VQFN-40-13

All dimensions in mm.