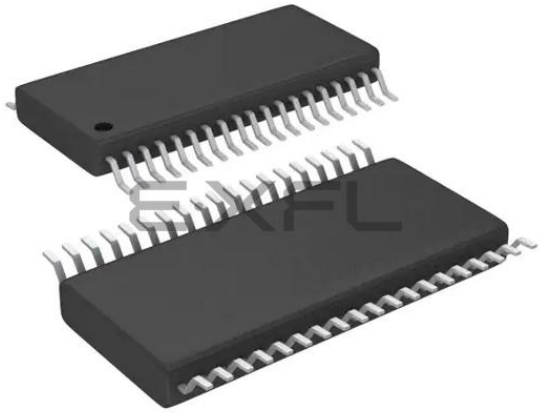
Infineon Technologies - XMC1201T038F0128ABXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1201t038f0128abxuma1

XMC1200

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex™-M0
32-bit processor core

Data Sheet

V1.4 2014-05

Microcontrollers

  - High code density with 32-bit performance
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support
  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

Communication Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

Analog Frontend Peripherals

- A/D Converters, up to 12 channels, includes 2 sample and hold stages and a fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

Industrial Control Peripherals

- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode

Table 1 Synopsis of XMC1200 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1200-T038F0200	PG-TSSOP-38-9	200	16
XMC1202-T028X0016	PG-TSSOP-28-16	16	16
XMC1202-T028X0032	PG-TSSOP-28-16	32	16
XMC1202-T016X0016	PG-TSSOP-16-8	16	16
XMC1202-T016X0032	PG-TSSOP-16-8	32	16
XMC1202-Q024X0016	PG-VQFN-24-19	16	16
XMC1202-Q024X0032	PG-VQFN-24-19	32	16
XMC1201-Q040F0016	PG-VQFN-40-13	16	16
XMC1201-Q040F0032	PG-VQFN-40-13	32	16
XMC1201-Q040F0064	PG-VQFN-40-13	64	16
XMC1201-Q040F0128	PG-VQFN-40-13	128	16
XMC1201-Q040F0200	PG-VQFN-40-13	200	16
XMC1202-Q040X0016	PG-VQFN-40-13	16	16
XMC1202-Q040X0032	PG-VQFN-40-13	32	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1200 Device Types[1)]

Derivative	ADC channel	ACMP	BCCU	LEDTS
XMC1200-T038	16	3	1	2
XMC1201-T038	16	-	-	2
XMC1202-T028	14	3	1	-
XMC1202-T016	11	2	1	-
XMC1202-Q024	13	3	1	-
XMC1201-Q040	16	-	-	2
XMC1202-Q040	16	3	1	-

1) Features that are not included in this table are available in all the derivatives

Table 3 ADC Channels [1)]

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	CH0..CH4
PG-TSSOP-28	CH0..CH7	CH0 .. CH4, CH7
PG-TSSOP-38	CH0..CH7	CH0..CH7
PG-VQFN-24	CH0..CH7	CH0..CH4
PG-VQFN-40	CH0..CH7	CH1, CH5 .. CH7

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 0F00$_H$ (MSB) - 1000 0F1B$_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 4 XMC1200 Chip Identification Number

Derivative	Value	Marking
XMC1201-T038F0016	00012012 01CF00FF 00001FF7 00006000 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1201-T038F0032	00012012 01CF00FF 00001FF7 00006000 00000B00 00001000 00009000 101ED083$_H$	AA
XMC1201-T038F0064	00012012 01CF00FF 00001FF7 00006000 00000B00 00001000 00011000 101ED083$_H$	AA
XMC1201-T038F0128	00012012 01CF00FF 00001FF7 00006000 00000B00 00001000 00021000 101ED083$_H$	AA
XMC1201-T038F0200	00012012 01CF00FF 00001FF7 00006000 00000B00 00001000 00033000 101ED083$_H$	AA
XMC1200-T038F0200	00012012 01CF00FF 00001FF7 0000E000 00000B00 00001000 00033000 101ED083$_H$	AA
XMC1202-T028X0016	00012023 01CF00FF 00001FF7 00008000 00000B00 00001000 00005000 101ED083$_H$	AA
XMC1202-T028X0032	00012023 01CF00FF 00001FF7 00008000 00000B00 00001000 00009000 101ED083$_H$	AA

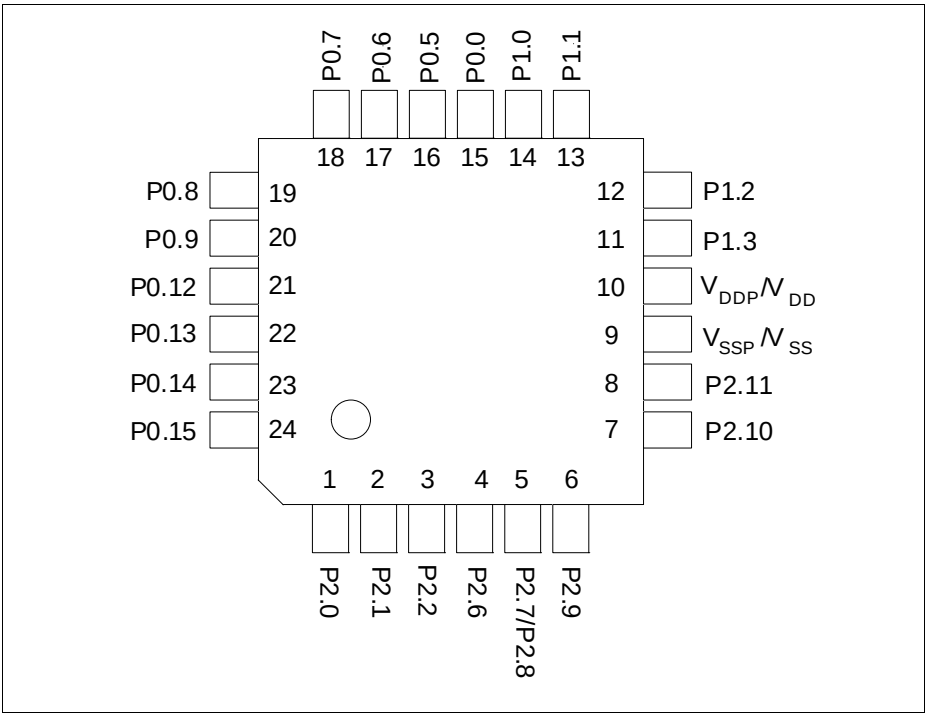

Figure 7 XMC1200 PG-VQFN-24 Pin Configuration (top view)

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 8 Port I/O Functions

Function	Outputs									Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0. PDOUT0	LEDTS0. LINE7	ERU0. GOUT0	CCU40. OUT0		USIC0_CH0. SELO0	USIC0_CH1. SELO0	LEDTS0. EXTENDED7		LEDTS0. TSIN7	LEDTS0. TSIN7	BCCU0. TRAPINB	CCU40.IN0C			USIC0_CH0. DX2A	USIC0_CH1. DX2A		
P0.1	ERU0. PDOUT1	LEDTS0. LINE6	ERU0. GOUT1	CCU40. OUT1		BCCU0. OUT8	SCU. VDROP	LEDTS0. EXTENDED6		LEDTS0. TSIN6	LEDTS0. TSIN6		CCU40.IN1C						
P0.2	ERU0. PDOUT2	LEDTS0. LINE5	ERU0. GOUT2	CCU40. OUT2		VADC0. EMUX02		LEDTS0. EXTENDED5		LEDTS0. TSIN5	LEDTS0. TSIN5		CCU40.IN2C						
P0.3	ERU0. PDOUT3	LEDTS0. LINE4	ERU0. GOUT3	CCU40. OUT3		VADC0. EMUX01		LEDTS0. EXTENDED4		LEDTS0. TSIN4	LEDTS0. TSIN4		CCU40.IN3C						
P0.4	BCCU0. OUT0	LEDTS0. LINE3	LEDTS0. COL3	CCU40. OUT1		VADC0. EMUX00	WWDT. SERVICE_OUT	LEDTS0. EXTENDED3		LEDTS0. TSIN3	LEDTS0. TSIN3								
P0.5	BCCU0. OUT1	LEDTS0. LINE2	LEDTS0. COL2	CCU40. OUT0		ACMP2. OUT		LEDTS0. EXTENDED2		LEDTS0. TSIN2	LEDTS0. TSIN2								
P0.6	BCCU0. OUT2	LEDTS0. LINE1	LEDTS0. COL1	CCU40. OUT0		USIC0_CH1. MCLKOUT	USIC0_CH1. DOUT0	LEDTS0. EXTENDED1		LEDTS0. TSIN1	LEDTS0. TSIN1		CCU40.IN0B			USIC0_CH1. DX0C			
P0.7	BCCU0. OUT3	LEDTS0. LINE0	LEDTS0. COL0	CCU40. OUT1		USIC0_CH0. SCLKOUT	USIC0_CH1. DOUT0	LEDTS0. EXTENDED0		LEDTS0. TSIN0	LEDTS0. TSIN0		CCU40.IN1B			USIC0_CH0. DX1C	USIC0_CH1. DX0D	USIC0_CH1. DX1C	
P0.8	BCCU0. OUT4	LEDTS1. LINE0	LEDTS0. COLA	CCU40. OUT2		USIC0_CH0. SCLKOUT	USIC0_CH1. SCLKOUT	LEDTS1. EXTENDED0		LEDTS1. TSIN0	LEDTS1. TSIN0		CCU40.IN2B			USIC0_CH0. DX1B	USIC0_CH1. DX1B		
P0.9	BCCU0. OUT5	LEDTS1. LINE1	LEDTS0. COL6	CCU40. OUT3		USIC0_CH0. SELO0	USIC0_CH1. SELO0	LEDTS1. EXTENDED1		LEDTS1. TSIN1	LEDTS1. TSIN1		CCU40.IN3B			USIC0_CH0. DX2B	USIC0_CH1. DX2B		
P0.10	BCCU0. OUT6	LEDTS1. LINE2	LEDTS0. COL5	ACMP0. OUT		USIC0_CH0. SELO1	USIC0_CH1. SELO1	LEDTS1. EXTENDED2		LEDTS1. TSIN2	LEDTS1. TSIN2					USIC0_CH0. DX2C	USIC0_CH1. DX2C		
P0.11	BCCU0. OUT7	LEDTS1. LINE3	LEDTS0. COL4	USIC0_CH0. MCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO2	LEDTS1. EXTENDED3		LEDTS1. TSIN3	LEDTS1. TSIN3					USIC0_CH0. DX2D	USIC0_CH1. DX2D		
P0.12	BCCU0. OUT6	LEDTS1. LINE4	LEDTS0. COL3	LEDTS1. COL3		USIC0_CH0. SELO3		LEDTS1. EXTENDED4		LEDTS1. TSIN4	LEDTS1. TSIN4	BCCU0. TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0. DX2E		
P0.13	WWDT. SERVICE_OUT	LEDTS1. LINE5	LEDTS0. COL2	LEDTS1. COL2		USIC0_CH0. SELO4		LEDTS1. EXTENDED5		LEDTS1. TSIN5	LEDTS1. TSIN5					USIC0_CH0. DX2F			
P0.14	BCCU0. OUT7	LEDTS1. LINE6	LEDTS0. COL1	LEDTS1. COL1		USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT	LEDTS1. EXTENDED6		LEDTS1. TSIN6	LEDTS1. TSIN6					USIC0_CH0. DX0A	USIC0_CH0. DX1A		
P0.15	BCCU0. OUT8	LEDTS1. LINE7	LEDTS0. COL0	LEDTS1. COL0		USIC0_CH0. DOUT0	USIC0_CH1. MCLKOUT	LEDTS1. EXTENDED7		LEDTS1. TSIN7	LEDTS1. TSIN7					USIC0_CH0. DX0B			
P1.0	BCCU0. OUT0	CCU40. OUT0	LEDTS0. COL0	LEDTS1. COLA		ACMP1. OUT	USIC0_CH0. DOUT0		USIC0_CH0. DOUT0		USIC0_CH0. HWIN0					USIC0_CH0. DX0C			
P1.1	VADC0. EMUX00	CCU40. OUT1	LEDTS0. COL1	LEDTS1. COL0		USIC0_CH0. DOUT0	USIC0_CH1. SELO0		USIC0_CH0. DOUT1		USIC0_CH0. HWIN1					USIC0_CH0. DX0D	USIC0_CH0. DX1D	USIC0_CH1. DX2E	
P1.2	VADC0. EMUX01	CCU40. OUT2	LEDTS0. COL2	LEDTS1. COL1		ACMP2. OUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT2		USIC0_CH0. HWIN2					USIC0_CH1. DX0B			
P1.3	VADC0. EMUX02	CCU40. OUT3	LEDTS0. COL3	LEDTS1. COL2		USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT3		USIC0_CH0. HWIN3					USIC0_CH1. DX0A	USIC0_CH1. DX1A		
P1.4	VADC0. EMUX10	USIC0_CH1. SCLKOUT	LEDTS0. COL4	LEDTS1. COL3		USIC0_CH0. SELO0	USIC0_CH1. SELO1									USIC0_CH0. DX5E	USIC0_CH1. DX5E		
P1.5	VADC0. EMUX11	USIC0_CH0. DOUT0	LEDTS0. COLA	BCCU0. OUT1		USIC0_CH0. SELO1	USIC0_CH1. SELO2									USIC0_CH1. DX5F			

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P1.6	VADC0. EMUX12	USIC0_CH1. DOUT0	LEDTS0. COL5	USIC0_CH0. SCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO3							USIC0_CH0. DX5F					
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3	LEDTS1. COL5		USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT						VADC0. G0CH5		ERU0.0B0	USIC0_CH0. DX0E	USIC0_CH0. DX1E	USIC0_CH1. DX2F	
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2	LEDTS1. COL6		USIC0_CH0. DOUT0	USIC0_CH1. SCLKOUT					ACMP2.INP	VADC0. G0CH6		ERU0.1B0	USIC0_CH0. DX0F	USIC0_CH1. DX3A	USIC0_CH1. DX4A	
P2.2												ACMP2.INN	VADC0. G0CH7		ERU0.0B1	USIC0_CH0. DX3A	USIC0_CH0. DX4A	USIC0_CH1. DX5A	ORC0.AIN
P2.3													VADC0. G1CH5		ERU0.1B1	USIC0_CH0. DX5B	USIC0_CH1. DX3C	USIC0_CH1. DX4C	ORC1.AIN
P2.4													VADC0. G1CH6		ERU0.0A1	USIC0_CH0. DX3B	USIC0_CH0. DX4B	USIC0_CH1. DX5B	ORC2.AIN
P2.5													VADC0. G1CH7		ERU0.1A1	USIC0_CH0. DX5D	USIC0_CH1. DX3E	USIC0_CH1. DX4E	ORC3.AIN
P2.6												ACMP1.INN	VADC0. G0CH0		ERU0.2A1	USIC0_CH0. DX3E	USIC0_CH0. DX4E	USIC0_CH1. DX5D	ORC4.AIN
P2.7												ACMP1.INP	VADC0. G1CH1		ERU0.3A1	USIC0_CH0. DX5C	USIC0_CH1. DX3D	USIC0_CH1. DX4D	ORC5.AIN
P2.8												ACMP0.INN	VADC0. G0CH1	VADC0. G1CH0	ERU0.3B1	USIC0_CH0. DX3D	USIC0_CH0. DX4D	USIC0_CH1. DX5C	ORC6.AIN
P2.9												ACMP0.INP	VADC0. G0CH2	VADC0. G1CH4	ERU0.3B0	USIC0_CH0. DX5A	USIC0_CH1. DX3B	USIC0_CH1. DX4B	ORC7.AIN
P2.10	ERU0. PDOUT1	CCU40. OUT2	ERU0. GOUT1	LEDTS1. COL4		ACMP0. OUT	USIC0_CH1. DOUT0						VADC0. G0CH3	VADC0. G1CH2	ERU0.2B0	USIC0_CH0. DX3C	USIC0_CH0. DX4C	USIC0_CH1. DX0F	
P2.11	ERU0. PDOUT0	CCU40. OUT3	ERU0. GOUT0	LEDTS1. COL3		USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0					ACMP.REF	VADC0. G0CH4	VADC0. G1CH3	ERU0.2B1	USIC0_CH1. DX0E	USIC0_CH1. DX1E		

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1200.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1200 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1200 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1200 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_S	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on any pin with respect to V_{SSP}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on any analog input pin with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	–
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	SR	–	–	50	mA	–
Analog comparator input voltage	V_{CM}	SR	-0.3	–	V_{DDP} + 0.3	V	

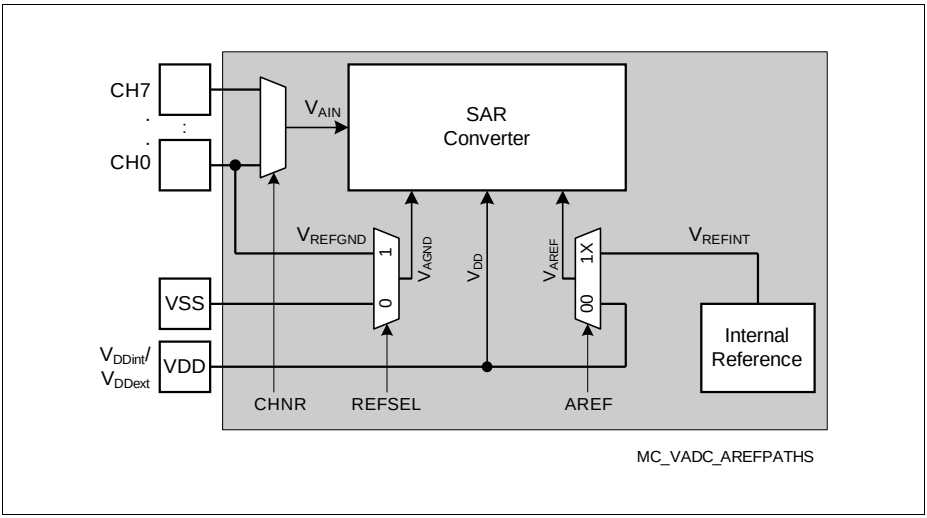

Figure 9 ADC Voltage Supply

3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Table 16 Power Supply Parameters[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[2)]	Max.		
Active mode current[3)]	I_{DDPA} CC	–	8.8	11.5	mA	f_{MCLK} = 32 MHz f_{PCLK} = 64 MHz
		–	3.9	–	mA	f_{MCLK} = 1 MHz f_{PCLK} = 1 MHz
Sleep mode current Peripherals clock enabled[4)]	I_{DDPSE} CC	–	6.2	–	mA	f_{MCLK} = 32 MHz f_{PCLK} = 64 MHz
Sleep mode current Peripherals clock disabled[5)]	I_{DDPSD} CC	–	1.2	–	mA	f_{MCLK} = 1 MHz f_{PCLK} = 1 MHz
Deep Sleep mode current[6)]	I_{DDPDS} CC	–	0.24	–	mA	
Wake-up time from Sleep to Active mode[7)]	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode[8)]	t_{DSA} CC	–	280	–	µsec	

1) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.

2) The typical values are measured at T_A = + 25 °C and V_{DDP} = 5 V.

3) CPU and all peripherals clock enabled, Flash is in active mode.

4) CPU is sleep, all peripherals clock enabled and Flash is in active mode.

5) CPU is sleep, Flash is powered down and code executed from RAM after wake-up.

6) CPU is sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.

7) CPU is sleep, Flash is in active mode during sleep mode.

8) CPU is sleep, Flash is in power down mode during deep sleep mode.

3.3.2 Output Rise/Fall Times

Table 19 provides the characteristics of the output rise/fall times in the XMC1200. **Figure 11** describes the rise time and fall time parameters.

Table 19 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad[1)2)]	t_{HCPR}, t_{HCPF}	–	9	ns	50 pF @ 5 V[3)]
		–	12	ns	50 pF @ 3.3 V[4)]
		–	25	ns	50 pF @ 1.8 V[5)]
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	12	ns	50 pF @ 5 V[6)]
		–	15	ns	50 pF @ 3.3 V[7)].
		–	31	ns	50 pF @ 1.8 V[8)].

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
8) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

3.3.6 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 24 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

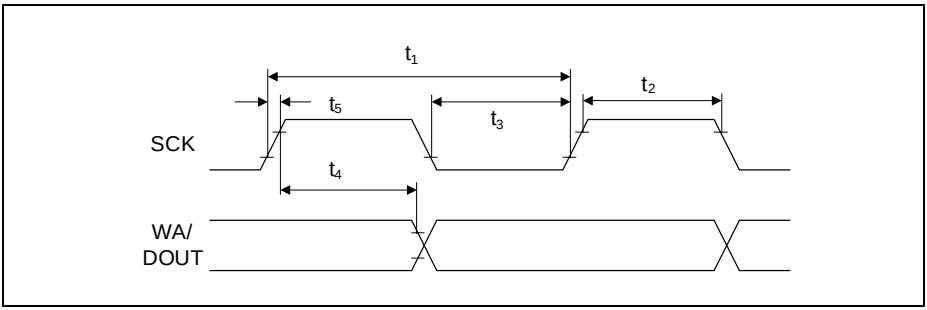

Figure 19 USIC IIS Master Transmitter Timing

Table 30 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t_8 SR	0.35 x t_{6min}	-	-	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

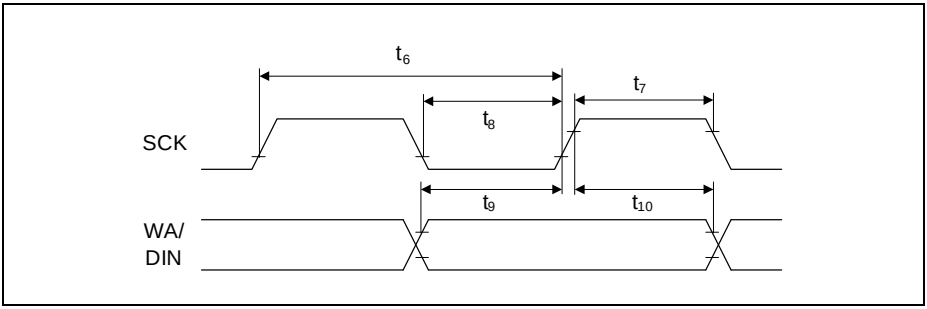

Figure 20 USIC IIS Slave Receiver Timing

4 Package and Reliability

The XMC1200 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 31 provides the thermal characteristics of the packages used in XMC1200.

Table 31 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8[1)]
		-	83.2	K/W	PG-TSSOP-28-16[1)]
		-	70.3	K/W	PG-TSSOP-38-9[1)]
		-	46.0	K/W	PG-VQFN-24-19[1)]
		-	38.4	K/W	PG-VQFN-40-13[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1200 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

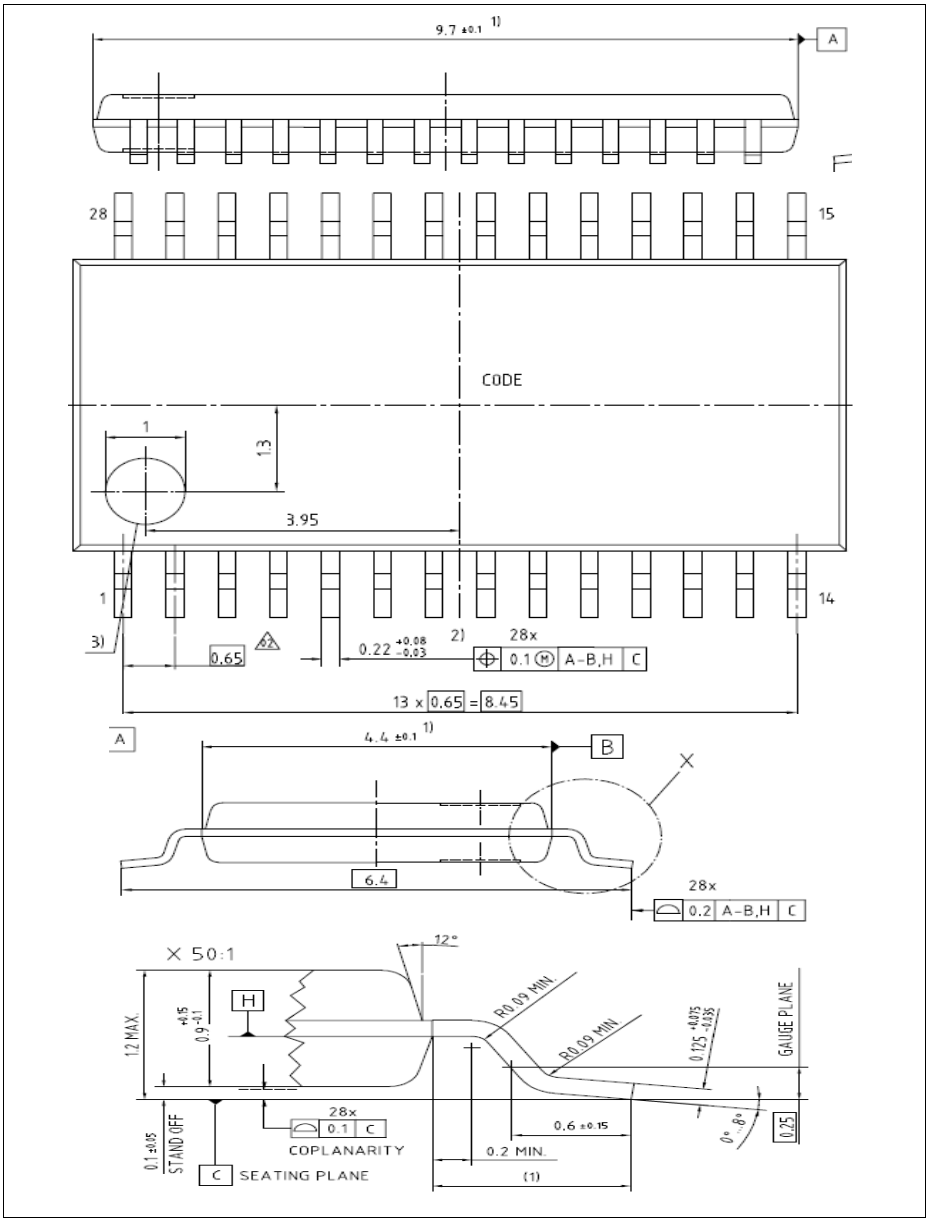

Figure 22 PG-TSSOP-28-16

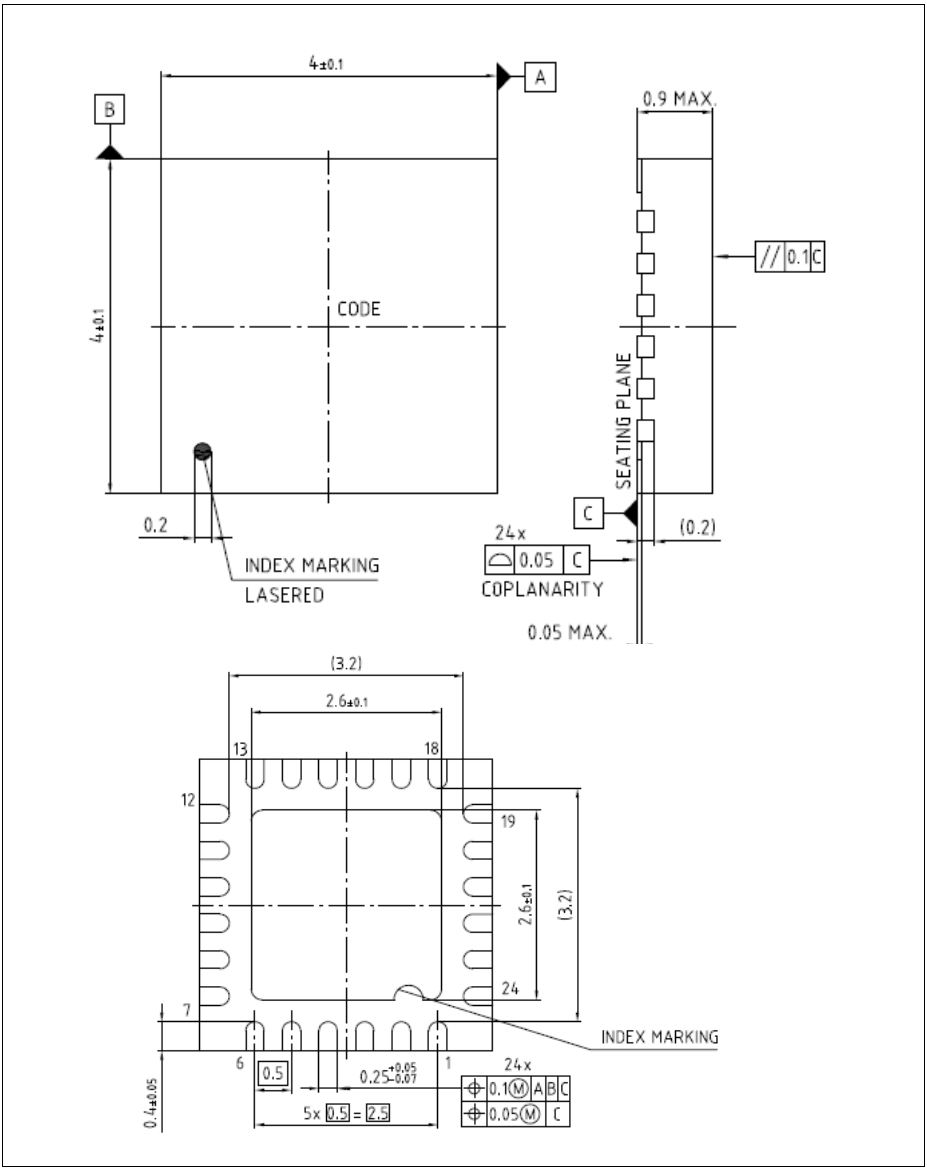

Figure 24 PG-VQFN-24-19

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