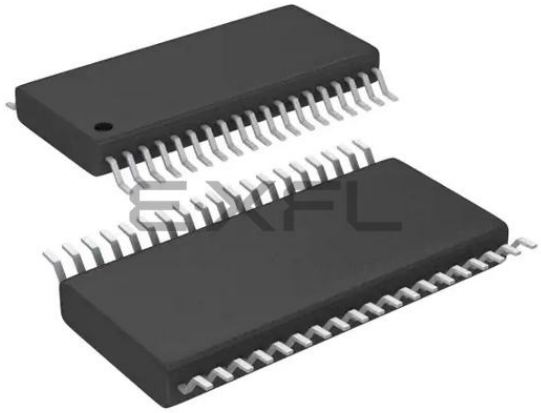
Infineon Technologies - XMC1201T038F0200AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	200KB (200K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1201t038f0200aaxuma1

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Table of Contents

1 Summary of Features

The XMC1200 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1200 series devices are optimized for LED Lighting and Human-Machine interface (HMI) applications.

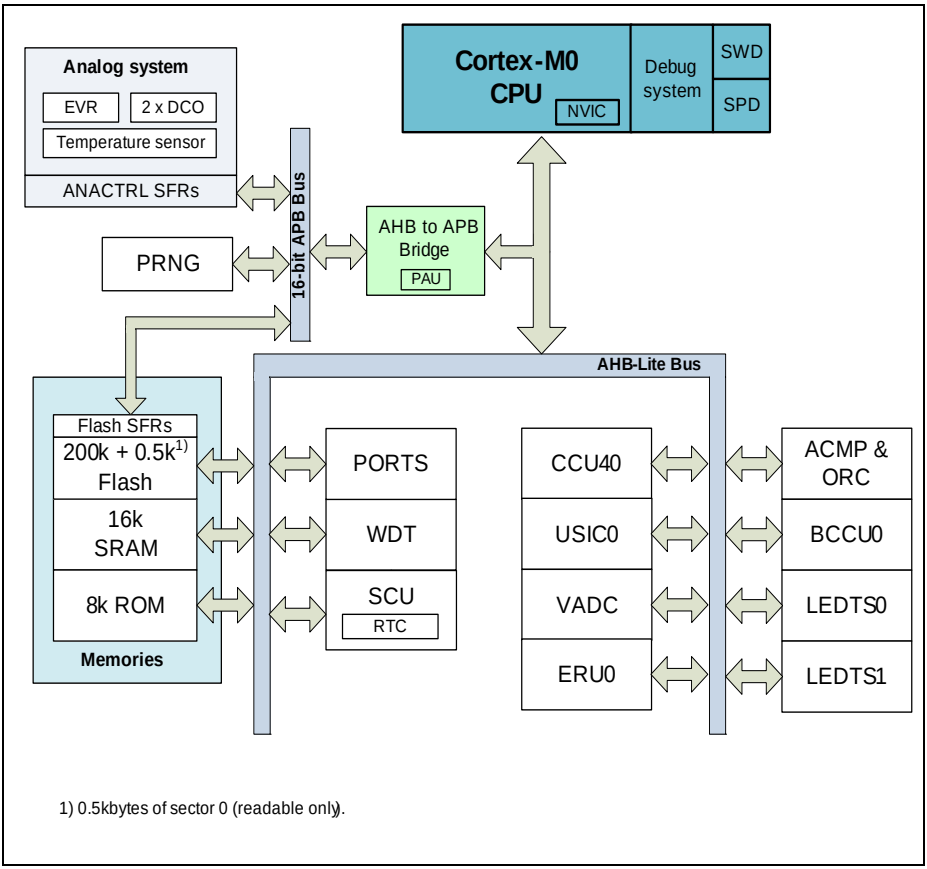

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M0 CPU
  - Most of 16-bit Thumb instruction set
  - Subset of 32-bit Thumb2 instruction set

  - High code density with 32-bit performance
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support
  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

Communication Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

Analog Frontend Peripherals

- A/D Converters, up to 12 channels, includes 2 sample and hold stages and a fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

Industrial Control Peripherals

- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

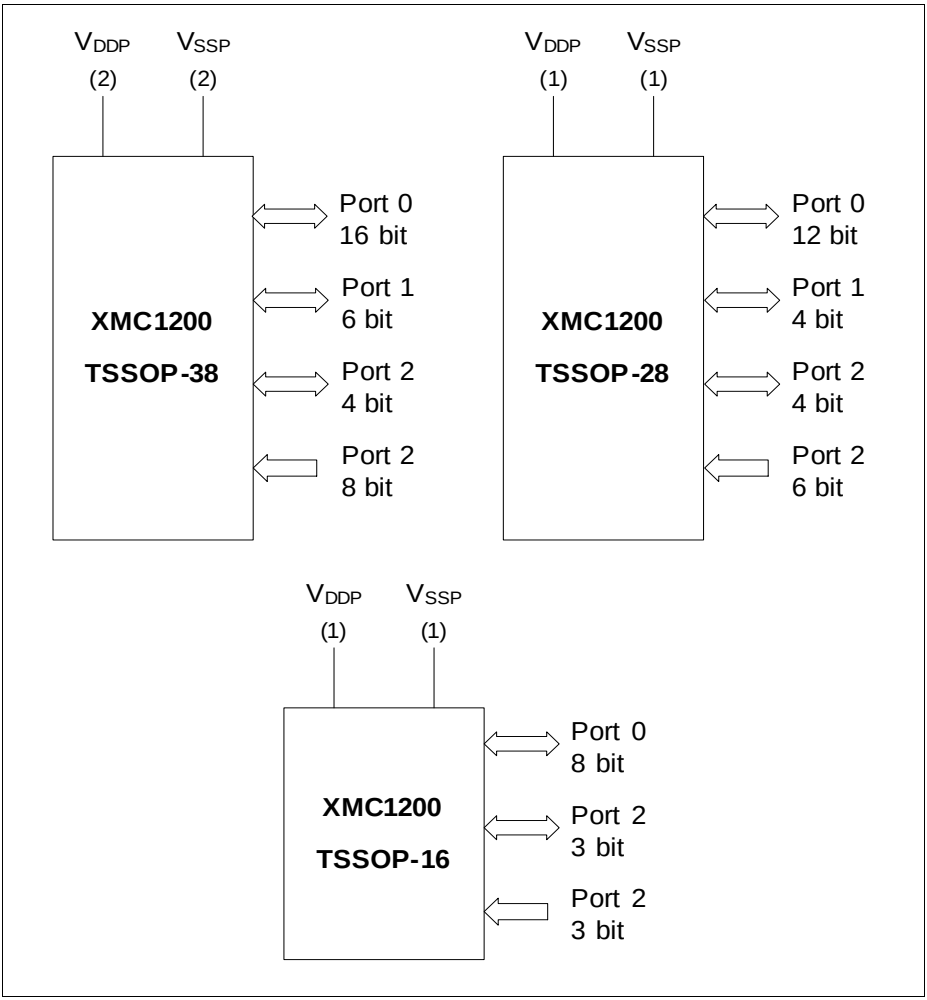

Figure 2 XMC1200 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16

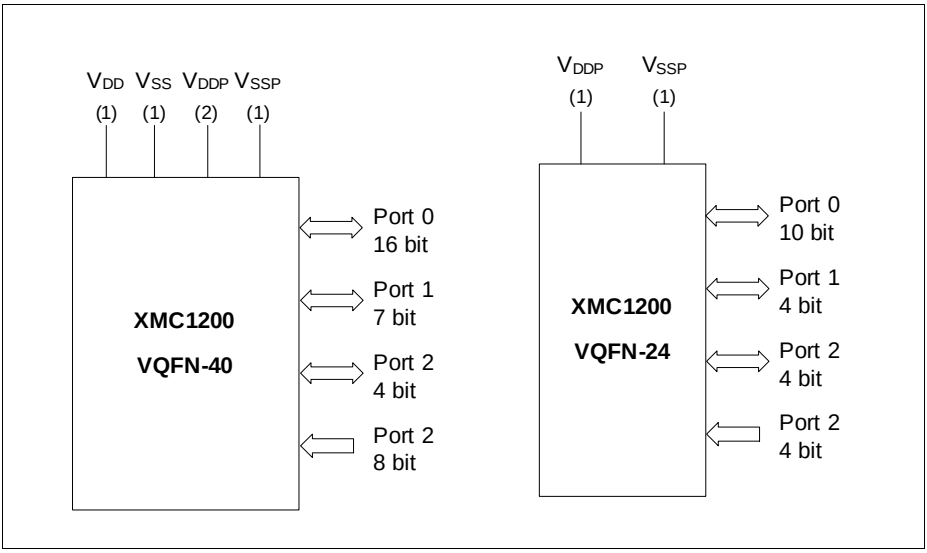

Figure 3 XMC1200 Logic Symbol for VQFN-24 and VQFN-40

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	13	15	7	STD_INOUT	
P0.1	24	18	-	-	-	STD_INOUT	
P0.2	25	19	-	-	-	STD_INOUT	
P0.3	26	20	-	-	-	STD_INOUT	
P0.4	27	21	14	-	-	STD_INOUT	
P0.5	28	22	15	16	8	STD_INOUT	
P0.6	29	23	16	17	9	STD_INOUT	
P0.7	30	24	17	18	10	STD_INOUT	
P0.8	33	27	18	19	11	STD_INOUT	
P0.9	34	28	19	20	12	STD_INOUT	
P0.10	35	29	20	-	-	STD_INOUT	
P0.11	36	30	-	-	-	STD_INOUT	
P0.12	37	31	21	21	-	STD_INOUT	

Table 8 Port I/O Functions

Function	Outputs									Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0. PDOUT0	LEDTS0. LINE7	ERU0. GOUT0	CCU40. OUT0		USIC0_CH0. SELO0	USIC0_CH1. SELO0	LEDTS0. EXTENDED7		LEDTS0. TSIN7	LEDTS0. TSIN7	BCCU0. TRAPINB	CCU40.IN0C			USIC0_CH0. DX2A	USIC0_CH1. DX2A		
P0.1	ERU0. PDOUT1	LEDTS0. LINE6	ERU0. GOUT1	CCU40. OUT1		BCCU0. OUT8	SCU. VDROP	LEDTS0. EXTENDED6		LEDTS0. TSIN6	LEDTS0. TSIN6		CCU40.IN1C						
P0.2	ERU0. PDOUT2	LEDTS0. LINE5	ERU0. GOUT2	CCU40. OUT2		VADC0. EMUX02		LEDTS0. EXTENDED5		LEDTS0. TSIN5	LEDTS0. TSIN5		CCU40.IN2C						
P0.3	ERU0. PDOUT3	LEDTS0. LINE4	ERU0. GOUT3	CCU40. OUT3		VADC0. EMUX01		LEDTS0. EXTENDED4		LEDTS0. TSIN4	LEDTS0. TSIN4		CCU40.IN3C						
P0.4	BCCU0. OUT0	LEDTS0. LINE3	LEDTS0. COL3	CCU40. OUT1		VADC0. EMUX00	WWDT. SERVICE_OUT	LEDTS0. EXTENDED3		LEDTS0. TSIN3	LEDTS0. TSIN3								
P0.5	BCCU0. OUT1	LEDTS0. LINE2	LEDTS0. COL2	CCU40. OUT0		ACMP2. OUT		LEDTS0. EXTENDED2		LEDTS0. TSIN2	LEDTS0. TSIN2								
P0.6	BCCU0. OUT2	LEDTS0. LINE1	LEDTS0. COL1	CCU40. OUT0		USIC0_CH1. MCLKOUT	USIC0_CH1. DOUT0	LEDTS0. EXTENDED1		LEDTS0. TSIN1	LEDTS0. TSIN1		CCU40.IN0B			USIC0_CH1. DX0C			
P0.7	BCCU0. OUT3	LEDTS0. LINE0	LEDTS0. COL0	CCU40. OUT1		USIC0_CH0. SCLKOUT	USIC0_CH1. DOUT0	LEDTS0. EXTENDED0		LEDTS0. TSIN0	LEDTS0. TSIN0		CCU40.IN1B			USIC0_CH0. DX1C	USIC0_CH1. DX0D	USIC0_CH1. DX1C	
P0.8	BCCU0. OUT4	LEDTS1. LINE0	LEDTS0. COLA	CCU40. OUT2		USIC0_CH0. SCLKOUT	USIC0_CH1. SCLKOUT	LEDTS1. EXTENDED0		LEDTS1. TSIN0	LEDTS1. TSIN0		CCU40.IN2B			USIC0_CH0. DX1B	USIC0_CH1. DX1B		
P0.9	BCCU0. OUT5	LEDTS1. LINE1	LEDTS0. COL6	CCU40. OUT3		USIC0_CH0. SELO0	USIC0_CH1. SELO0	LEDTS1. EXTENDED1		LEDTS1. TSIN1	LEDTS1. TSIN1		CCU40.IN3B			USIC0_CH0. DX2B	USIC0_CH1. DX2B		
P0.10	BCCU0. OUT6	LEDTS1. LINE2	LEDTS0. COL5	ACMP0. OUT		USIC0_CH0. SELO1	USIC0_CH1. SELO1	LEDTS1. EXTENDED2		LEDTS1. TSIN2	LEDTS1. TSIN2					USIC0_CH0. DX2C	USIC0_CH1. DX2C		
P0.11	BCCU0. OUT7	LEDTS1. LINE3	LEDTS0. COL4	USIC0_CH0. MCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO2	LEDTS1. EXTENDED3		LEDTS1. TSIN3	LEDTS1. TSIN3					USIC0_CH0. DX2D	USIC0_CH1. DX2D		
P0.12	BCCU0. OUT6	LEDTS1. LINE4	LEDTS0. COL3	LEDTS1. COL3		USIC0_CH0. SELO3		LEDTS1. EXTENDED4		LEDTS1. TSIN4	LEDTS1. TSIN4	BCCU0. TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0. DX2E		
P0.13	WWDT. SERVICE_OUT	LEDTS1. LINE5	LEDTS0. COL2	LEDTS1. COL2		USIC0_CH0. SELO4		LEDTS1. EXTENDED5		LEDTS1. TSIN5	LEDTS1. TSIN5					USIC0_CH0. DX2F			
P0.14	BCCU0. OUT7	LEDTS1. LINE6	LEDTS0. COL1	LEDTS1. COL1		USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT	LEDTS1. EXTENDED6		LEDTS1. TSIN6	LEDTS1. TSIN6					USIC0_CH0. DX0A	USIC0_CH0. DX1A		
P0.15	BCCU0. OUT8	LEDTS1. LINE7	LEDTS0. COL0	LEDTS1. COL0		USIC0_CH0. DOUT0	USIC0_CH1. MCLKOUT	LEDTS1. EXTENDED7		LEDTS1. TSIN7	LEDTS1. TSIN7					USIC0_CH0. DX0B			
P1.0	BCCU0. OUT0	CCU40. OUT0	LEDTS0. COL0	LEDTS1. COLA		ACMP1. OUT	USIC0_CH0. DOUT0		USIC0_CH0. DOUT0		USIC0_CH0. HWIN0					USIC0_CH0. DX0C			
P1.1	VADC0. EMUX00	CCU40. OUT1	LEDTS0. COL1	LEDTS1. COL0		USIC0_CH0. DOUT0	USIC0_CH1. SELO0		USIC0_CH0. DOUT1		USIC0_CH0. HWIN1					USIC0_CH0. DX0D	USIC0_CH0. DX1D	USIC0_CH1. DX2E	
P1.2	VADC0. EMUX01	CCU40. OUT2	LEDTS0. COL2	LEDTS1. COL1		ACMP2. OUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT2		USIC0_CH0. HWIN2					USIC0_CH1. DX0B			
P1.3	VADC0. EMUX02	CCU40. OUT3	LEDTS0. COL3	LEDTS1. COL2		USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT3		USIC0_CH0. HWIN3					USIC0_CH1. DX0A	USIC0_CH1. DX1A		
P1.4	VADC0. EMUX10	USIC0_CH1. SCLKOUT	LEDTS0. COL4	LEDTS1. COL3		USIC0_CH0. SELO0	USIC0_CH1. SELO1									USIC0_CH0. DX5E	USIC0_CH1. DX5E		
P1.5	VADC0. EMUX11	USIC0_CH0. DOUT0	LEDTS0. COLA	BCCU0. OUT1		USIC0_CH0. SELO1	USIC0_CH1. SELO2									USIC0_CH1. DX5F			

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1200.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1200 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1200 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1200 is designed in.

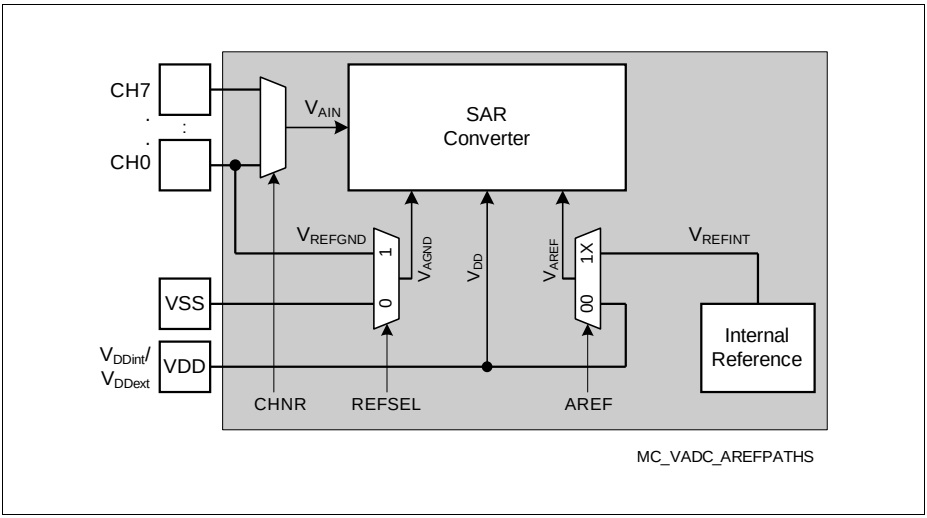

Figure 9 ADC Voltage Supply

Table 17 provides the active current consumption of some modules operating at 5 V power supply at 25 °C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 17 Typical Active Current Consumption[1)]

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP[2)]
VADC and SHS	I_{ADCDDC}	3.4	mA	Set CGATCLR0.VADC to 1[3)]
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1[4)]
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1[5)]
LEDTSx	$I_{LTSxDDC}$	0.76	mA	Set CGATCLR0.LEDTSx to 1[6)]
BCCU0	$I_{BCCU0DDC}$	0.24	mA	Set CGATCLR0.BCCU0 to 1[7)]
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1[8)]
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1[9)]

1) Not subject to production test, verified by design/characterisation.

2) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.

3) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode

4) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms

5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle

6) Active current is measured with: module enabled, MCLK=32 MHz, 1 LED column, 6 LED/TS lines, Pad Scheme A with large pad hysteresis config, time slice duration = 1.048 ms

7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s

8) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s

9) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

3.3.2 Output Rise/Fall Times

Table 19 provides the characteristics of the output rise/fall times in the XMC1200. **Figure 11** describes the rise time and fall time parameters.

Table 19 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad[1)2)]	t_{HCPR}, t_{HCPF}	–	9	ns	50 pF @ 5 V[3)]
		–	12	ns	50 pF @ 3.3 V[4)]
		–	25	ns	50 pF @ 1.8 V[5)]
Rise/fall times on Standard Pad[1)2)]	t_R, t_F	–	12	ns	50 pF @ 5 V[6)]
		–	15	ns	50 pF @ 3.3 V[7)].
		–	31	ns	50 pF @ 1.8 V[8)].

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
3) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
4) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
5) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
6) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
7) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
8) Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

3.3.3 Power-Up and Supply Threshold Charcteristics

Table 20 provides the characteristics of the supply threshold in XMC1200.

Table 20 Power-Up and Supply Threshold Parameters (Operating Conditions apply) [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ [2)] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[3)]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_ SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_ SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_ SELECT = 10_B
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
Start-up time from power-on reset	t_{SSW} SR	–	320	–	µs	Time to the first user code instruction[4)]

1) Not all parameters are 100% tested, but are verified by design/characterisation.

2) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	

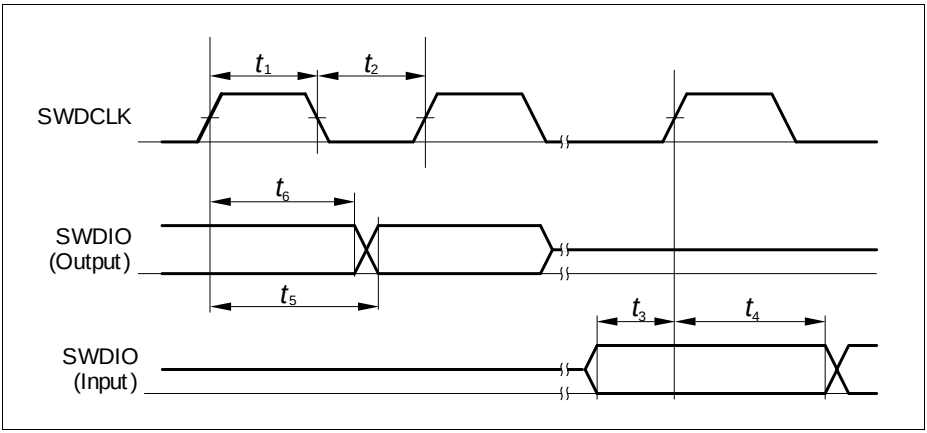

Figure 16 SWD Timing

Table 26 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 28 USIC IIC Fast Mode Timing [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

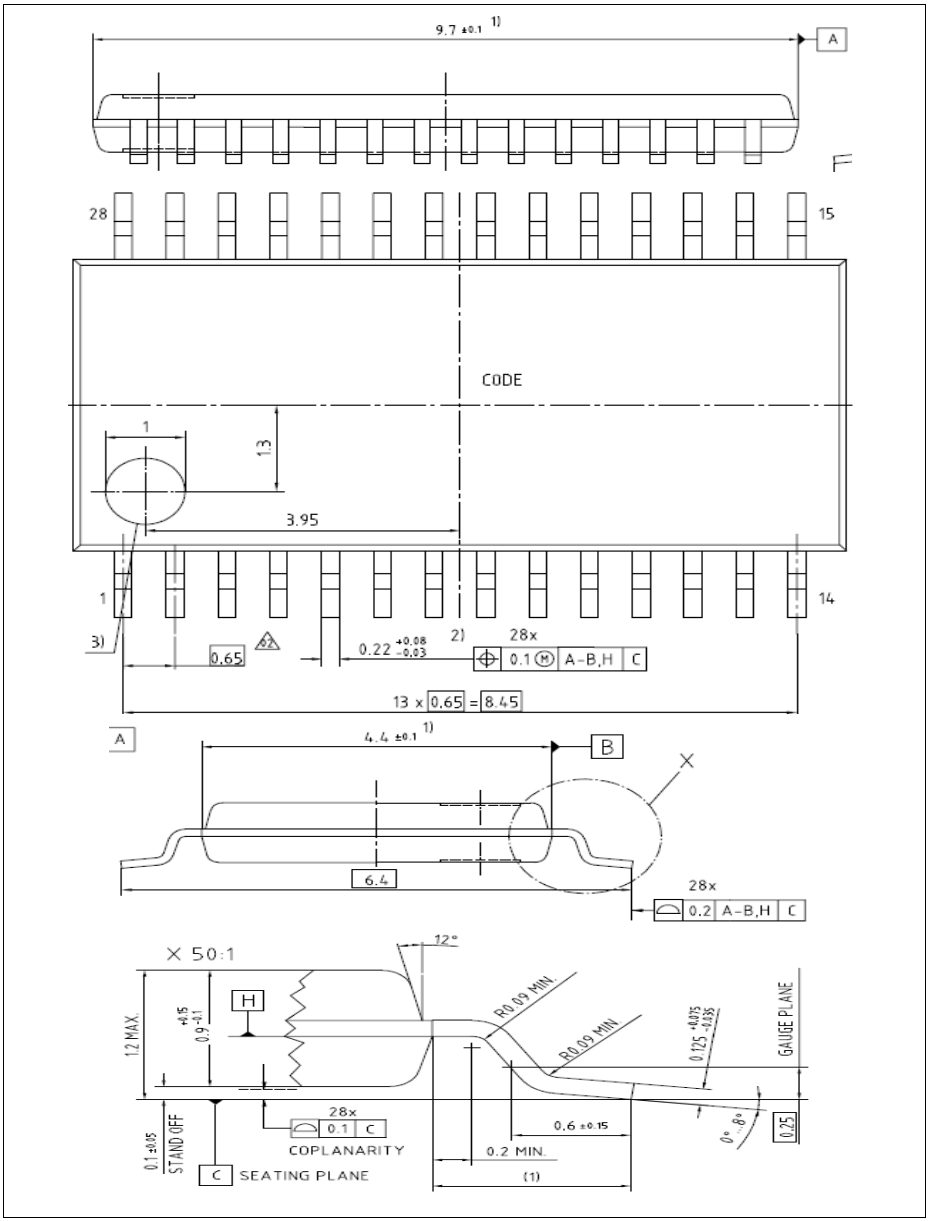

Figure 22 PG-TSSOP-28-16

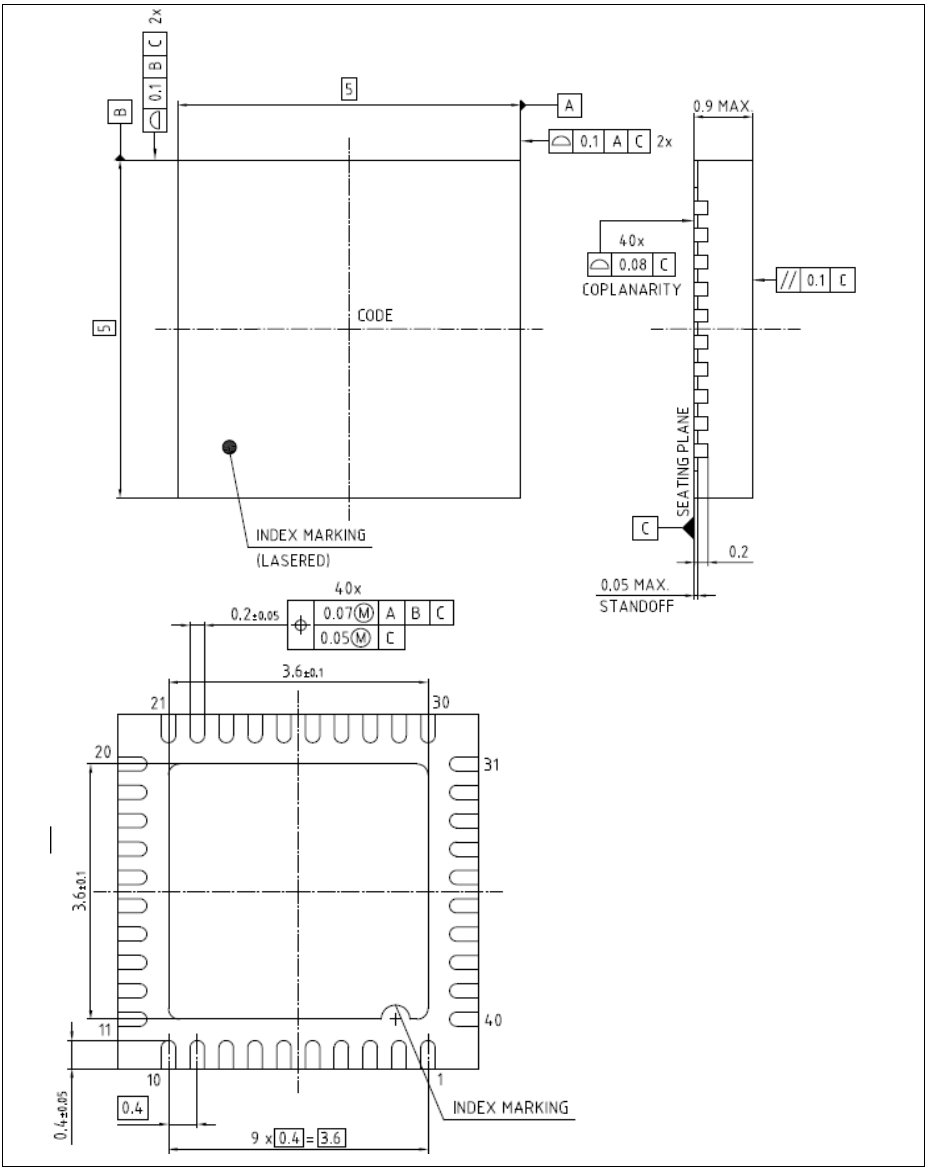

Figure 25 PG-VQFN-40-13

All dimensions in mm.

5 Quality Declaration

Table 32 shows the characteristics of the quality parameters in the XMC1200.

Table 32 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020C