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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1202q024x0016abxuma1

Edition 2014-05

Published by
Infineon Technologies AG
81726 Munich, Germany

XMC1200

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex™-M0
32-bit processor core

Data Sheet

V1.4 2014-05

Microcontrollers

Table of Contents

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

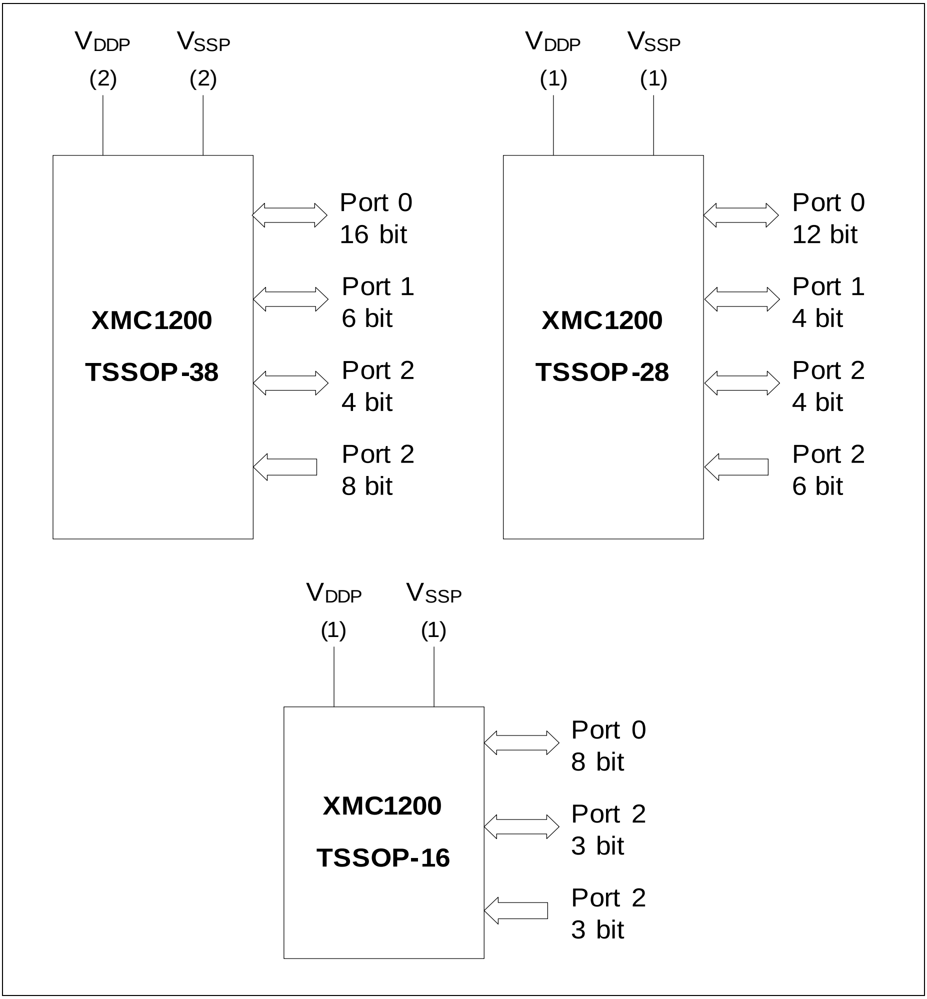

Figure 2 XMC1200 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16

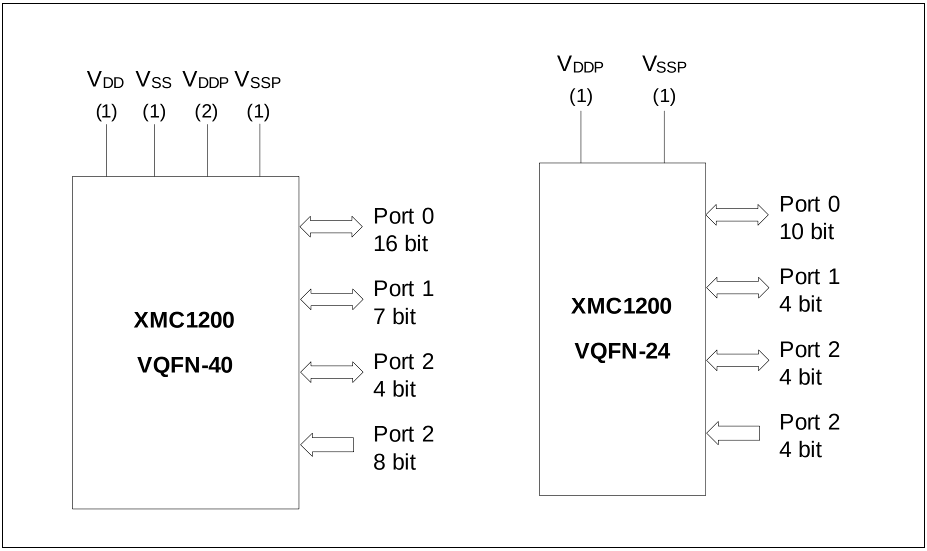

Figure 3 XMC1200 Logic Symbol for VQFN-24 and VQFN-40

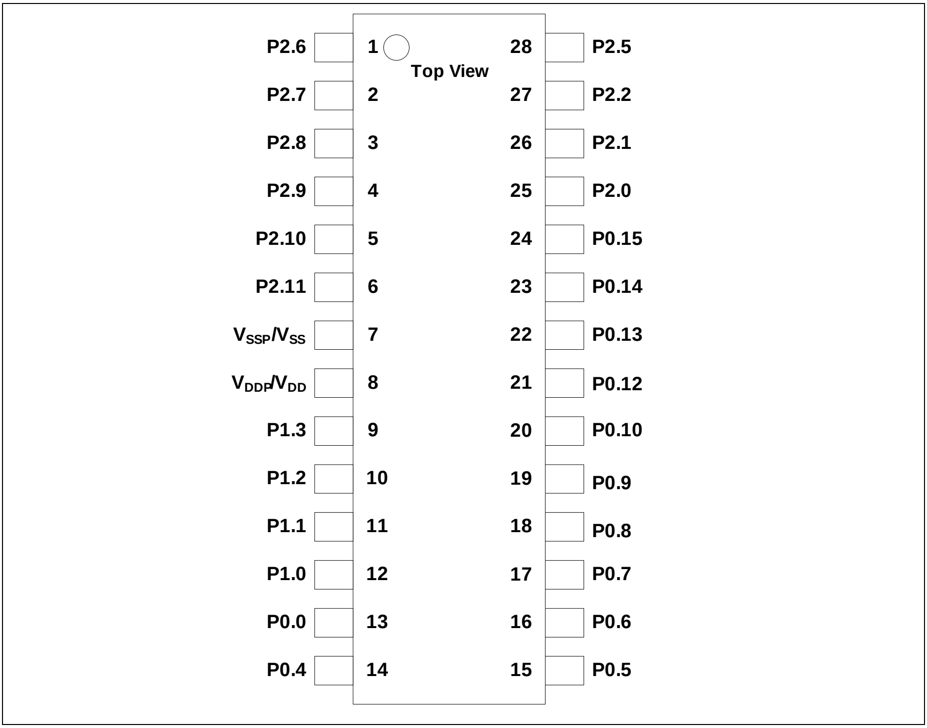

Figure 5 XMC1200 PG-TSSOP-28 Pin Configuration (top view)

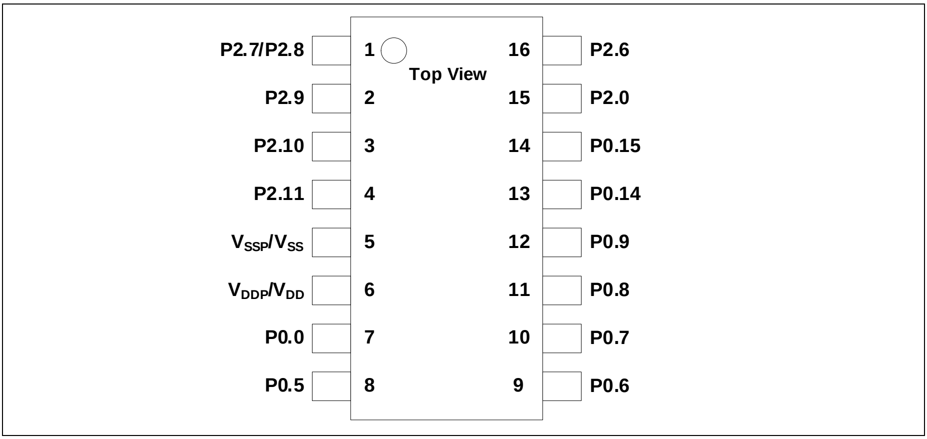

Figure 6 XMC1200 PG-TSSOP-16 Pin Configuration (top view)

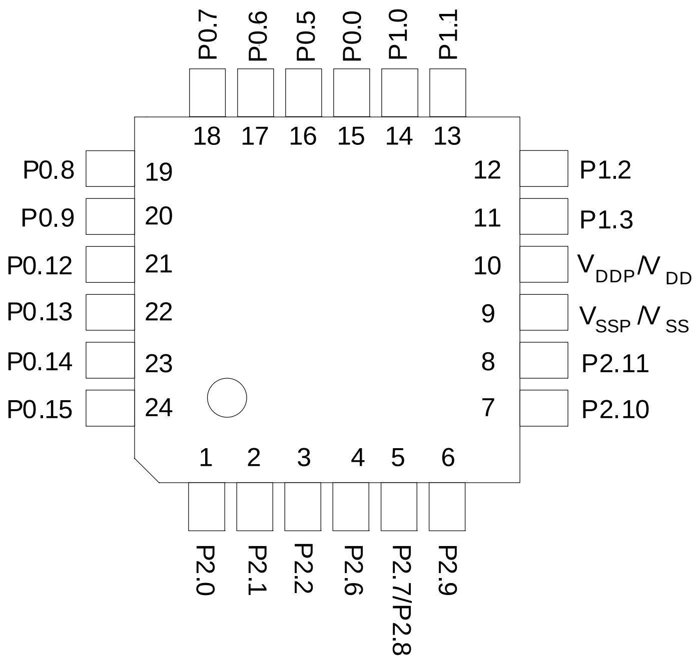

Figure 7 XMC1200 PG-VQFN-24 Pin Configuration (top view)

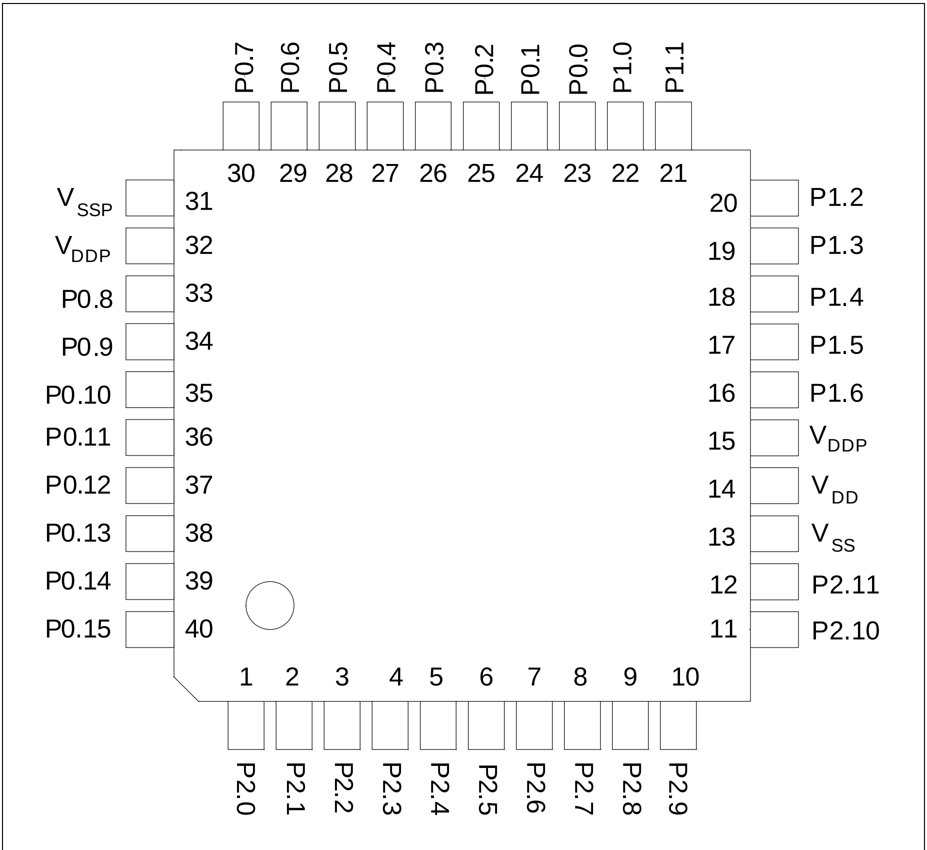

Figure 8 XMC1200 PG-VQFN-40 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the "Function" column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The "Pad Type" indicates the employed pad type:

- STD_INOUT (standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	13	15	7	STD_INOUT	
P0.1	24	18	-	-	-	STD_INOUT	
P0.2	25	19	-	-	-	STD_INOUT	
P0.3	26	20	-	-	-	STD_INOUT	
P0.4	27	21	14	-	-	STD_INOUT	
P0.5	28	22	15	16	8	STD_INOUT	
P0.6	29	23	16	17	9	STD_INOUT	
P0.7	30	24	17	18	10	STD_INOUT	
P0.8	33	27	18	19	11	STD_INOUT	
P0.9	34	28	19	20	12	STD_INOUT	
P0.10	35	29	20	-	-	STD_INOUT	
P0.11	36	30	-	-	-	STD_INOUT	
P0.12	37	31	21	21	-	STD_INOUT	

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.13	38	32	22	22	-	STD_INOUT	
P0.14	39	33	23	23	13	STD_INOUT	
P0.15	40	34	24	24	14	STD_INOUT	
P1.0	22	16	12	14	-	High Current	
P1.1	21	15	11	13	-	High Current	
P1.2	20	14	10	12	-	High Current	
P1.3	19	13	9	11	-	High Current	
P1.4	18	12	-	-	-	High Current	
P1.5	17	11	-	-	-	High Current	
P1.6	16	-	-	-	-	STD_INOUT	
P2.0	1	35	25	1	15	STD_INOUT /AN	
P2.1	2	36	26	2	-	STD_INOUT /AN	
P2.2	3	37	27	3	-	STD_IN/AN	
P2.3	4	38	-	-	-	STD_IN/AN	
P2.4	5	1	-	-	-	STD_IN/AN	
P2.5	6	2	28	-	-	STD_IN/AN	
P2.6	7	3	1	4	16	STD_IN/AN	
P2.7	8	4	2	5	1	STD_IN/AN	
P2.8	9	5	3	5	1	STD_IN/AN	
P2.9	10	6	4	6	2	STD_IN/AN	
P2.10	11	7	5	7	3	STD_INOUT /AN	
P2.11	12	8	6	8	4	STD_INOUT /AN	
VSS	13	9	7	9	5	Power	Supply GND, ADC reference GND

Table 8 Port I/O Functions (cont'd)

Function	Outputs									Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P1.6	VADC0. EMUX12	USIC0_CH1. DOUT0	LEDTS0. COL5	USIC0_CH0. SCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO3							USIC0_CH0. DX5F					
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3	LEDTS1. COL5		USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT						VADC0. G0CH5		ERU0.0B0	USIC0_CH0. DX0E	USIC0_CH0. DX1E	USIC0_CH1. DX2F	
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2	LEDTS1. COL6		USIC0_CH0. DOUT0	USIC0_CH1. SCLKOUT					ACMP2.INP	VADC0. G0CH6		ERU0.1B0	USIC0_CH0. DX0F	USIC0_CH1. DX3A	USIC0_CH1. DX4A	
P2.2												ACMP2.INN	VADC0. G0CH7		ERU0.0B1	USIC0_CH0. DX3A	USIC0_CH0. DX4A	USIC0_CH1. DX5A	ORC0.AIN
P2.3													VADC0. G1CH5		ERU0.1B1	USIC0_CH0. DX5B	USIC0_CH1. DX3C	USIC0_CH1. DX4C	ORC1.AIN
P2.4													VADC0. G1CH6		ERU0.0A1	USIC0_CH0. DX3B	USIC0_CH0. DX4B	USIC0_CH1. DX5B	ORC2.AIN
P2.5													VADC0. G1CH7		ERU0.1A1	USIC0_CH0. DX5D	USIC0_CH1. DX3E	USIC0_CH1. DX4E	ORC3.AIN
P2.6												ACMP1.INN	VADC0. G0CH0		ERU0.2A1	USIC0_CH0. DX3E	USIC0_CH0. DX4E	USIC0_CH1. DX5D	ORC4.AIN
P2.7												ACMP1.INP	VADC0. G1CH1		ERU0.3A1	USIC0_CH0. DX5C	USIC0_CH1. DX3D	USIC0_CH1. DX4D	ORC5.AIN
P2.8												ACMP0.INN	VADC0. G0CH1	VADC0. G1CH0	ERU0.3B1	USIC0_CH0. DX3D	USIC0_CH0. DX4D	USIC0_CH1. DX5C	ORC6.AIN
P2.9												ACMP0.INP	VADC0. G0CH2	VADC0. G1CH4	ERU0.3B0	USIC0_CH0. DX5A	USIC0_CH1. DX3B	USIC0_CH1. DX4B	ORC7.AIN
P2.10	ERU0. PDOUT1	CCU40. OUT2	ERU0. GOUT1	LEDTS1. COL4		ACMP0. OUT	USIC0_CH1. DOUT0						VADC0. G0CH3	VADC0. G1CH2	ERU0.2B0	USIC0_CH0. DX3C	USIC0_CH0. DX4C	USIC0_CH1. DX0F	
P2.11	ERU0. PDOUT0	CCU40. OUT3	ERU0. GOUT0	LEDTS1. COL3		USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0					ACMP.REF	VADC0. G0CH4	VADC0. G1CH3	ERU0.2B1	USIC0_CH1. DX0E	USIC0_CH1. DX1E		

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_S	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on any pin with respect to V_{SSP}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on any analog input pin with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	–
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	SR	–	–	50	mA	–
Analog comparator input voltage	V_{CM}	SR	-0.3	–	V_{DDP} + 0.3	V	

Table 12 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC		1		–	GNCTRxz.GAINy = 00_B (unity gain)
			3		–	GNCTRxz.GAINy = 01_B (gain g1)
			6		–	GNCTRxz.GAINy = 10_B (gain g2)
			12		–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	V_{DDP} = 5.0 V
		3	–	–	1 / f_{ADC}	V_{DDP} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DDP} = 1.8 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC		9		1 / f_{ADC}	2)
Conversion time in 12-bit mode	t_{C12} CC		20		1 / f_{ADC}	2)
Maximum sample rate in 12-bit mode 3)	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC		18		1 / f_{ADC}	2)
Maximum sample rate in 10-bit mode 3)	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC		16		1 / f_{ADC}	2)

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 13 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; V_{DDP} = 3.0 V - 5.5 V)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	60	–	120	mV	$V_{AIN} \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	25	–	V_{ODC}	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			88	–	–	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			–	–	11	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Detection Delay	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			31	–	121	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

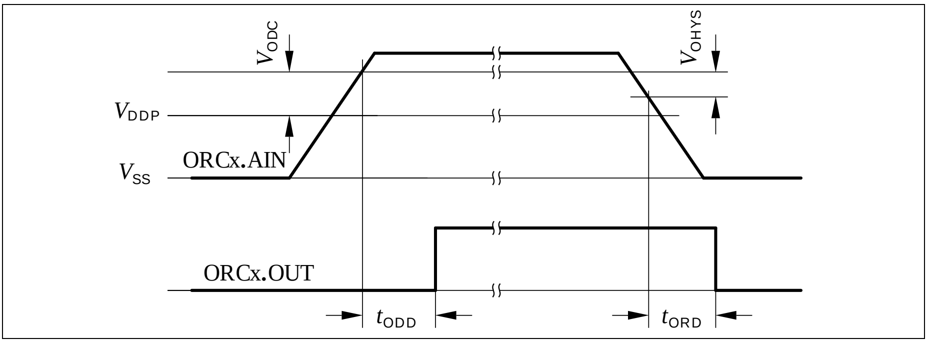

Figure 10 ORCx.OUT Trigger Generation

Table 17 provides the active current consumption of some modules operating at 5 V power supply at 25 °C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 17 Typical Active Current Consumption[1)]

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP[2)]
VADC and SHS	I_{ADCDDC}	3.4	mA	Set CGATCLR0.VADC to 1[3)]
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1[4)]
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1[5)]
LEDTSx	$I_{LTSxDDC}$	0.76	mA	Set CGATCLR0.LEDTSx to 1[6)]
BCCU0	$I_{BCCU0DDC}$	0.24	mA	Set CGATCLR0.BCCU0 to 1[7)]
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1[8)]
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1[9)]

1) Not subject to production test, verified by design/characterisation.
2) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.
3) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode
4) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms
5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle
6) Active current is measured with: module enabled, MCLK=32 MHz, 1 LED column, 6 LED/TS lines, Pad Scheme A with large pad hysteresis config, time slice duration = 1.048 ms
7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s
8) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s
9) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

Figure 15 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

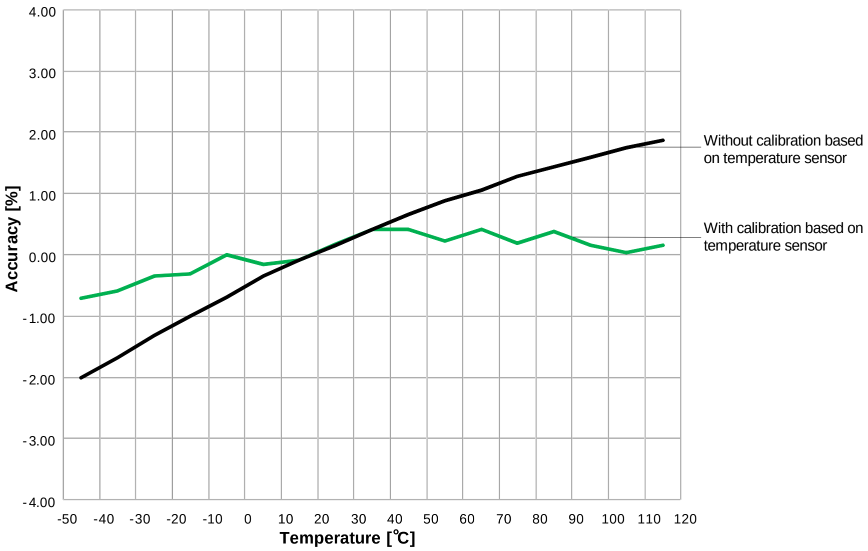

Figure 15 Typical DCO1 accuracy over temperature

Table 22 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1200.

Table 22 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	32.5	32.75	33	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)[2]
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)[2]

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) Not subject to production test, verified by design/characterisation.

4 Package and Reliability

The XMC1200 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 31 provides the thermal characteristics of the packages used in XMC1200.

Table 31 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8[1)]
		-	83.2	K/W	PG-TSSOP-28-16[1)]
		-	70.3	K/W	PG-TSSOP-38-9[1)]
		-	46.0	K/W	PG-VQFN-24-19[1)]
		-	38.4	K/W	PG-VQFN-40-13[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1200 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$" quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

4.2 Package Outlines

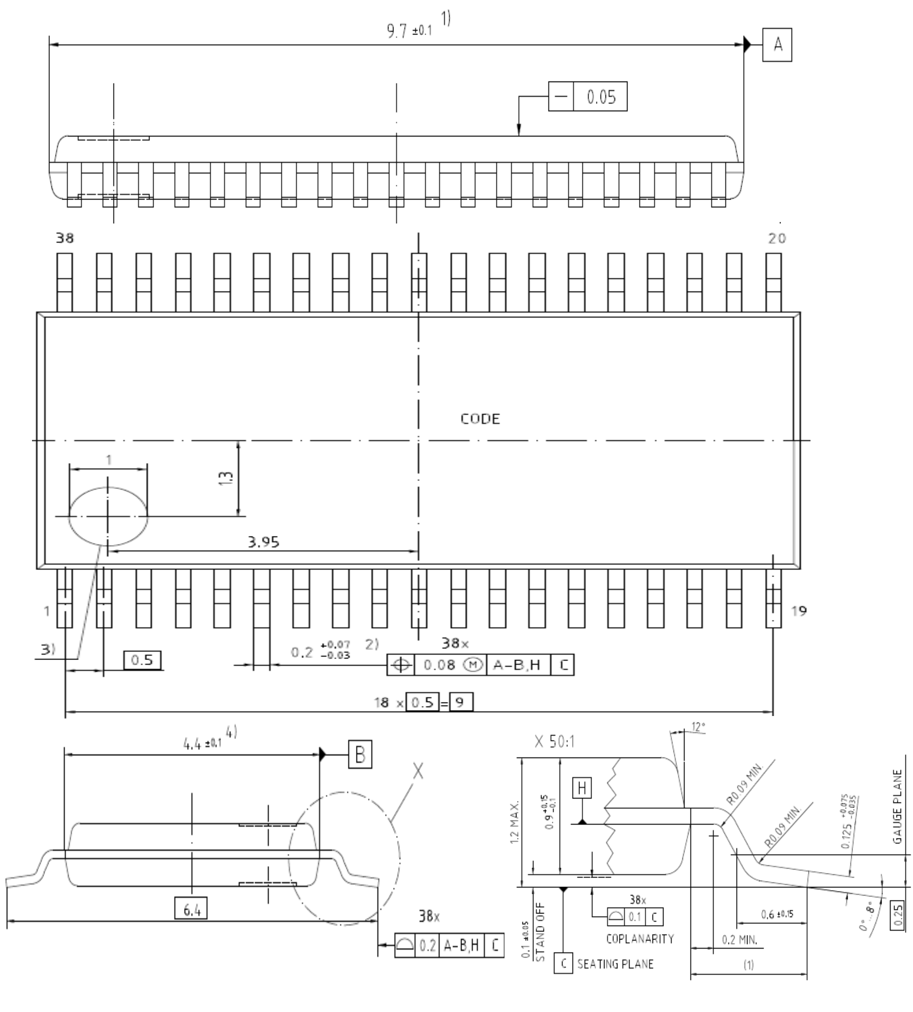

Figure 21 PG-TSSOP-38-9

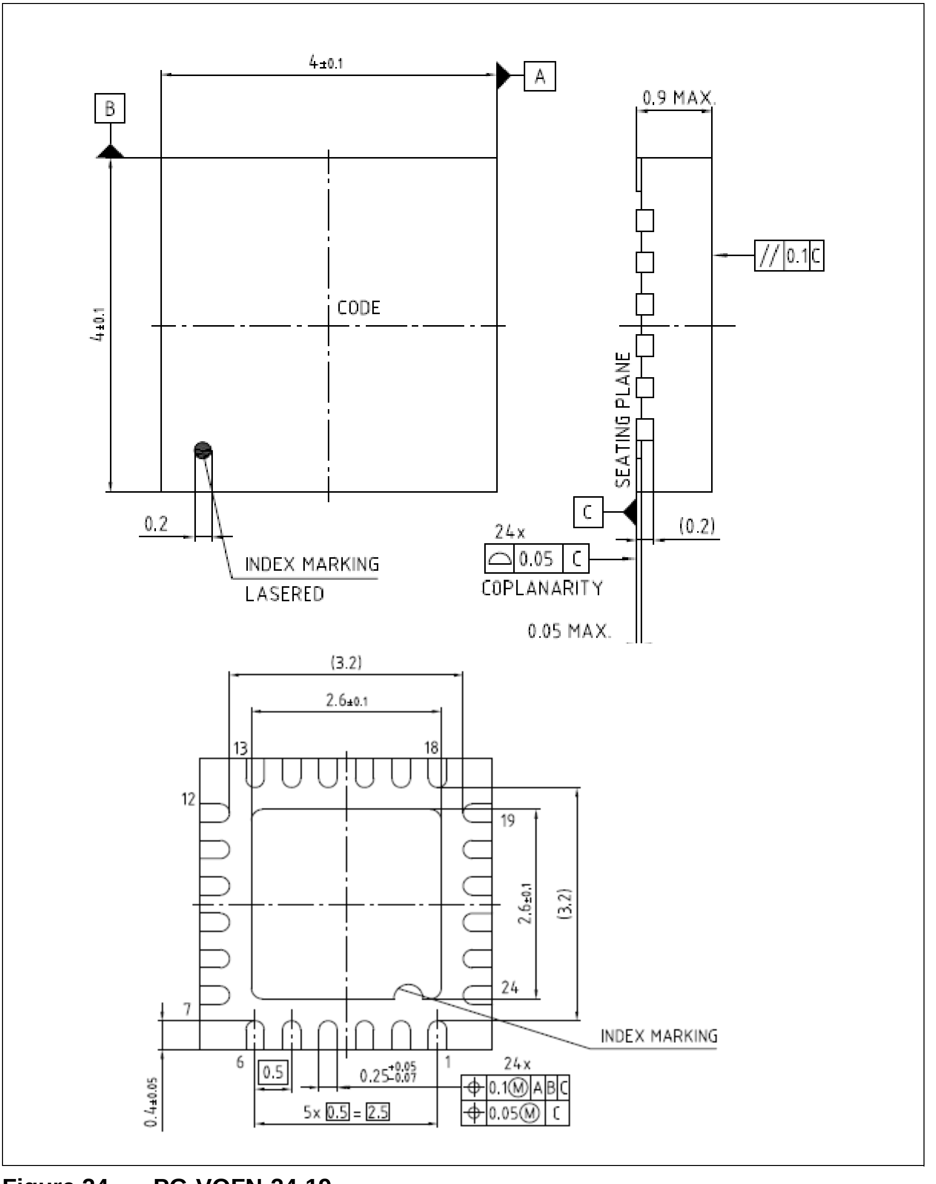

Figure 24 PG-VQFN-24-19

5 Quality Declaration

Table 32 shows the characteristics of the quality parameters in the XMC1200.

Table 32 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	*MSL* CC	-	3	-	JEDEC J-STD-020C