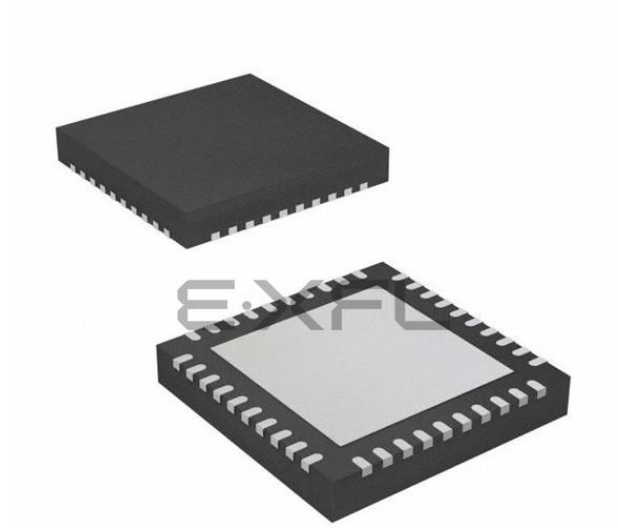
# Infineon Technologies - XMC1202Q040X0016ABXUMA1 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 40-VFQFN Exposed Pad |
| Supplier Device Package | PG-VQFN-40-13 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1202q040x0016abxuma1 |

5 Quality Declaration . . . . . 64

# About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1200 series devices.

The document describes the characteristics of a superset of the XMC1200 series devices. For simplicity, the various device types are referred to by the collective term XMC1200 throughout this document.

### XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

***Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.***

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

**Table 1 Synopsis of XMC1200 Device Types (cont'd)**

| Derivative | Package | Flash Kbytes | SRAM Kbytes |
|---|---|---|---|
| XMC1200-T038F0200 | PG-TSSOP-38-9 | 200 | 16 |
| XMC1202-T028X0016 | PG-TSSOP-28-16 | 16 | 16 |
| XMC1202-T028X0032 | PG-TSSOP-28-16 | 32 | 16 |
| XMC1202-T016X0016 | PG-TSSOP-16-8 | 16 | 16 |
| XMC1202-T016X0032 | PG-TSSOP-16-8 | 32 | 16 |
| XMC1202-Q024X0016 | PG-VQFN-24-19 | 16 | 16 |
| XMC1202-Q024X0032 | PG-VQFN-24-19 | 32 | 16 |
| XMC1201-Q040F0016 | PG-VQFN-40-13 | 16 | 16 |
| XMC1201-Q040F0032 | PG-VQFN-40-13 | 32 | 16 |
| XMC1201-Q040F0064 | PG-VQFN-40-13 | 64 | 16 |
| XMC1201-Q040F0128 | PG-VQFN-40-13 | 128 | 16 |
| XMC1201-Q040F0200 | PG-VQFN-40-13 | 200 | 16 |
| XMC1202-Q040X0016 | PG-VQFN-40-13 | 16 | 16 |
| XMC1202-Q040X0032 | PG-VQFN-40-13 | 32 | 16 |

## 1.3 Device Type Features

The following table lists the available features per device type.

**Table 2 Features of XMC1200 Device Types[1)]**

| Derivative | ADC channel | ACMP | BCCU | LEDTS |
|---|---|---|---|---|
| XMC1200-T038 | 16 | 3 | 1 | 2 |
| XMC1201-T038 | 16 | - | - | 2 |
| XMC1202-T028 | 14 | 3 | 1 | - |
| XMC1202-T016 | 11 | 2 | 1 | - |
| XMC1202-Q024 | 13 | 3 | 1 | - |
| XMC1201-Q040 | 16 | - | - | 2 |
| XMC1202-Q040 | 16 | 3 | 1 | - |

1) Features that are not included in this table are available in all the derivatives

# 2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

## 2.1 Logic Symbols

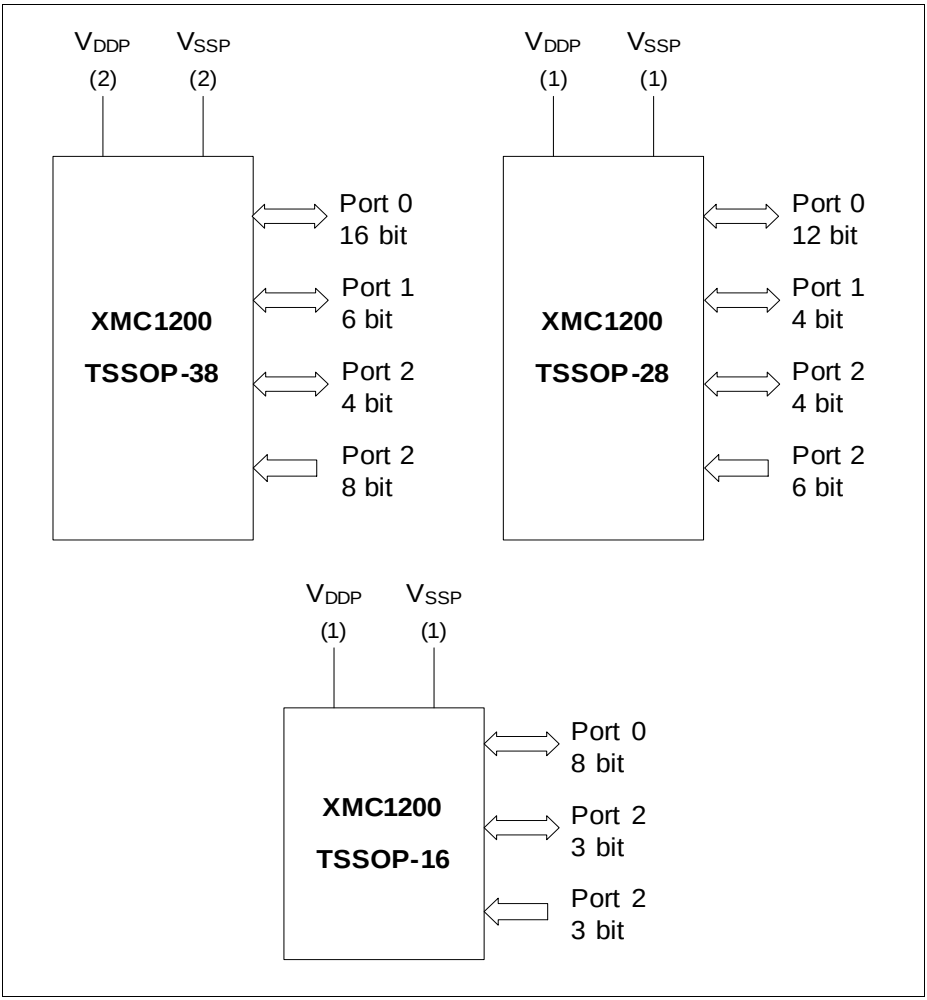


**Figure 2 XMC1200 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16**

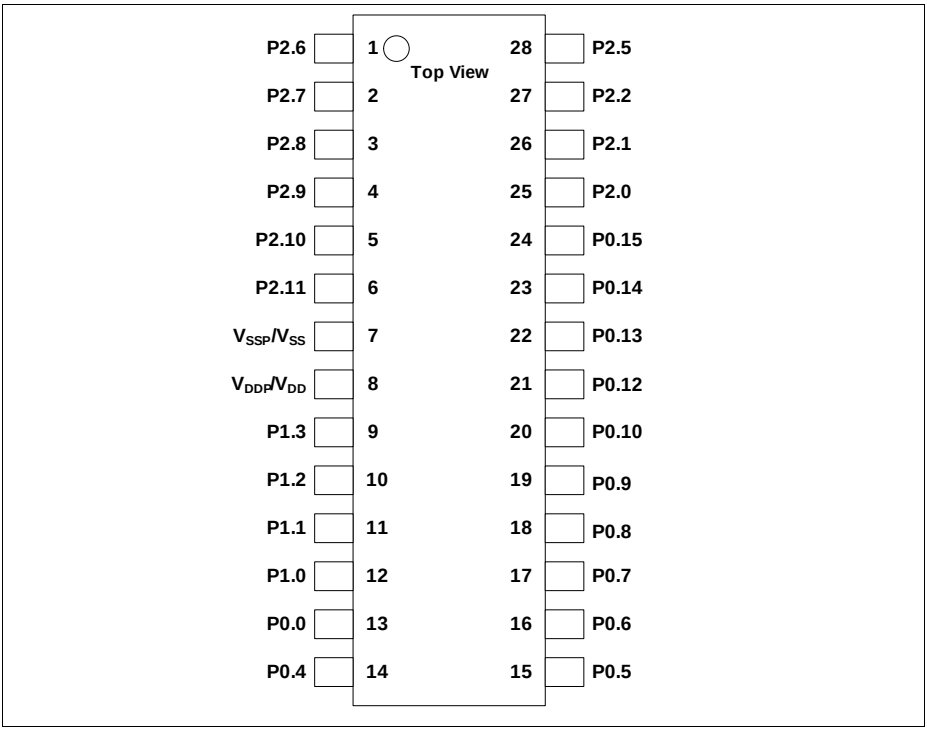


**Figure 5 XMC1200 PG-TSSOP-28 Pin Configuration** (top view)

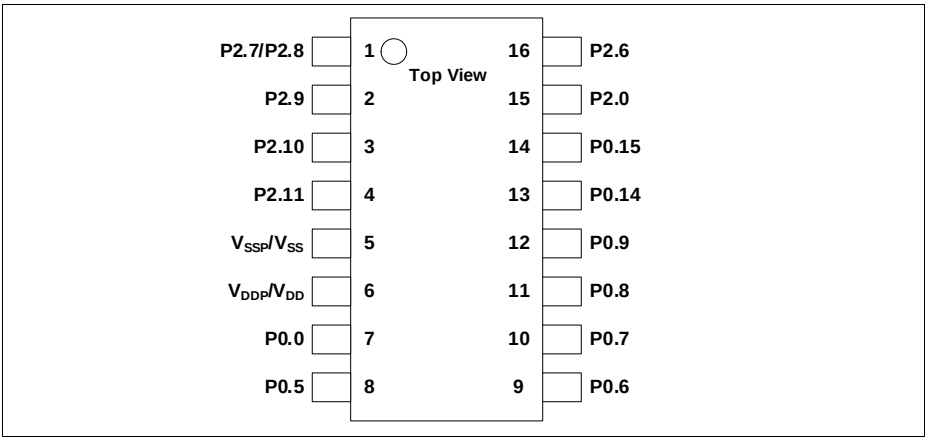


**Figure 6 XMC1200 PG-TSSOP-16 Pin Configuration** (top view)

**Table 6 Package Pin Mapping**

| Function | VQFN 40 | TSSOP 38 | TSSOP 28 | VQFN 24 | TSSOP 16 | Pad Type | Notes |
|---|---|---|---|---|---|---|---|
| VDD | 14 | 10 | 8 | 10 | 6 | Power | Supply VDD, ADC reference voltage/ORC reference voltage. VDD has to be supplied with the same voltage as VDDP |
| VDDP | 15 | 10 | 8 | 10 | 6 | Power | I/O port supply |
| VSSP | 31 | 25 | - | - | - | Power | I/O port ground |
| VDDP | 32 | 26 | - | - | - | Power | I/O port supply |
| VSSP | Exp. Pad | - | - | Exp. Pad | - | Power | **Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter. |

## Table 8 Port I/O Functions (cont'd)

| Function | Outputs | | | | | | | | | Inputs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | HWO0 | HWO1 | HWI0 | HWI1 | Input | Input | Input | Input | Input | Input | Input | Input |
| P1.6 | VADC0. EMUX12 | USIC0_CH1. DOUT0 | LEDTS0. COL5 | USIC0_CH0. SCLKOUT | | USIC0_CH0. SELO2 | USIC0_CH1. SELO3 | | | | | | | USIC0_CH0. DX5F | | | | | |
| P2.0 | ERU0. PDOUT3 | CCU40. OUT0 | ERU0. GOUT3 | LEDTS1. COL5 | | USIC0_CH0. DOUT0 | USIC0_CH0. SCLKOUT | | | | | | VADC0. G0CH5 | | ERU0.0B0 | USIC0_CH0. DX0E | USIC0_CH0. DX1E | USIC0_CH1. DX2F | |
| P2.1 | ERU0. PDOUT2 | CCU40. OUT1 | ERU0. GOUT2 | LEDTS1. COL6 | | USIC0_CH0. DOUT0 | USIC0_CH1. SCLKOUT | | | | | ACMP2.INP | VADC0. G0CH6 | | ERU0.1B0 | USIC0_CH0. DX0F | USIC0_CH1. DX3A | USIC0_CH1. DX4A | |
| P2.2 | | | | | | | | | | | | ACMP2.INN | VADC0. G0CH7 | | ERU0.0B1 | USIC0_CH0. DX3A | USIC0_CH0. DX4A | USIC0_CH1. DX5A | ORC0.AIN |
| P2.3 | | | | | | | | | | | | | VADC0. G1CH5 | | ERU0.1B1 | USIC0_CH0. DX5B | USIC0_CH1. DX3C | USIC0_CH1. DX4C | ORC1.AIN |
| P2.4 | | | | | | | | | | | | | VADC0. G1CH6 | | ERU0.0A1 | USIC0_CH0. DX3B | USIC0_CH0. DX4B | USIC0_CH1. DX5B | ORC2.AIN |
| P2.5 | | | | | | | | | | | | | VADC0. G1CH7 | | ERU0.1A1 | USIC0_CH0. DX5D | USIC0_CH1. DX3E | USIC0_CH1. DX4E | ORC3.AIN |
| P2.6 | | | | | | | | | | | | ACMP1.INN | VADC0. G0CH0 | | ERU0.2A1 | USIC0_CH0. DX3E | USIC0_CH0. DX4E | USIC0_CH1. DX5D | ORC4.AIN |
| P2.7 | | | | | | | | | | | | ACMP1.INP | VADC0. G1CH1 | | ERU0.3A1 | USIC0_CH0. DX5C | USIC0_CH1. DX3D | USIC0_CH1. DX4D | ORC5.AIN |
| P2.8 | | | | | | | | | | | | ACMP0.INN | VADC0. G0CH1 | VADC0. G1CH0 | ERU0.3B1 | USIC0_CH0. DX3D | USIC0_CH0. DX4D | USIC0_CH1. DX5C | ORC6.AIN |
| P2.9 | | | | | | | | | | | | ACMP0.INP | VADC0. G0CH2 | VADC0. G1CH4 | ERU0.3B0 | USIC0_CH0. DX5A | USIC0_CH1. DX3B | USIC0_CH1. DX4B | ORC7.AIN |
| P2.10 | ERU0. PDOUT1 | CCU40. OUT2 | ERU0. GOUT1 | LEDTS1. COL4 | | ACMP0. OUT | USIC0_CH1. DOUT0 | | | | | | VADC0. G0CH3 | VADC0. G1CH2 | ERU0.2B0 | USIC0_CH0. DX3C | USIC0_CH0. DX4C | USIC0_CH1. DX0F | |
| P2.11 | ERU0. PDOUT0 | CCU40. OUT3 | ERU0. GOUT0 | LEDTS1. COL3 | | USIC0_CH1. SCLKOUT | USIC0_CH1. DOUT0 | | | | | ACMP.REF | VADC0. G0CH4 | VADC0. G1CH3 | ERU0.2B1 | USIC0_CH1. DX0E | USIC0_CH1. DX1E | | |

### 3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 9 Absolute Maximum Rating Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Junction temperature | $T_J$ | SR | -40 | – | 115 | °C | – |
| Storage temperature | $T_S$ | SR | -40 | – | 125 | °C | – |
| Voltage on power supply pin with respect to $V_{SSP}$ | $V_{DDP}$ | SR | -0.3 | – | 6 | V | – |
| Voltage on any pin with respect to $V_{SSP}$ | $V_{IN}$ | SR | -0.5 | – | $V_{DDP}$ + 0.5 or max. 6 | V | whichever is lower |
| Voltage on any analog input pin with respect to $V_{SSP}$ | $V_{AIN}$<br>$V_{AREF}$ | SR | -0.5 | – | $V_{DDP}$ + 0.5 or max. 6 | V | – |
| Input current on any pin during overload condition | $I_{IN}$ | SR | -10 | – | 10 | mA | – |
| Absolute sum of all input currents during overload condition | $\Sigma\|I_{IN}\|$ | SR | – | – | 50 | mA | – |
| Analog comparator input voltage | $V_{CM}$ | SR | -0.3 | – | $V_{DDP}$ + 0.3 | V | |

## 3.2 DC Parameters

### 3.2.1 Input/Output Characteristics

Table 11 provides the characteristics of the input/output pins of the XMC1200.

**Table 11 Input/Output Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Output low voltage on port pins (with standard pads) | $V_{OLP}$ | CC | – | 1.0 | V | $I_{OL}$ = 11 mA (5 V)<br>$I_{OL}$ = 7 mA (3.3 V) |
| | | | – | 0.4 | V | $I_{OL}$ = 5 mA (5 V)<br>$I_{OL}$ = 3.5 mA (3.3 V) |
| Output low voltage on high current pads | $V_{OLP1}$ | CC | – | 1.0 | V | $I_{OL}$ = 50 mA (5 V)<br>$I_{OL}$ = 25 mA (3.3 V) |
| | | | – | 0.32 | V | $I_{OL}$ = 10 mA (5 V) |
| | | | – | 0.4 | V | $I_{OL}$ = 5 mA (3.3 V) |
| Output high voltage on port pins (with standard pads) | $V_{OHP}$ | CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -10 mA (5 V)<br>$I_{OH}$ = -7 mA (3.3 V) |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -4.5 mA (5 V)<br>$I_{OH}$ = -2.5 mA (3.3 V) |
| Output high voltage on high current pads | $V_{OHP1}$ | CC | $V_{DDP}$ - 0.32 | – | V | $I_{OH}$ = -6 mA (5 V) |
| | | | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -8 mA (3.3 V) |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -4 mA (3.3 V) |
| Input low voltage on port pins (Standard Hysteresis) | $V_{ILPS}$ | SR | – | 0.19 × $V_{DDP}$ | V | CMOS Mode (5 V, 3.3 V & 2.2 V) |
| Input high voltage on port pins (Standard Hysteresis) | $V_{IHPS}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode (5 V, 3.3 V & 2.2 V) |
| Input low voltage on port pins (Large Hysteresis) | $V_{ILPL}$ | SR | – | 0.08 × $V_{DDP}$ | V | CMOS Mode (5 V, 3.3 V & 2.2 V)[3)] |

**Table 12 ADC Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum sample rate in 8-bit mode [3] | $f_{C8}$ CC | – | – | $f_{ADC}$ / 38.5 | – | 1 sample pending |
| | | – | – | $f_{ADC}$ / 54.5 | – | 2 samples pending |
| DNL error | $EA_{DNL}$ CC | – | ±2.0 | – | LSB 12 | |
| INL error | $EA_{INL}$ CC | – | ±4.0 | – | LSB 12 | |
| Gain error with external reference | $EA_{GAIN}$ CC | – | ±0.5 | – | % | SHSCFG.AREF = $00_B$ (calibrated) |
| Gain error with internal reference | $EA_{GAIN}$ CC | – | ±3.6 | – | % | SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C |
| | | – | ±2.0 | – | % | SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C |
| Offset error | $EA_{OFF}$ CC | – | ±6.0 | – | LSB 12 | Calibrated |

1) Not subject to production test, verified by design/characterization.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

### 3.2.5 Temperature Sensor Characteristics

**Table 15 Temperature Sensor Characteristics[1)]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Measurement time | $t_M$ CC | – | – | 10 | ms | |
| Temperature sensor range | $T_{SR}$ SR | -40 | – | 115 | °C | |
| Sensor Accuracy[2)] | $T_{TSAL}$ CC | – | +/- 20 | – | °C | $T_J$ = -40 °C |
| | | – | +/- 12 | – | °C | $T_J$ = -25 °C |
| | | -5 | – | 5 | °C | $T_J$ = 0 °C |
| | | -2 | – | 2 | °C | $T_J$ = 25 °C |
| | | -4 | – | 4 | °C | $T_J$ = 70 °C |
| | | -2 | – | 2 | °C | $T_J$ = 115 °C |

1) Not subject to production test, verified by design/characterization.

2) The temperature sensor accuracy is independent of the supply voltage.

### 3.2.7 Flash Memory Parameters

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 18 Flash Memory Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Erase Time per page | $t_{ERASE}$ CC | 6.8 | 7.1 | 7.6 | ms | |
| Program time per block | $t_{PSER}$ CC | 102 | 152 | 204 | µs | |
| Wake-Up time | $t_{WU}$ CC | – | 32.2 | – | µs | |
| Read time per word | $t_a$ CC | – | 50 | – | ns | |
| Data Retention Time | $t_{RET}$ CC | 10 | – | – | years | Max. 100 erase / program cycles |
| Flash Wait States [1] | $N_{WSFLASH}$ CC | 0 | 0.5 | – | | $f_{MCLK}$ = 8 MHz |
| | | 0 | 1.4 | – | | $f_{MCLK}$ = 16 MHz |
| | | 1 | 1.9 | – | | $f_{MCLK}$ = 32 MHz |
| Erase Cycles per page | $N_{ECYC}$ CC | – | – | $5*10^4$ | cycles | |
| Total Erase Cycles | $N_{TECYC}$ CC | – | – | $2*10^6$ | cycles | |

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

### 3.3.2 Output Rise/Fall Times

**Table 19** provides the characteristics of the output rise/fall times in the XMC1200. **Figure 11** describes the rise time and fall time parameters.

**Table 19 Output Rise/Fall Times Parameters (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Rise/fall times on High Current Pad[1)2)] | $t_{HCPR}$, $t_{HCPF}$ | – | 9 | ns | 50 pF @ 5 V[3)] |
| | | – | 12 | ns | 50 pF @ 3.3 V[4)] |
| | | – | 25 | ns | 50 pF @ 1.8 V[5)] |
| Rise/fall times on Standard Pad[1)2)] | $t_R$, $t_F$ | – | 12 | ns | 50 pF @ 5 V[6)] |
| | | – | 15 | ns | 50 pF @ 3.3 V[7)]. |
| | | – | 31 | ns | 50 pF @ 1.8 V[8)]. |

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.
3) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
4) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
5) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
6) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
7) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
8) Additional rise/fall time valid for $C_L$ = 50 pF - $C_L$ = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.

### 3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 23 SWD Interface Timing Parameters**(Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SWDCLK high time | $t_1$ SR | 50 | – | 500000 | ns | – |
| SWDCLK low time | $t_2$ SR | 50 | – | 500000 | ns | – |
| SWDIO input setup to SWDCLK rising edge | $t_3$ SR | 10 | – | – | ns | – |
| SWDIO input hold after SWDCLK rising edge | $t_4$ SR | 10 | – | – | ns | – |
| SWDIO output valid time after SWDCLK rising edge | $t_5$ CC | – | – | 68 | ns | $C_L$ = 50 pF |
| | | – | – | 62 | ns | $C_L$ = 30 pF |
| SWDIO output hold time from SWDCLK rising edge | $t_6$ CC | 4 | – | – | ns | |

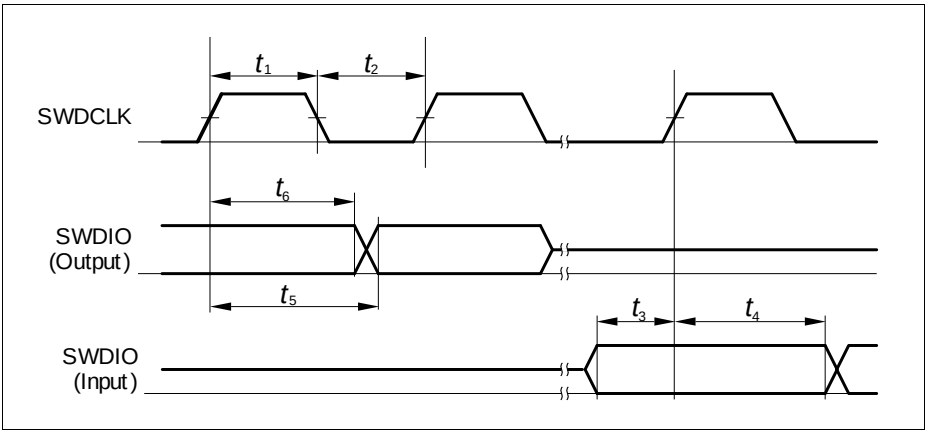


**Figure 16 SWD Timing**

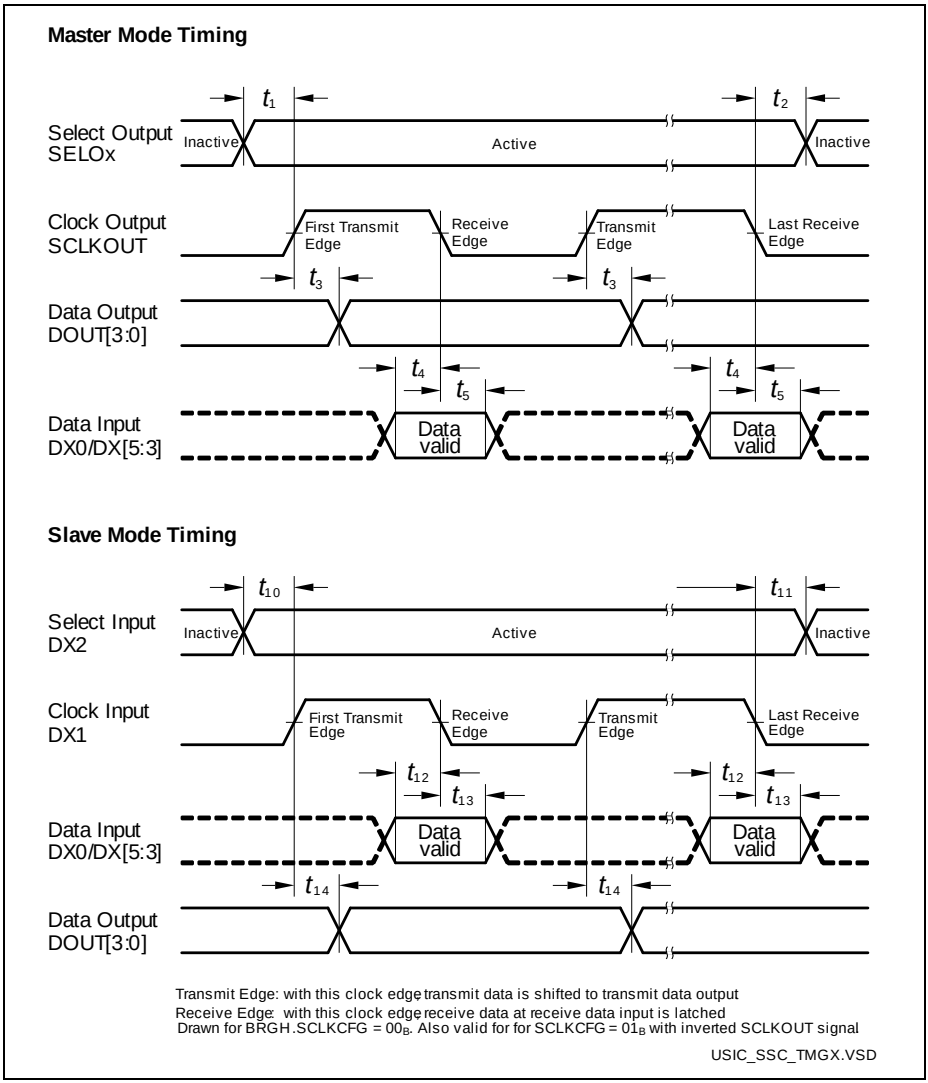


**Figure 17 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

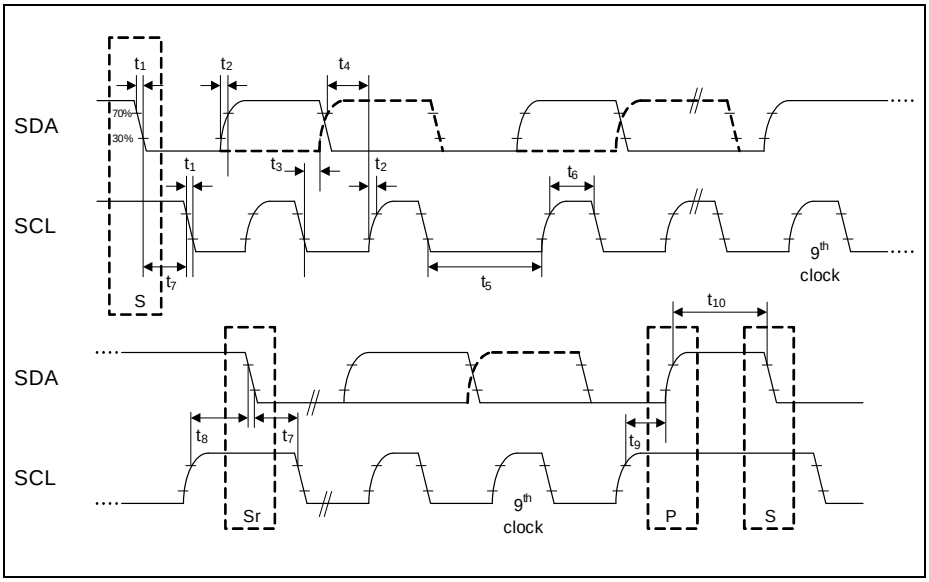


**Figure 18 USIC IIC Stand and Fast Mode Timing**

### 3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 29 USIC IIS Master Transmitter Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_1$ CC | $2/f_{MCLK}$ | - | - | ns | $V_{DDP} \geq 3$ V |
| | | $4/f_{MCLK}$ | - | - | ns | $V_{DDP} < 3$ V |
| Clock HIGH | $t_2$ CC | 0.35 x $t_{1min}$ | - | - | ns | |
| Clock Low | $t_3$ CC | 0.35 x $t_{1min}$ | - | - | ns | |
| Hold time | $t_4$ CC | 0 | - | - | ns | |
| Clock rise time | $t_5$ CC | - | - | 0.15 x $t_{1min}$ | ns | |

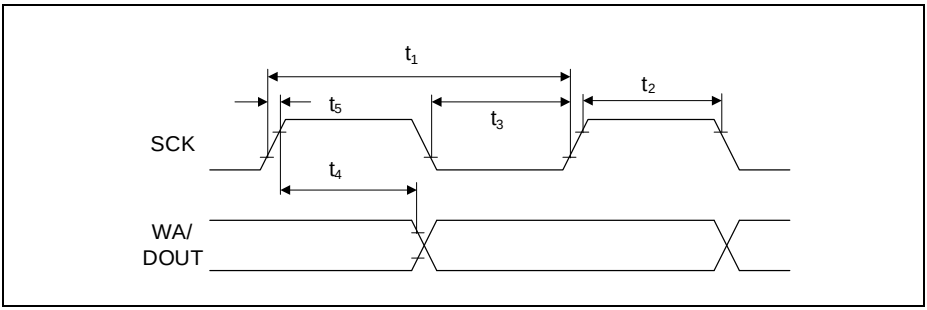


**Figure 19 USIC IIS Master Transmitter Timing**

**Table 30 USIC IIS Slave Receiver Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_6$ SR | $4/f_{MCLK}$ | - | - | ns | |
| Clock HIGH | $t_7$ SR | 0.35 x $t_{6min}$ | - | - | ns | |
| Clock Low | $t_8$ SR | 0.35 x $t_{6min}$ | - | - | ns | |
| Set-up time | $t_9$ SR | 0.2 x $t_{6min}$ | - | - | ns | |
| Hold time | $t_{10}$ SR | 10 | - | - | ns | |

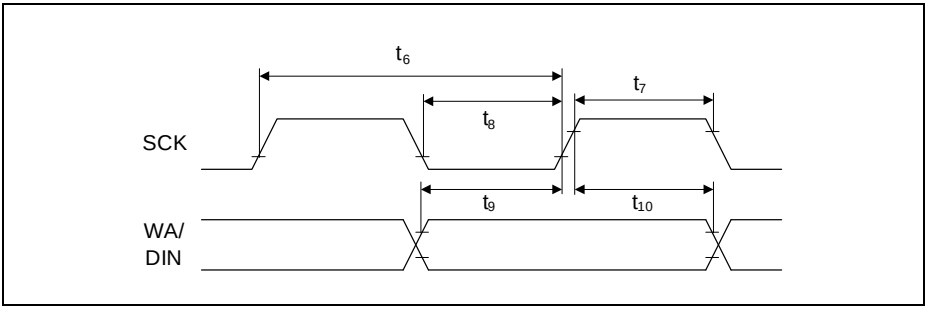


**Figure 20 USIC IIS Slave Receiver Timing**

# 4 Package and Reliability

The XMC1200 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

## 4.1 Package Parameters

**Table 31** provides the thermal characteristics of the packages used in XMC1200.

**Table 31 Thermal Characteristics of the Packages**

| Parameter | Symbol | Limit Values | | Unit | Package Types |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Exposed Die Pad Dimensions | Ex × Ey CC | - | 2.7 × 2.7 | mm | PG-VQFN-24-19 |
| | | - | 3.7 × 3.7 | mm | PG-VQFN-40-13 |
| Thermal resistance Junction-Ambient | $R_{\Theta JA}$ CC | - | 104.6 | K/W | PG-TSSOP-16-8[1)] |
| | | - | 83.2 | K/W | PG-TSSOP-28-16[1)] |
| | | - | 70.3 | K/W | PG-TSSOP-38-9[1)] |
| | | - | 46.0 | K/W | PG-VQFN-24-19[1)] |
| | | - | 38.4 | K/W | PG-VQFN-40-13[1)] |

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

*Note: For electrical reasons, it is required to connect the exposed pad to the board ground $V_{SSP}$, independent of EMC and thermal requirements.*

### 4.1.1 Thermal Considerations

When operating the XMC1200 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

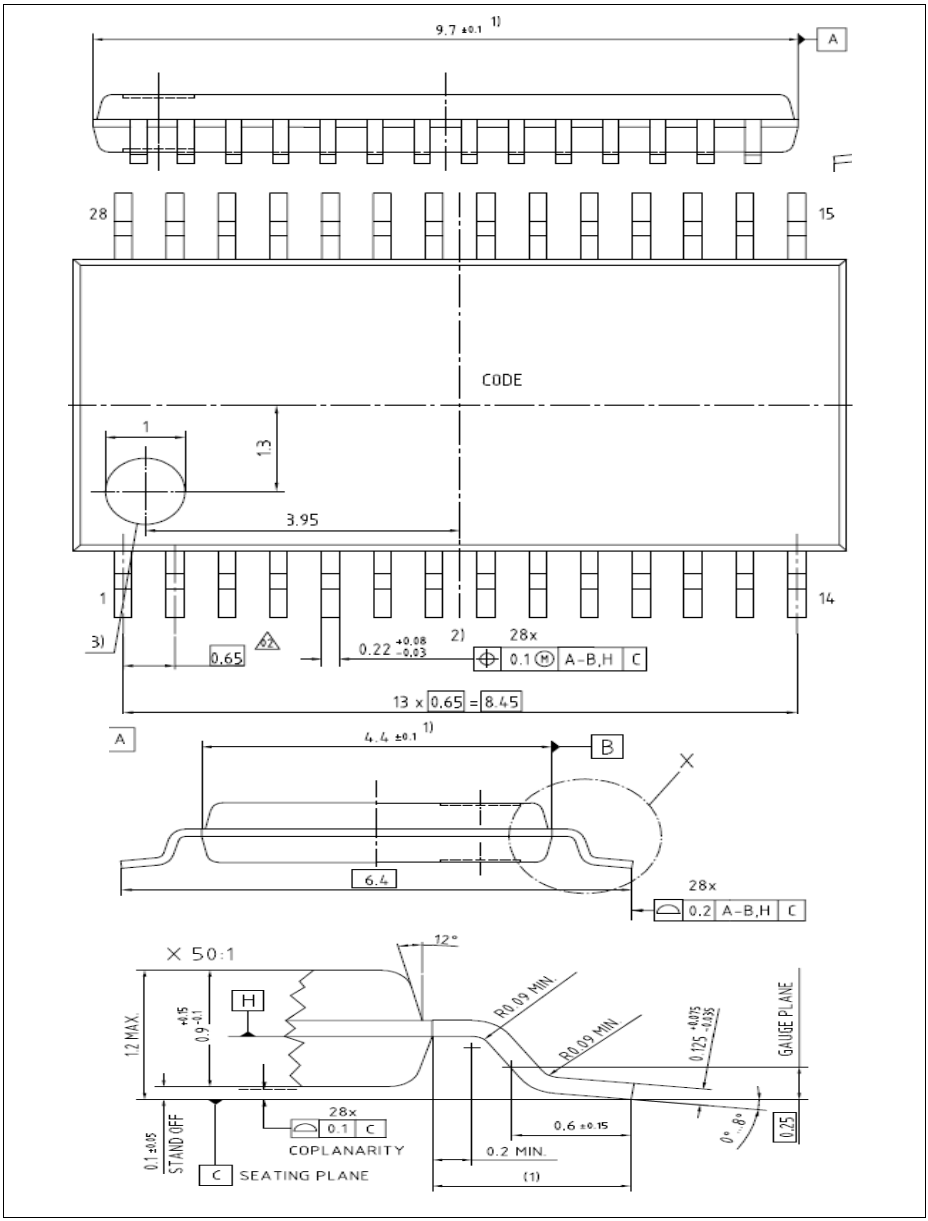


**Figure 22 PG-TSSOP-28-16**

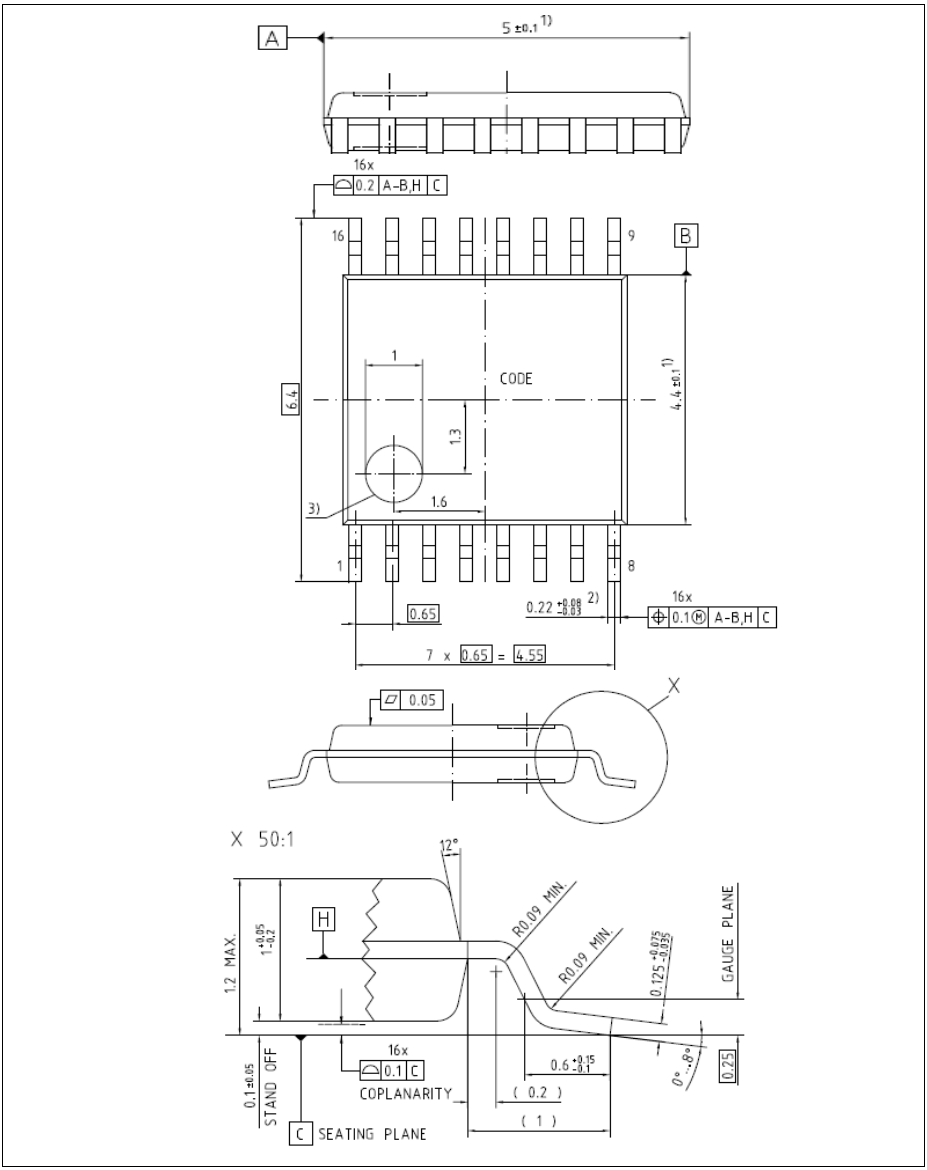


**Figure 23 PG-TSSOP-16-8**