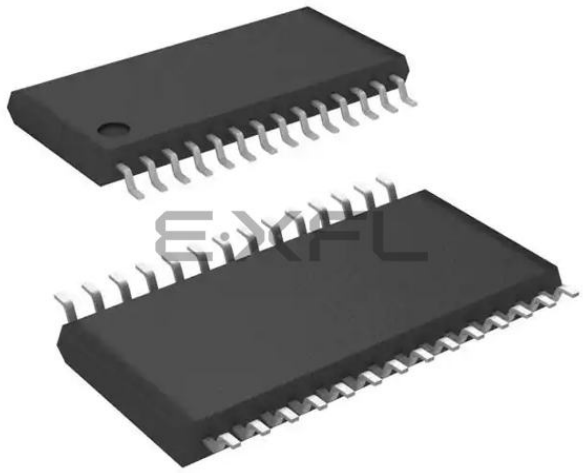
Infineon Technologies - XMC1202T028X0064AAXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	20
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 14x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-28-16
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1202t028x0064aaxuma1

XMC1200

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex™-M0
32-bit processor core

Data Sheet

V1.4 2014-05

Microcontrollers

1 Summary of Features

The XMC1200 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1200 series devices are optimized for LED Lighting and Human-Machine interface (HMI) applications.

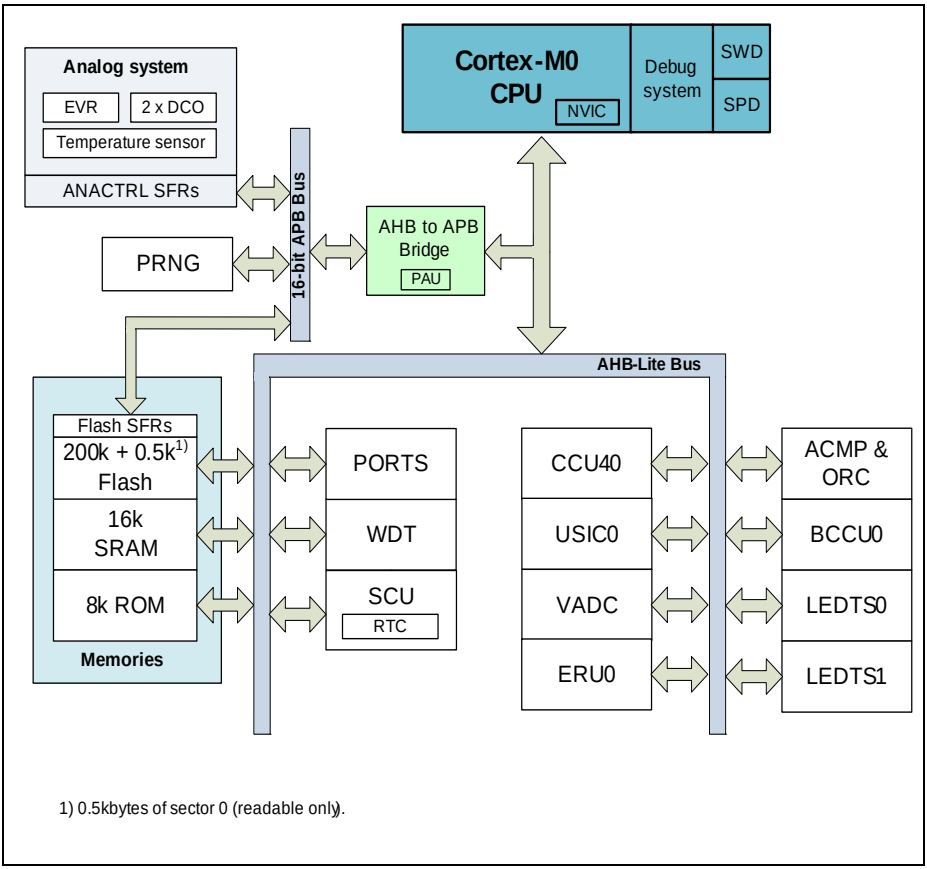

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M0 CPU
  - Most of 16-bit Thumb instruction set
  - Subset of 32-bit Thumb2 instruction set

  - High code density with 32-bit performance
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support
  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

Communication Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

Analog Frontend Peripherals

- A/D Converters, up to 12 channels, includes 2 sample and hold stages and a fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

Industrial Control Peripherals

- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode

Table 1 Synopsis of XMC1200 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1200-T038F0200	PG-TSSOP-38-9	200	16
XMC1202-T028X0016	PG-TSSOP-28-16	16	16
XMC1202-T028X0032	PG-TSSOP-28-16	32	16
XMC1202-T016X0016	PG-TSSOP-16-8	16	16
XMC1202-T016X0032	PG-TSSOP-16-8	32	16
XMC1202-Q024X0016	PG-VQFN-24-19	16	16
XMC1202-Q024X0032	PG-VQFN-24-19	32	16
XMC1201-Q040F0016	PG-VQFN-40-13	16	16
XMC1201-Q040F0032	PG-VQFN-40-13	32	16
XMC1201-Q040F0064	PG-VQFN-40-13	64	16
XMC1201-Q040F0128	PG-VQFN-40-13	128	16
XMC1201-Q040F0200	PG-VQFN-40-13	200	16
XMC1202-Q040X0016	PG-VQFN-40-13	16	16
XMC1202-Q040X0032	PG-VQFN-40-13	32	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1200 Device Types[1)]

Derivative	ADC channel	ACMP	BCCU	LEDTS
XMC1200-T038	16	3	1	2
XMC1201-T038	16	-	-	2
XMC1202-T028	14	3	1	-
XMC1202-T016	11	2	1	-
XMC1202-Q024	13	3	1	-
XMC1201-Q040	16	-	-	2
XMC1202-Q040	16	3	1	-

1) Features that are not included in this table are available in all the derivatives

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

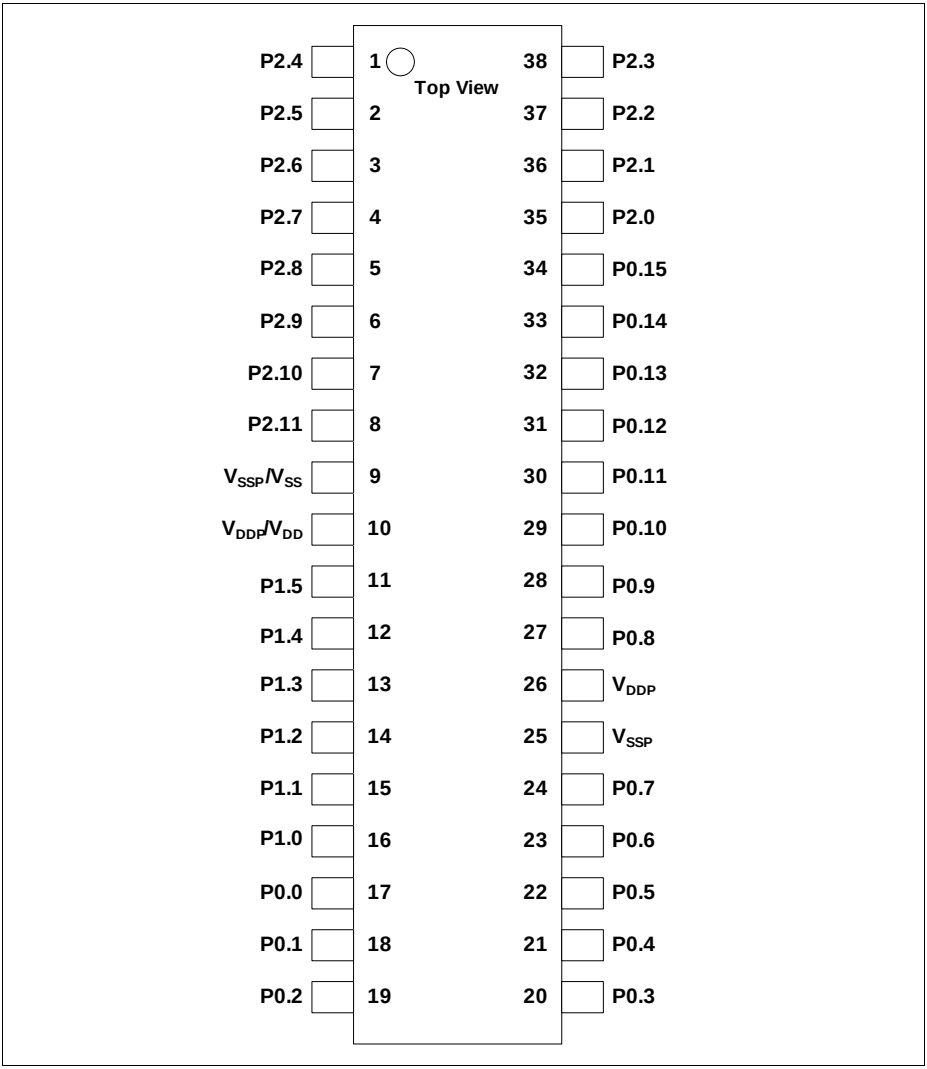

Figure 4 XMC1200 PG-TSSOP-38 Pin Configuration (top view)

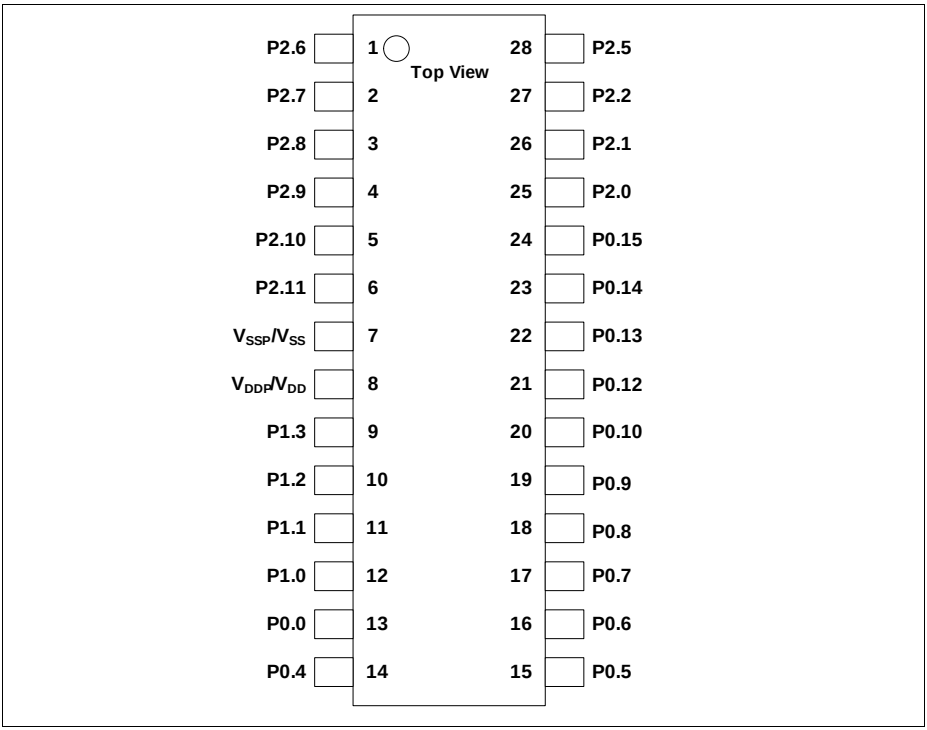

Figure 5 XMC1200 PG-TSSOP-28 Pin Configuration (top view)

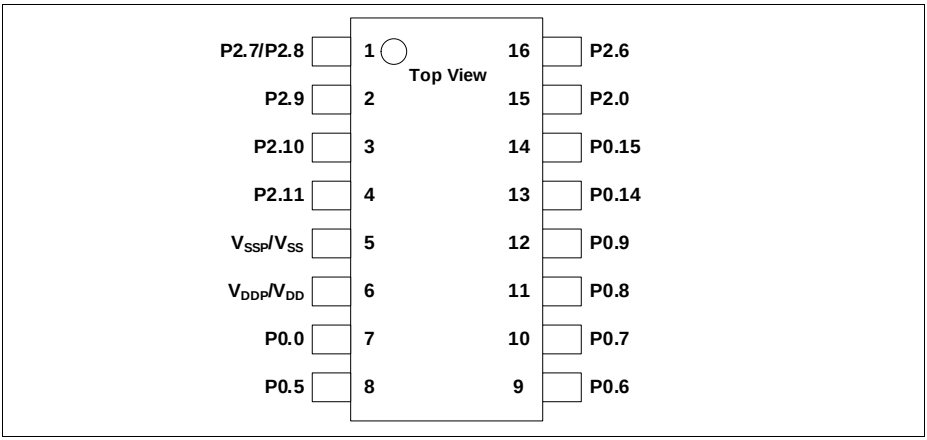

Figure 6 XMC1200 PG-TSSOP-16 Pin Configuration (top view)

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 8 Port I/O Functions

Function	Outputs									Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0. PDOUT0	LEDTS0. LINE7	ERU0. GOUT0	CCU40. OUT0		USIC0_CH0. SELO0	USIC0_CH1. SELO0	LEDTS0. EXTENDED7		LEDTS0. TSIN7	LEDTS0. TSIN7	BCCU0. TRAPINB	CCU40.IN0C			USIC0_CH0. DX2A	USIC0_CH1. DX2A		
P0.1	ERU0. PDOUT1	LEDTS0. LINE6	ERU0. GOUT1	CCU40. OUT1		BCCU0. OUT8	SCU. VDROP	LEDTS0. EXTENDED6		LEDTS0. TSIN6	LEDTS0. TSIN6		CCU40.IN1C						
P0.2	ERU0. PDOUT2	LEDTS0. LINE5	ERU0. GOUT2	CCU40. OUT2		VADC0. EMUX02		LEDTS0. EXTENDED5		LEDTS0. TSIN5	LEDTS0. TSIN5		CCU40.IN2C						
P0.3	ERU0. PDOUT3	LEDTS0. LINE4	ERU0. GOUT3	CCU40. OUT3		VADC0. EMUX01		LEDTS0. EXTENDED4		LEDTS0. TSIN4	LEDTS0. TSIN4		CCU40.IN3C						
P0.4	BCCU0. OUT0	LEDTS0. LINE3	LEDTS0. COL3	CCU40. OUT1		VADC0. EMUX00	WWDT. SERVICE_OUT	LEDTS0. EXTENDED3		LEDTS0. TSIN3	LEDTS0. TSIN3								
P0.5	BCCU0. OUT1	LEDTS0. LINE2	LEDTS0. COL2	CCU40. OUT0		ACMP2. OUT		LEDTS0. EXTENDED2		LEDTS0. TSIN2	LEDTS0. TSIN2								
P0.6	BCCU0. OUT2	LEDTS0. LINE1	LEDTS0. COL1	CCU40. OUT0		USIC0_CH1. MCLKOUT	USIC0_CH1. DOUT0	LEDTS0. EXTENDED1		LEDTS0. TSIN1	LEDTS0. TSIN1		CCU40.IN0B			USIC0_CH1. DX0C			
P0.7	BCCU0. OUT3	LEDTS0. LINE0	LEDTS0. COL0	CCU40. OUT1		USIC0_CH0. SCLKOUT	USIC0_CH1. DOUT0	LEDTS0. EXTENDED0		LEDTS0. TSIN0	LEDTS0. TSIN0		CCU40.IN1B			USIC0_CH0. DX1C	USIC0_CH1. DX0D	USIC0_CH1. DX1C	
P0.8	BCCU0. OUT4	LEDTS1. LINE0	LEDTS0. COLA	CCU40. OUT2		USIC0_CH0. SCLKOUT	USIC0_CH1. SCLKOUT	LEDTS1. EXTENDED0		LEDTS1. TSIN0	LEDTS1. TSIN0		CCU40.IN2B			USIC0_CH0. DX1B	USIC0_CH1. DX1B		
P0.9	BCCU0. OUT5	LEDTS1. LINE1	LEDTS0. COL6	CCU40. OUT3		USIC0_CH0. SELO0	USIC0_CH1. SELO0	LEDTS1. EXTENDED1		LEDTS1. TSIN1	LEDTS1. TSIN1		CCU40.IN3B			USIC0_CH0. DX2B	USIC0_CH1. DX2B		
P0.10	BCCU0. OUT6	LEDTS1. LINE2	LEDTS0. COL5	ACMP0. OUT		USIC0_CH0. SELO1	USIC0_CH1. SELO1	LEDTS1. EXTENDED2		LEDTS1. TSIN2	LEDTS1. TSIN2					USIC0_CH0. DX2C	USIC0_CH1. DX2C		
P0.11	BCCU0. OUT7	LEDTS1. LINE3	LEDTS0. COL4	USIC0_CH0. MCLKOUT		USIC0_CH0. SELO2	USIC0_CH1. SELO2	LEDTS1. EXTENDED3		LEDTS1. TSIN3	LEDTS1. TSIN3					USIC0_CH0. DX2D	USIC0_CH1. DX2D		
P0.12	BCCU0. OUT6	LEDTS1. LINE4	LEDTS0. COL3	LEDTS1. COL3		USIC0_CH0. SELO3		LEDTS1. EXTENDED4		LEDTS1. TSIN4	LEDTS1. TSIN4	BCCU0. TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	USIC0_CH0. DX2E		
P0.13	WWDT. SERVICE_OUT	LEDTS1. LINE5	LEDTS0. COL2	LEDTS1. COL2		USIC0_CH0. SELO4		LEDTS1. EXTENDED5		LEDTS1. TSIN5	LEDTS1. TSIN5					USIC0_CH0. DX2F			
P0.14	BCCU0. OUT7	LEDTS1. LINE6	LEDTS0. COL1	LEDTS1. COL1		USIC0_CH0. DOUT0	USIC0_CH0. SCLKOUT	LEDTS1. EXTENDED6		LEDTS1. TSIN6	LEDTS1. TSIN6					USIC0_CH0. DX0A	USIC0_CH0. DX1A		
P0.15	BCCU0. OUT8	LEDTS1. LINE7	LEDTS0. COL0	LEDTS1. COL0		USIC0_CH0. DOUT0	USIC0_CH1. MCLKOUT	LEDTS1. EXTENDED7		LEDTS1. TSIN7	LEDTS1. TSIN7					USIC0_CH0. DX0B			
P1.0	BCCU0. OUT0	CCU40. OUT0	LEDTS0. COL0	LEDTS1. COLA		ACMP1. OUT	USIC0_CH0. DOUT0		USIC0_CH0. DOUT0		USIC0_CH0. HWIN0					USIC0_CH0. DX0C			
P1.1	VADC0. EMUX00	CCU40. OUT1	LEDTS0. COL1	LEDTS1. COL0		USIC0_CH0. DOUT0	USIC0_CH1. SELO0		USIC0_CH0. DOUT1		USIC0_CH0. HWIN1					USIC0_CH0. DX0D	USIC0_CH0. DX1D	USIC0_CH1. DX2E	
P1.2	VADC0. EMUX01	CCU40. OUT2	LEDTS0. COL2	LEDTS1. COL1		ACMP2. OUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT2		USIC0_CH0. HWIN2					USIC0_CH1. DX0B			
P1.3	VADC0. EMUX02	CCU40. OUT3	LEDTS0. COL3	LEDTS1. COL2		USIC0_CH1. SCLKOUT	USIC0_CH1. DOUT0		USIC0_CH0. DOUT3		USIC0_CH0. HWIN3					USIC0_CH1. DX0A	USIC0_CH1. DX1A		
P1.4	VADC0. EMUX10	USIC0_CH1. SCLKOUT	LEDTS0. COL4	LEDTS1. COL3		USIC0_CH0. SELO0	USIC0_CH1. SELO1									USIC0_CH0. DX5E	USIC0_CH1. DX5E		
P1.5	VADC0. EMUX11	USIC0_CH0. DOUT0	LEDTS0. COLA	BCCU0. OUT1		USIC0_CH0. SELO1	USIC0_CH1. SELO2									USIC0_CH1. DX5F			

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1200.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1200 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1200 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1200 is designed in.

Table 12 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC		1		–	GNCTRxz.GAINy = 00_B (unity gain)
			3		–	GNCTRxz.GAINy = 01_B (gain g1)
			6		–	GNCTRxz.GAINy = 10_B (gain g2)
			12		–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	V_{DDP} = 5.0 V
		3	–	–	1 / f_{ADC}	V_{DDP} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DDP} = 1.8 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC		9		1 / f_{ADC}	2)
Conversion time in 12-bit mode	t_{C12} CC		20		1 / f_{ADC}	2)
Maximum sample rate in 12-bit mode 3)	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC		18		1 / f_{ADC}	2)
Maximum sample rate in 10-bit mode 3)	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC		16		1 / f_{ADC}	2)

Table 12 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode [3]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±6.0	–	LSB 12	Calibrated

1) Not subject to production test, verified by design/characterization.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

3.3 AC Parameters

3.3.1 Testing Waveforms

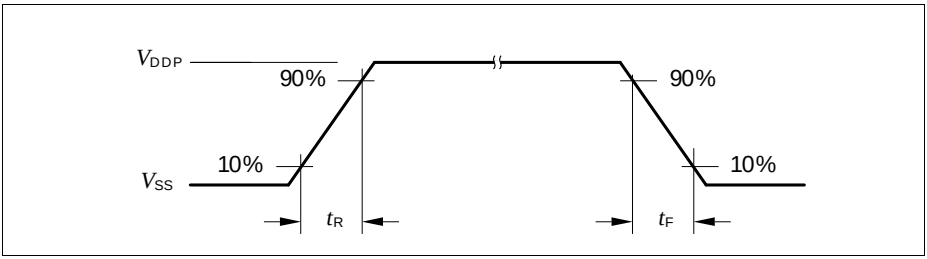

Figure 11 Rise/Fall Time Parameters

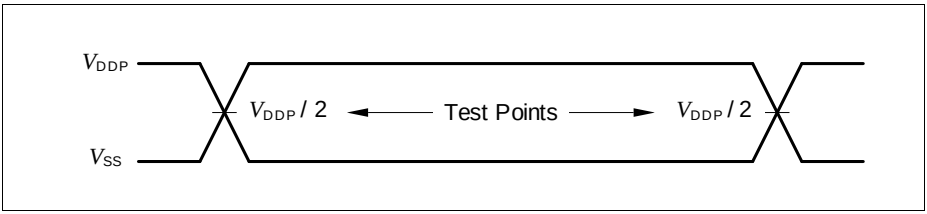

Figure 12 Testing Waveform, Output Delay

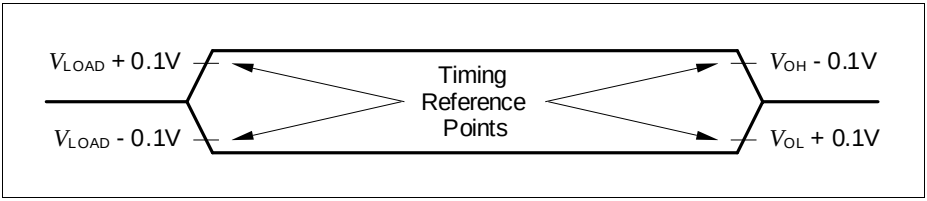

Figure 13 Testing Waveform, Output High Impedance

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	68	ns	C_L = 50 pF
		–	–	62	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	–	–	ns	

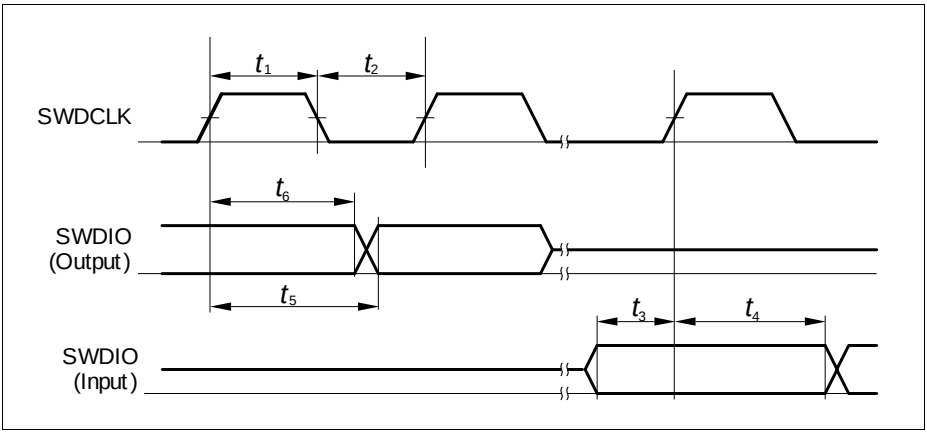

Figure 16 SWD Timing

3.3.6 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 24 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

3.3.7 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.7.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 25 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	0	–	–	ns	

Table 26 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10}	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11}	SR	10	–	–	ns	

Table 26 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

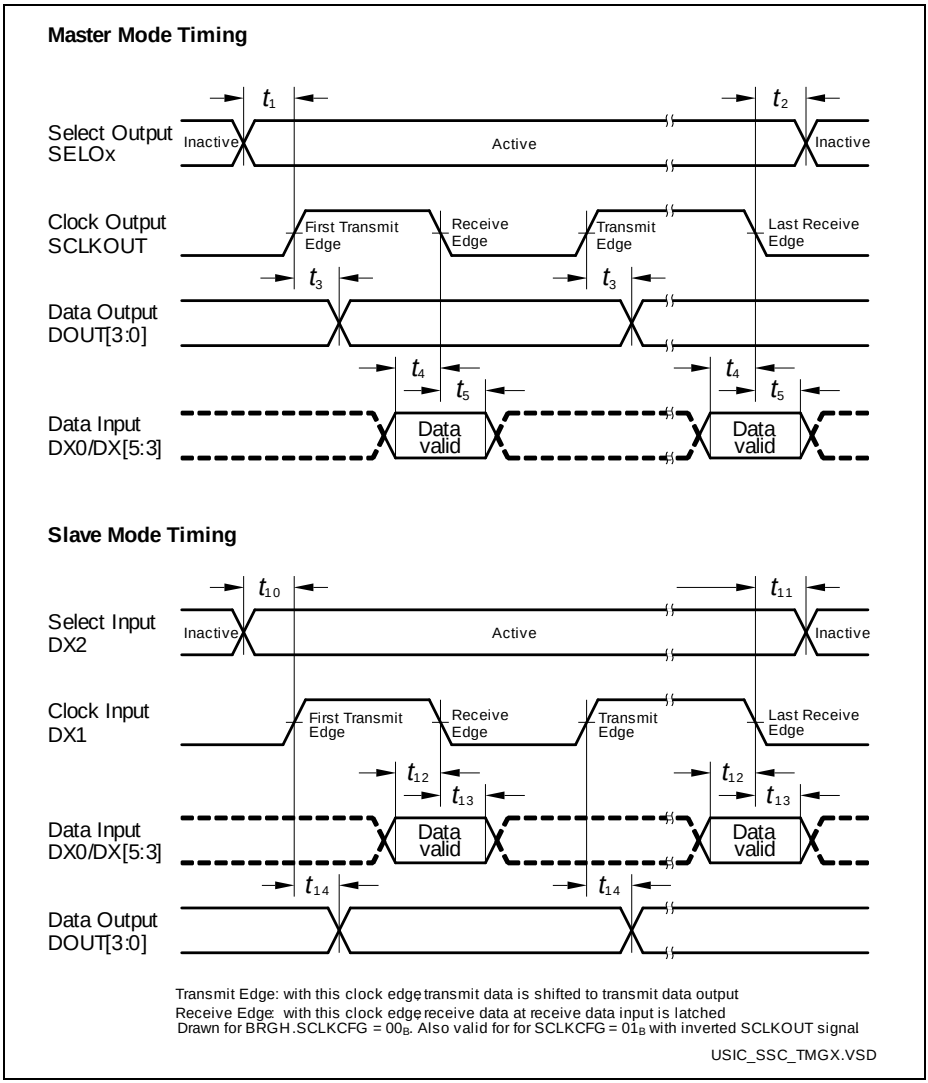

Figure 17 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

4 Package and Reliability

The XMC1200 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 31 provides the thermal characteristics of the packages used in XMC1200.

Table 31 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8[1)]
		-	83.2	K/W	PG-TSSOP-28-16[1)]
		-	70.3	K/W	PG-TSSOP-38-9[1)]
		-	46.0	K/W	PG-VQFN-24-19[1)]
		-	38.4	K/W	PG-VQFN-40-13[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1200 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

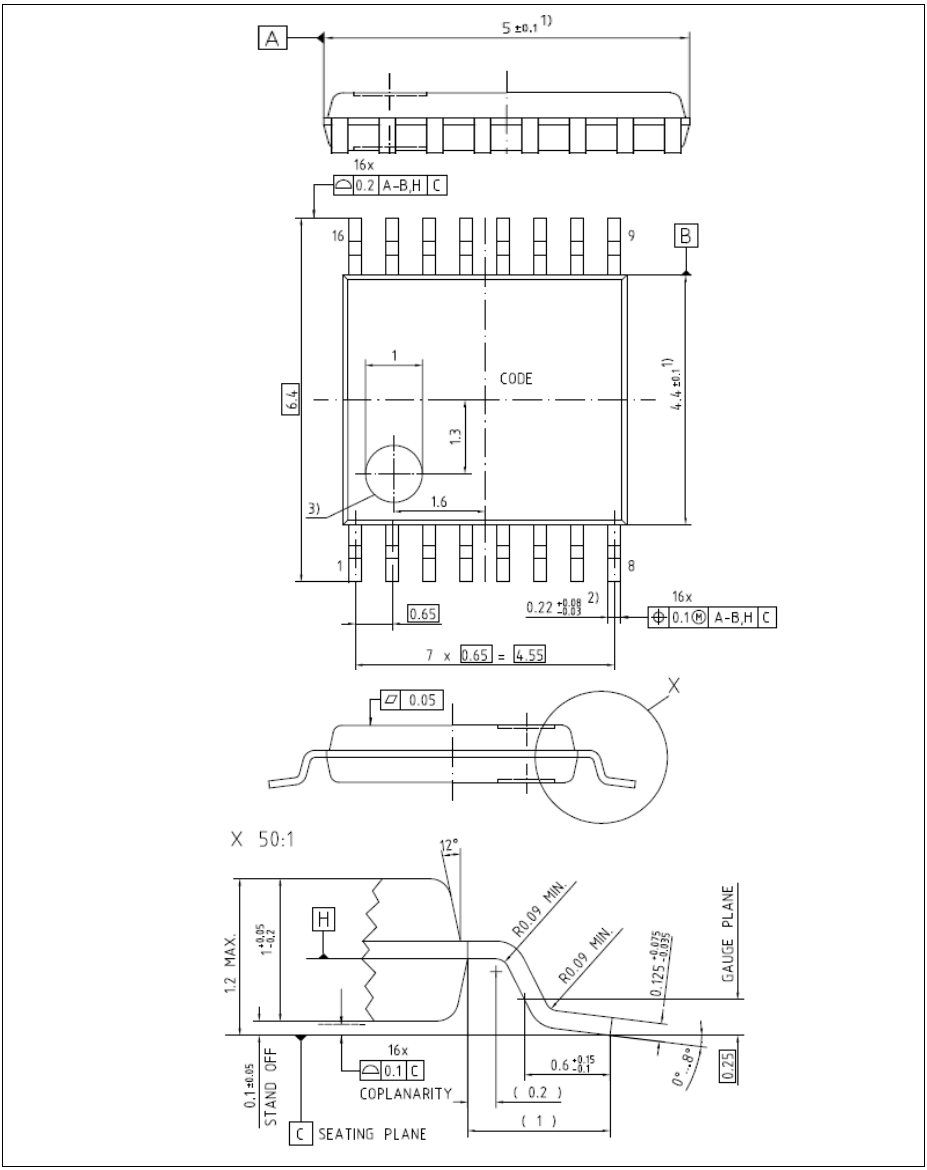

Figure 23 PG-TSSOP-16-8

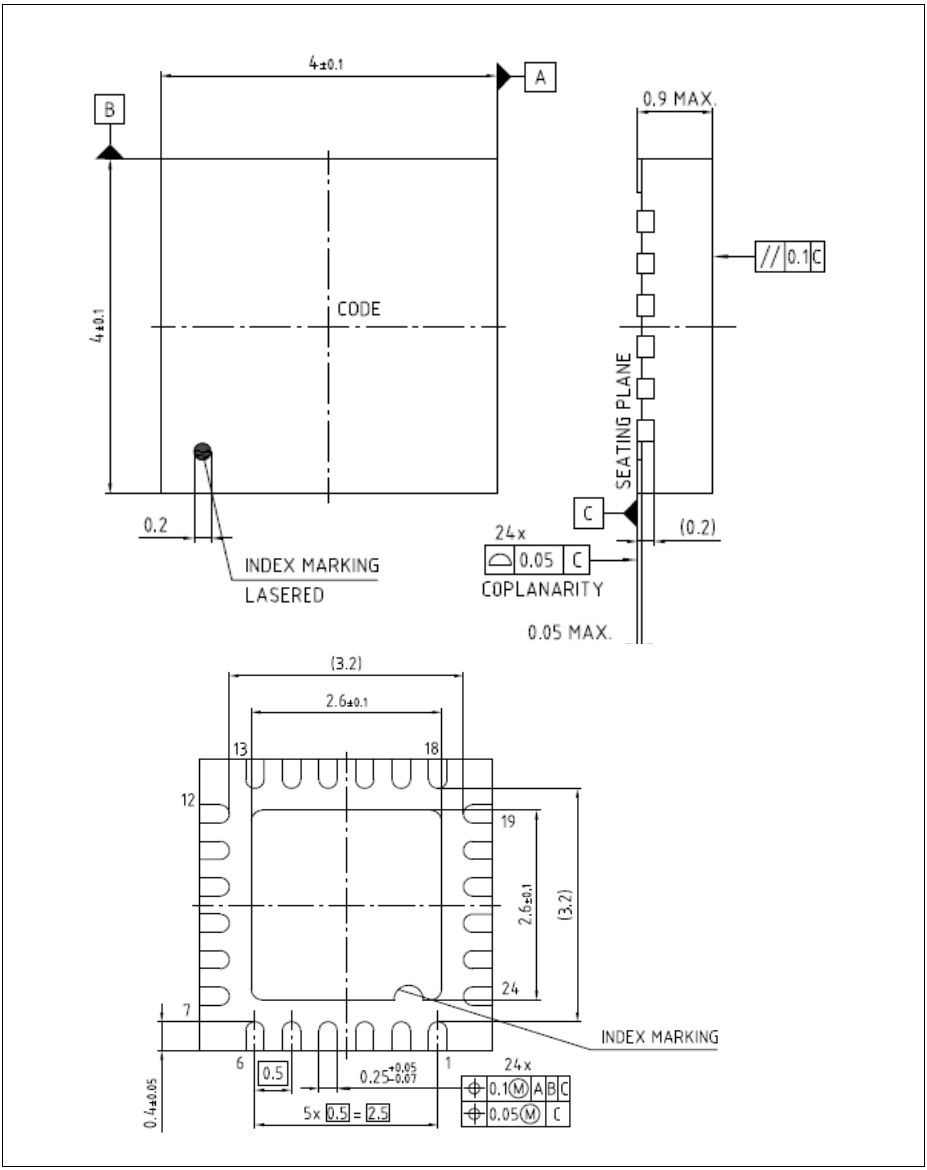

Figure 24 PG-VQFN-24-19