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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	74
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 22x12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/toshiba-semiconductor-and-storage/tmpm370fydfg

1.4 Pin names and Functions

Table 1-1 sorts the input and output pins of the TMPM370FYDFG/FYFG by pin or port. Each table includes alternate pin names and functions for multi-function pins.

1.4.1 Sorted by Port

Table 1-1 Pin Names and Functions Sorted by Port (1/5)

PORT	Type	Pin No. (DFG/ FG)	Pin Name	Input / Output	Function
PORT A	Function	4 / 2	PA0 TB0IN INT3	I/O I I	I/O port Inputting the timer B capture trigger External interrupt pin
PORT A	Function	5 / 3	PA1 TB0OUT	I/O O	I/O port Timer B output
PORT A	Function	6 / 4	PA2 TB1IN INT4	I/O I I	I/O port Inputting the timer B capture trigger External interrupt pin
PORT A	Function	7 / 5	PA3 TB1OUT	I/O O	I/O port Timer B output
PORT A	Function	8 / 6	PA4 SCLK1 $\overline{\text{CTS1}}$	I/O I/O I	I/O port Serial clock input/ output Handshake input pin
PORT A	Function	9 / 7	PA5 TXD1 TB6OUT	I/O O O	I/O port Sending serial data Timer B output
PORT A	Function	10 / 8	PA6 RXD1 TB6IN	I/O I I	I/O port Receiving serial data Inputting the timer B capture trigger
PORT A	Function	11 / 9	PA7 TB4IN INT8	I/O I I	I/O port Inputting the timer B capture trigger External interrupt pin
PORT B	Function/ Debug	65 / 63	PB0 TRACECLK	I/O O	I/O port Debug pin
PORT B	Function/ Debug	66 / 64	PB1 TRACEDATA0	I/O O	I/O port Debug pin
PORT B	Function/ Debug	67 / 65	PB2 TRACEDATA1	I/O O	I/O port Debug pin
PORT B	Function/ Debug	68 / 66	PB3 TMS/SWDIO	I/O I/O	I/O port Debug pin
PORT B	Function/ Debug	69 / 67	PB4 TCK/SWCLK	I/O I	I/O port Debug pin
PORT B	Function/ Debug	70 / 68	PB5 TDO/SWV	I/O O	I/O port Debug pin
PORT B	Function/ Debug	71 / 69	PB6 TDI	I/O I	I/O port Debug pin
PORT B	Function/ Debug	72 / 70	PB7 $\overline{\text{TRST}}$	I/O I	I/O port Debug pin
PORT C	Function	24 / 22	PC0 UO0	I/O O	I/O port U-phase output pin

Table 1-1 Pin Names and Functions Sorted by Port (4/5)

PORT	Type	Pin No. (DFG/ FG)	Pin Name	Input / Output	Function
PORT H	Function	93 / 91	PH5 AINA5	I/O I	I/O port Analog input
PORT H	Function	92 / 90	PH6 AINA6	I/O I	I/O port Analog input
PORT H	Function	91 / 89	PH7 AINA7	I/O I	I/O port Analog input
PORT I	Function	90 / 88	PI0 AINA8	I/O I	I/O port Analog input
PORT I	Function	87 / 85	PI1 AINA9/AINB0	I/O I	I/O port Analog input
PORT I	Function	86 / 84	PI2 AINA10/AINB1	I/O I	I/O port Analog input
PORT I	Function	85 / 83	PI3 AINA11/AINB2	I/O I	I/O port Analog input
PORT J	Function	82 / 80	PJ0 AINB3	I/O I	I/O port Analog input
PORT J	Function	81 / 79	PJ1 AINB4	I/O I	I/O port Analog input
PORT J	Function	80 / 78	PJ2 AINB5	I/O I	I/O port Analog input
PORT J	Function	79 / 77	PJ3 AINB6	I/O I	I/O port Analog input
PORT J	Function	78 / 76	PJ4 AINB7	I/O I	I/O port Analog input
PORT J	Function	77 / 75	PJ5 AINB8	I/O I	I/O port Analog input
PORT J	Function	76 / 74	PJ6 INTC AINB9	I/O I I	I/O port External interrupt pin Analog input
PORT J	Function	75 / 73	PJ7 INTD AINB10	I/O I I	I/O port External interrupt pin Analog input
PORT K	Function	74 / 72	PK0 INTE AINB11	I/O I I	I/O port External interrupt pin Analog input
PORT K	Function	73 / 71	PK1 INTF AINB12	I/O I I	I/O port External interrupt pin Analog input
PORT L	Function	22 / 20	PL0 INTB	I I	Input port External interrupt pin
PORT L	Function	23 / 21	PL1 INTA	I I	Input port External interrupt pin
-	Clock	49 / 47	X1	I	Connected to a high-speed oscillator
-	Clock	51 / 49	X2	O	Connected to a high-speed oscillator
-	Control		MODE	I	Mode pin (note) MODE pin must be connected to GND.

5.3.6 System Clock

The TMPM370FYDFG/FYFG offers high-speed clock as system clock. The high-speed clock is dividable.

- Input frequency from X1 and X2 : 8 MHz to 10MHz
- Clock gear : 1/1, 1/2, 1/4, 1/8, 1/16 (after reset : 1/1)

Table 5-1 Range of high-speed frequency (unit : MHz)

Input freq.		Min. operating freq.	Max. operating freq.	After reset (PLL = OFF, CG = 1/1)	Clock gear (CG) : PLL = ON					Clock gear (CG) : PLL = OFF				
					1/1	1/2	1/4	1/8	1/16	1/1	1/2	1/4	1/8	1/16
OSC	8	1	80	8	64	32	16	8	4	8	4	2	1	-
	10			10	80	40	20	10	5	10	5	2.5	1.25	-

Note 1: PLL=ON/OFF setting: available in CGOSCCR<PLLON>.

Note 2: Switching of clock gear is executed when a value is written to the CGSYSCR<GEAR[2:0]> register. The actual switching takes place after a slight delay.

Note 3: "-" : Reserved

Note 4: Do not use 1/16 when "PLL =OFF" is used.

Note 5: Do not use 1/16 when SysTick is used.

Bit	Bit Symbol	Type	Function
31	–	R	Read as 0.
30-28	EMCG7[2:0]	R/W	active level setting of INT7 standby clear request. (101 to 111: setting prohibited) 000: "Low" level 001: "High" level 010: Falling edge 011: Rising edge 100: Both edge
27-26	EMST7[1:0]	R	active level of INT7 standby clear request 00: – 01: Rising edge 10: Falling edge 11: Both edge
25	–	R	Reads as undefined.
24	INT7EN	R/W	INT7 clear input 0: Disable 1: Enable
23	–	R	Read as 0.
22-20	EMCG6[2:0]	R/W	active level setting of INT6 standby clear request. (101 to 111: setting prohibited) 000: "Low" level 001: "High" level 010: Falling edge 011: Rising edge 100: Both edge
19-18	EMST6[1:0]	R	active level of INT6 standby clear request 00: – 01: Rising edge 10: Falling edge 11: Both edge
17	–	R	Reads as undefined.
16	INT6EN	R/W	INT6 clear input 0:Disable 1: Enable
15	–	R	Read as 0.
14-12	EMCG5[2:0]	R/W	active level setting of INT5 standby clear request. (101 to 111: setting prohibited) 000: "Low" level 001: "High" level 010: Falling edge 011: Rising edge 100: Both edge
11-10	EMST5[1:0]	R	active level of INT5 standby clear request 00: – 01: Rising edge 10: Falling edge 11: Both edge
9	–	R	Reads as undefined.
8	INT5EN	R/W	INT5 clear input 0: Disable 1: Enable
7	–	R	Read as 0.
6-4	EMCG4[2:0]	R/W	active level setting of INT4 standby clear request. (101 to 111: setting prohibited) 000: "Low" level 001: "High" level 010: Falling edge 011: Rising edge 100: Both edge
3-2	EMST4[1:0]	R	active level of INT4 standby clear request 00: – 01: Rising edge 10: Falling edge 11: Both edge
1	–	R	Reads as undefined.

6.6.3.5 CGICRCG (CG Interrupt Request Clear Register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	-	-	-	ICRCG				
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-5	–	R	Read as 0,
4-0	ICRCG[4:0]	W	Clear interrupt requests. 0_0000:INT0 0_1000: INT8 0_0001: INT1 0_1001: INT9 0_0010: INT2 0_1010:INTA 0_0011: INT3 0_1011: INTB 0_0100: INT4 0_1100:INTC 0_0101: INT5 0_1101: INTD 0_0110: INT6 0_1110: INTE 0_ 0111: INT7 0_1111: INTF 1_0000 to 1_1111: Reserved Read as 0.

7.2.11.9 PKIE (Port K input control register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	-	-	-	-	-	-	PK1IE	PK0IE
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-2	–	R	Read as 0.
1-0	PK1IE-PK0IE	R/W	Input 0: Disable 1: Enable

7.3 Block Diagrams of Ports

7.3.1 Port Types

The ports are classified as shown below. Please refer to the following pages for the block diagrams of each port type.

Dot lines in the figure indicate the part of the equivalent circuit described in the "Block diagrams of ports".

Table 7-3 Function Lists

Type	GP Port	Function1	Function2	Function3	Analog	Pull-up	Pull-dn	Program-mable open-drain	Note
T1	I / O	Output	–	–	–	R	R	o	Function output triggered by enable signal
T2	I / O	Output	–	–	–	R	R	o	
T3	I / O	Input	–	–	–	R	R	o	
T4	I / O	Input (int)	–	–	–	R	R	o	
T5	Input	Input (int)	–	–	–	–	–	–	
T6	I / O	I / O	–	–	–	NoR	–	–	Function output triggered by enable signal
T7	I / O	Input	–	–	–	NoR	–	–	
T8	I / O	Input	–	–	–	–	NoR	–	
T9	I / O	I / O	Input	–	–	R	R	o	
T10	I / O	Input	Output	–	–	R	R	o	
T11	I / O	Input	Input	–	–	R	R	o	
T12	I / O	Input	Input(int)	–	–	R	R	o	
T13	I / O	Output	Output	–	–	R	R	o	
T14	I / O	Output	I / O	–	–	R	R	o	
T15	I / O	Input	I / O	Input	–	R	R	o	
T16	I / O	–	–	–	o	R	R	o	
T17	I / O	Input(int)	–	–	o	R	R	o	
T18	I / O	Output	–	–	–	R	–	–	
T19	I / O	Output	–	–	–	NoR	–	–	Function output triggered by enable signal
T20	I / O	Input	–	–	–	NoR	NoR	o	$\overline{\text{BOOT}}$ input enabled during reset
T21	I / O	- (OSC1)	–	–	–	R	R	o	High-speed osscillator (External)

int : Interrupt input
- : Not exist
o : Exist

R: Forced disable during reset
NoR: Unaffected by reset

9.4.7 SCxMOD2 (Mode Control Register 2)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	TBEMP	RBFLL	TXRUN	SBLEN	DRCHG	WBUF	SWRST	
After reset	1	0	0	0	0	0	0	0

10.4.12ADxREG2(Conversion Result Register 2)

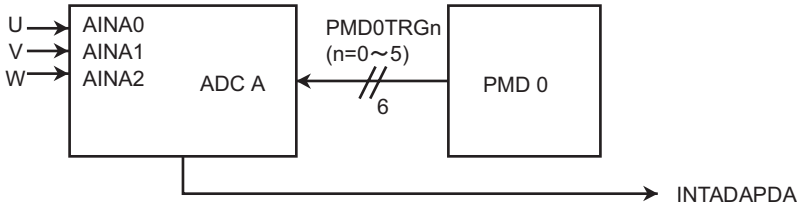
	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	ADR2							
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	ADR2				-	-	OVR2	ADR2RF
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-16	-	R	Read as "0".
15-4	ADR2[11:0]	R	The value of an AD conversion result
3-2	-	R	Read as "0".
1	OVR2	R	OverRun flag 0:No overrun occurred 1:Overrun occurred This flag is set when a new AD conversion result is stored before the value of ADxREG2 is read and is cleared when the low-order byte of ADxREG2 is read.
0	ADR2RF	R	AD conversion result store flag 0:No result stored 1:Result stored <ADR2RF> is a flag that is set when an AD conversion result is stored in the ADxREG2 register and is cleared when the low-order byte of ADxREG2 is read.

10.7 Usage Examples

10.7.1 Successive Conversion Using One PMD0(Three Shunts) and One ADC

The following shows a circuit diagram for AD conversion using one PMD0 for three shunts and one ADC.



Example ADC settings are shown below.

ADC UnitA

Program	0	1	2	3	4	5
reg0	U	V	W	V	W	U
reg1	V	W	U	U	V	W
INT	A	A	A	A	A	A

Programs 0 to 5 are assigned to trigger inputs PMD0TRG0 to 5. "reg0" and "reg1" indicate the PMD Trigger Program Registers ADAPSETn[7:0] and ADAPSETn[15:8]. "U", "V" and "W" indicate the phases of a motor. AIN inputs are selected to obtain these phases.

When a trigger input occurs, AD conversion is performed based on reg0 and reg1 sequentially, and then the interrupt signal (INTADAPDA) is generated.

12.3.4.19VEIDx/VEIQx(d-axis/q-axis Current Registers)

VEIDx

	31	30	29	28	27	26	25	24
bit symbol	ID							
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	ID							
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	ID							
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	ID							
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-0	ID[31:0]	R/W	d-axis current (32-bit fixed-point data: -1.0 to 1.0) d-axis current: 0x0000_0000 to 0xFFFF_FFFF The actual current value is: ID value×Max_I value÷2^{31} Max_I : (Phase current value [A] which corresponds to 1 LSB of ADC)×2^{11}

VEIQx

	31	30	29	28	27	26	25	24
bit symbol	IQ							
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	IQ							
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	IQ							
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	IQ							
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-0	IQ[31:0]	R/W	q-axis current (32-bit fixed-point data: -1.0 to 1.0) q-axis current: 0x0000_0000 to 0xFFFF_FFFF The actual current value is: IQ value×Max_I value÷2^{31} Max_I : (Phase current value [A] which corresponds to 1 LSB of ADC)×2^{11}

12.4.1.1 Schedule Control

The VEACTSCH register is used to select the schedule to be executed.

A schedule is comprised of an output schedule handling output-related tasks and an input schedule handling input-related tasks. Table 12-1 shows the tasks that are executed in each schedule.

The VEMODE register is used to enable or disable phase interpolation, control output operation, and enable or disable zero-current detection as appropriate for each step of the motor control flow (see Table 12-2).

Table 12-1 Tasks To Be Executed in Each Schedule

Schedule Selection VEACTSCH	Output Schedule						Input Schedule		
	Current control	SIN/COS computation	Output coordinate axis conversion	Output phase conversion	Output control	Trigger generation	Input processing	Input phase conversion	Input coordinate axis conversion
0 : Individual execution	(Note1)	(Note1)	(Note1)	(Note1)	(Note1)	(Note1)	(Note1)	(Note1)	(Note1)
1 : Schedule 1	o	o (Note2)	o	o	o (Note3)	o	o(Note4)	o	o
4 : Schedule 4	-	o (Note2)	o	o	o(Note3)	o	o (Note4)	o	o
9 : Schedule 9	-	-	-	-	o (Note3)	o	o(Note4)	-	-

Note 1: Each task is executed only when it is specified.
Note 2: Phase interpolation.
Note 3: Output OFF: <EMGRS>
Note 4: Task operation to be switched by zero-current detection.

Table 12-2 Typical Setting Example

Register Setting / Motor Control Flow	Schedule selection VEACTSCH <VACTn[3:0]>	Task specification VETASKAPP <VTASKn[3:0]>	Phase interpolation VEMODE <PVIEN>	Output control VEMODE <OCRMD[1:0]>	Zero-current detection VEMODE <ZIEN>
Stop	9	0	x	00	0
Initial input	9	0	x	00	1
Positioning	1	5	0	01	0
Forced commutation	1	5	1	01	0
Speed control by current feedback	1	5	1	01	0
Brake	4	6	0	01	0
EMG return	9	0	x	11	0

An output schedule begins executing by the VECPURUNTRG command. When all output-related tasks are completed, the Vector Engine enters a standby state and waits for a start trigger for input-related tasks. At this time, schedules of the other channel can be executed.

An input schedule begins executing by a start trigger. When all input-related tasks are completed, the Vector Engine generates an interrupt to the CPU and enters a halt state. However, if the schedule has its repeat count (VEREPTIME) set to "2" or more, an interrupt is not generated until the schedule is executed the specified number of times.

13.4.2 ENxTNCR(Encoder Input Control Register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	MODE		P3EN
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	CMP	REVERR	UD	ZDET	SFTCAP	ENCLR	ZESEL	CMPEN
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	ZEN	ENRUN	NR		INTEN	ENDEV		
After reset	0	0	0	0	0	0	0	0

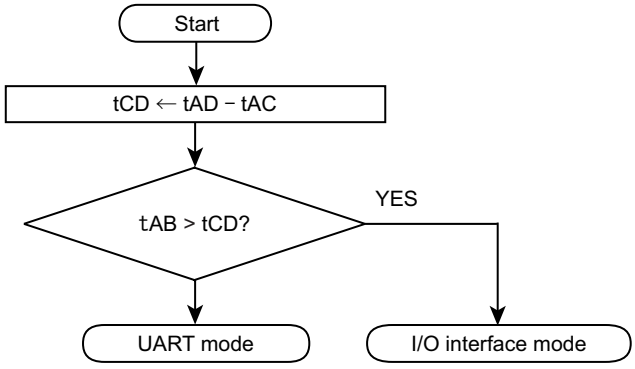


Figure 19-6 Serial Operation Mode Determination Flowchart

19.2.10.5Password

The RAM Transfer command (0x10) causes the boot program to perform password verification. Following an echo-back of the command code, the boot program verifies the contents of the 12-byte password area within the flash memory. The following table shows the password area of each product.

Product name	Area
TMPM370FYDFG/ FYFG	0x3F83_FFF4 to 0x3F83_FFFF

Note: **If a password is set to 0xFF (erased data area), it is difficult to protect data securely due to an easy-to-guess password. Even if Single Boot mode is not used, it is recommended to set a unique value as a password.**

If all these address locations contain the same bytes of data other than 0xFF, a password area error occurs as shown in Figure 19-7. In this case, the boot program returns an error acknowledge (0x11) in response to the checksum byte (the 17th byte), regardless of whether the password sequence sent from the controller is all 0xFFs.

Receiving data (5th to 16th bytes) from the controller is compared to the password stored in the flash memory. All of the 12 bytes must match to pass the password verification. Otherwise, a password error occurs, which causes the boot program to reply an error acknowledge in response to the checksum byte (the 17th byte).

The password verification is performed even if the security function is enabled.

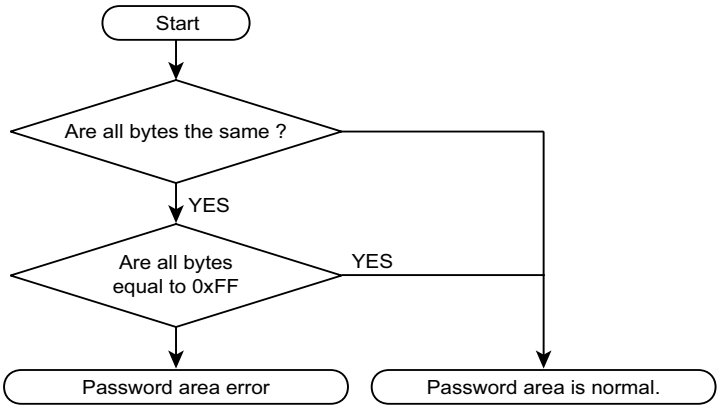


Figure 19-7 Password Area Verification Flowchart

19.2.10.6Checksum Calculation

The checksum byte for a series of bytes of data is calculated by adding the bytes together with ignoring the carries and calculating the 8-bit two's complement by using lower 8 bits. The controller must perform the same checksum operation in transmitting checksum bytes.

Example) To calculate the checksum for a series of 0xE5 and 0xF6:

Add the bytes together

0xE5 + 0xF6 = 0x1DB

Calculate the two's complement by using lower 8 bits, and that is the checksum byte. Then send 0x25 to the controller.

0 - 0xDB = 0x25

19.2.11 General Boot Program Flowchart

Figure 19-8 shows an overall flowchart of the boot program.

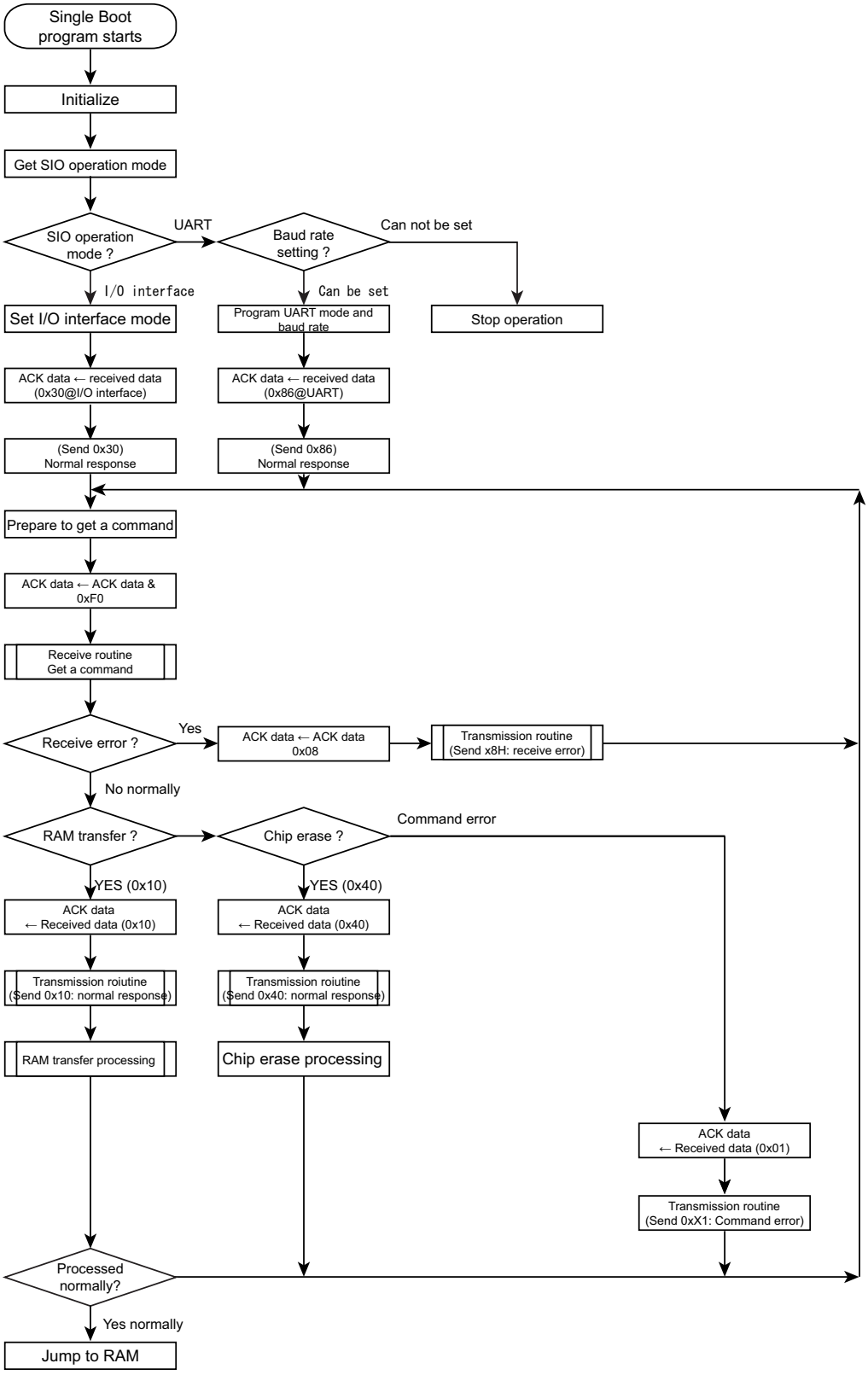


Figure 19-8 Overall Boot Program Flowchart

19.3 On-board Programming of Flash Memory (Rewrite/Erase)

In on-board programming, the CPU is to execute software commands for rewriting or erasing the flash memory. The rewrite/erase control program should be prepared by the user beforehand. Because the flash memory content cannot be read while it is being written or erased, it is necessary to run the rewrite/erase program from the internal RAM after shifting to the user boot mode.

19.3.1 Flash Memory

Except for some functions, writing and erasing flash memory data are in accordance with the standard JEDEC commands.

In writing or erasing, use 32-bit data transfer command of the CPU to enter commands to the flash memory. Once the command is entered, the actual write or erase operation is automatically performed internally.

Table 19-12 Flash Memory Functions

Major functions	Description
Automatic page program	Writes data automatically per page.
Automatic chip erase	Erase the entire area of the flash memory automatically.
Automatic block erase	Erases a selected block automatically.
Protect function	The write or erase operation can be individually inhibited for each block.

19.3.1.1 Block Configuration

(1) TMPM370FYDFG/ FYFG

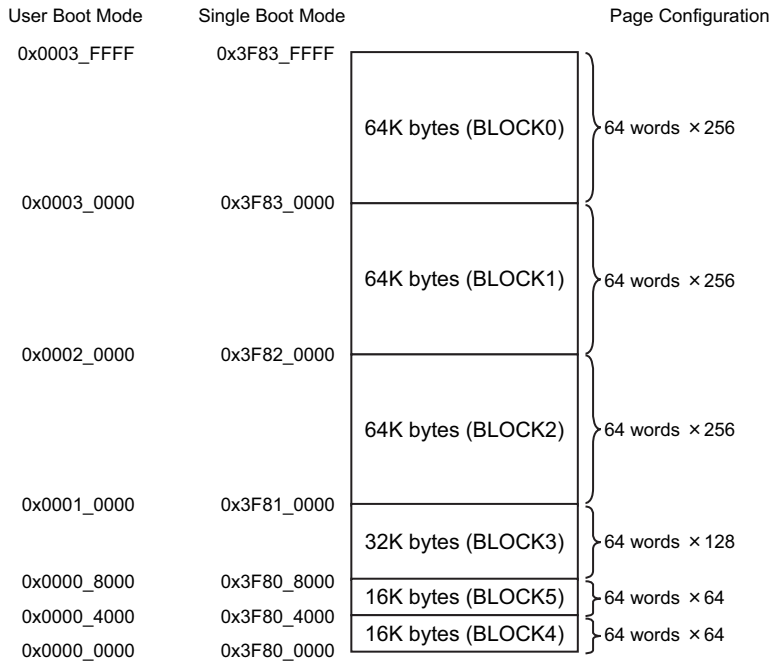


Figure 19-9 Block Configuration of Flash Memory (TMPM370FYDFG / FYFG)

22.3 DC Electrical Characteristics (2/2)

DVDD5 = DVDD5E =RVDD5 = AVDD5A = AVDD5B = AMPVDD5 = 4.5 V to 5.5 V, Ta = −40 to 85 °C

Parameter	Symbol	Rating	Min.	Typ. (Note 1)	Max.	Unit
NORMAL (Note 2) Gear 1/1	I_{DD}	fsys = 80 MHz	−	70	80	mA
IDLE (Note 4) Gear 1/1			−	21	30	
STOP		−	−	7	11	mA

Note 1: Ta=25°C, DVDD5 = DVDD5E = AVDD5A = AVDD5B = RVDD5 = AMPVDD5 = 5V, unless otherwise.

Note 2: I_{DD} NORMAL:
All functions operates excluding A/D, Op amp and Comparator.

Note 3: A/D reference voltage supply can not go into off state.

Note 4: I_{DD} IDLE :
All peripheral functions stopped.

22.7.6 Debug Communication

22.7.6.1 AC measurement condition

- Output levels : High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacitance : CL(TRACECLK) = 25pF, CL(TRACEDATA) = 20pF

22.7.6.2 SWD Interface

Parameter	Symbol	Min.	Max	Unit
CLK cycle	T_{dck}	100	–	ns
DATA hold after CLK rising	T_{d1}	4	–	
DATA valid after CLK rising	T_{d2}	–	37	
DATA valid to CLK rising	T_{ds}	20	–	
DATA hold after CLK falling	T_{dh}	15	–	

22.7.6.3 JTAG Interface

Parameter	Symbol	Min.	Max	Unit
CLK cycle	T_{dck}	100	–	ns
DATA hold after CLK falling	T_{d3}	4	–	
DATA valid after CLK falling	T_{d4}	–	37	
DATA valid to CLK rising	T_{ds}	20	–	
DATA hold after CLK rising	T_{dh}	15	–	

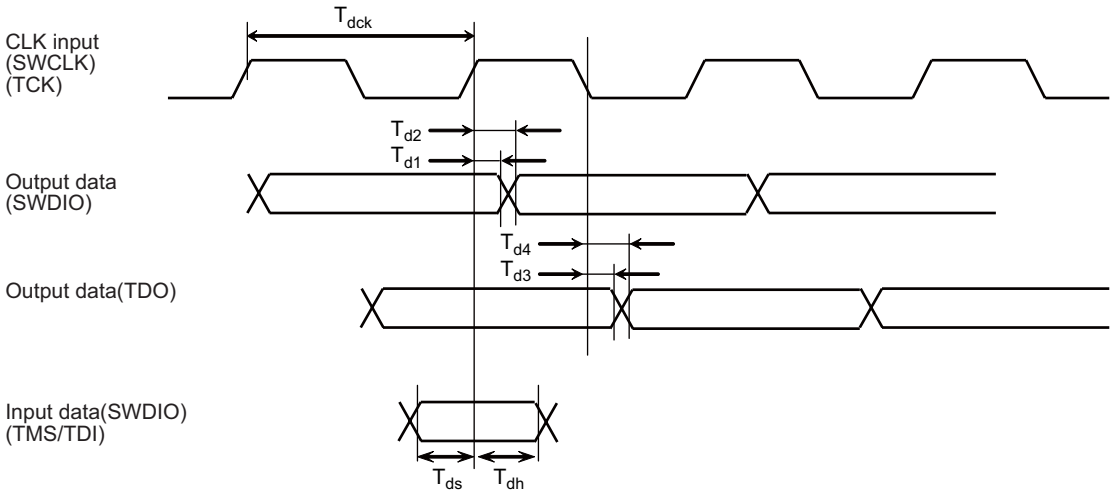


Figure 22-2 JTAG and SWD communication timing