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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	16192
Total RAM Bits	151552
Number of I/O	297
Number of Gates	899000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort8850h-1bm680c

LVDS Reference Clock

The reference clock for the ORT8850 SERDES is an LVDS input (SYS_CLK_[P:N]). This reference clock can run in the range from 63.00 MHz to 106.25 MHz and is used to clock the entire Embedded Core. This clock is also available in the FPGA interface as the output signal FPGA_SYSCLK at the Embedded Core/FPGA Logic interface.

The supported range of reference clock frequencies will drive the internal and link serial rates from 504 MHz to 850 MHz. For standard SONET applications a reference clock rate of 77.76 MHz will allow the ORT8850 to communicate with standard SONET devices. If the ORT8850 is communicating with another ORT8850, the reference clock can run anywhere in the defined range. When using a non 77.76 MHz reference clock, the frame pulse will now need to be derived from the non standard rate thus making the frame pulse rate not 8 kHz, but rather a single clock pulse every 9720 clock cycles.

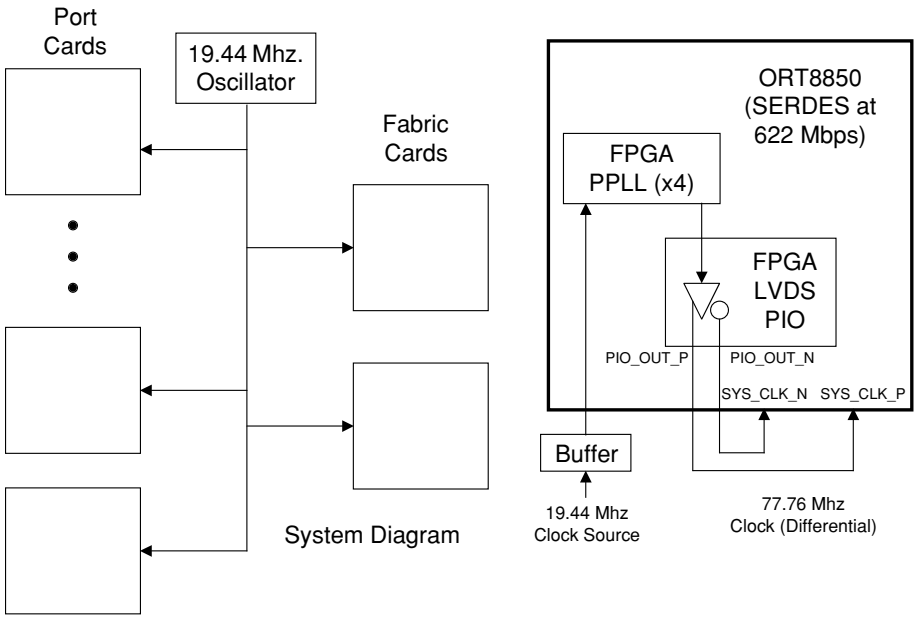
System Considerations for Reference Clock Distribution

There are two main system clocking architectures that can be used with the ORT8850 at the system level to provide the LVDS reference clocks. The recommended approach is to distribute a single reference clock to all boards. However, independent clocks can be used on each board provided that they are matched with sufficient accuracy and the alignment is not used. These two approaches are summarized in the following paragraphs

Distributed Clocking

A distributed clock architecture, shown in Figure 5, uses a single source for the system reference clock. This single source drives all devices on both the line and switch sides of the backplane. Typically this is a lower speed clock such as a 19.44 MHz signal. An external PLL on each board or and internal ORT8850 FPGA PLL is then used to multiply the clock to the desired reference clock rate (i.e. by 4x to 77.76 MHz if the distributed clock is at 19.44 MHz). Using this type of clock architecture the ORT8850 data channels are fully synchronous and no domain transfer is required from the transmitter to the receiver.

Figure 5. Distributed Clock Architecture

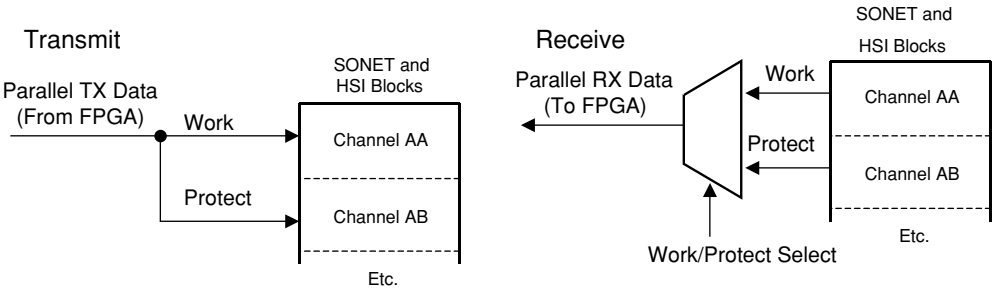


Independent Clocking

An independent clock architecture uses independent clock sources on each ORT8850 board. With this architecture, for the SERDES to sample correctly the independent oscillators must be within reference clock tolerance requirements for the Clock and Data Recovery (CDR) to correctly sample the incoming data and recover data and clock. The local reference clock and the recovered clock will not be synchronous since they are created from a different source. The alignment FIFO uses the recovered clock for write and the local reference clock for read. Due to

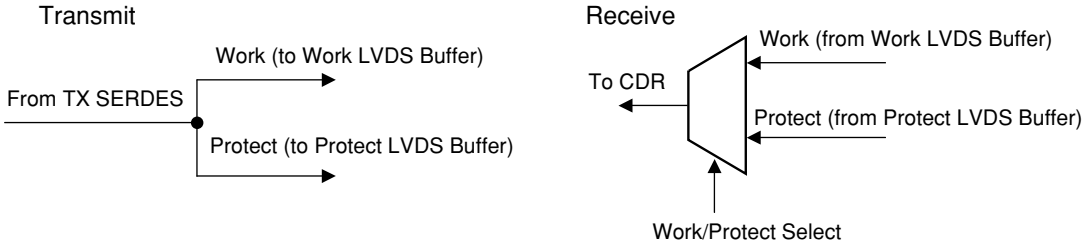
AA. This same scheme is used for channels groupings of AC/AD, BA/BB, and BC/BD. For quad protection when the alignment FIFOs are to be used, the protection switching must be done in FPGA logic.

Figure 9. Parallel Protection Switching



LVDS protection switching (Figure 10) takes place at the LVDS buffer before the serial data is sent into the CDR. The selection is between the main LVDS buffer and the protect LVDS buffer. The main LVDS buffer provide the main receive data on RXDxx_W_[P:N] while the protect LVDS buffers provide protection receive data on RXDxx_P_[P:N]. When operating using the main LVDS buffers (default) no status information is available on the protect LVDS buffers since the serial stream must reach the SONET framer before status information is available on the data stream. The same is also true for the main LVDS buffers when operating with the protect buffers.

Figure 10. LVDS Protection Switching



See Table 17 and Table 18 and the accompanying text for details and register settings for the protection switching options.

FPSC Configuration - Overview

Configuration of the ORT8850 occurs in two stages: FPGA bit stream configuration and embedded core setup.

FPGA Configuration - Overview

Prior to becoming operational, the FPGA goes through a sequence of states, including power-up, initialization, configuration, start-up, and operation. The FPGA logic is configured by the standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet. The options for the embedded core are set via registers that are accessed through the FPGA system bus. The system bus can be driven by an external PPC compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block, that drives the system by using the user interface and uses very little FPGA logic, is available in the *MPI/System Bus* technical note (TN1017). This IP block sets up the embedded core via a state machine and allows the ORT8850 to work in an independent system without an external MicroProcessor Interface.

Embedded Core Setup

All options for the operation of the core are configured according to the memory map shown in Table 19.

During the power-up sequence, the ORT8850 device (FPGA programmable circuit and the core) is held in reset. All the LVDS output buffers and other output buffers are held in 3-state. All Flip-Flops in the core area are in reset state, with the exception of the boundry-scan shift registers, which can only be reset by boundary-scan reset. After power-up reset, the FPGA can start configuration. During FPGA configuration, the ORT8850 core will be held in

passes, the next state will either still be Frame Confirm or will be In Frame. For the framer to declare an In Frame state the framer must detect 4 consecutive correct A1/A2 framing patterns.

This state is similar to the Frame Confirm state except that if the comparison at the A1/A2 time is incorrect, the next state will be the Errored Frame state. If the comparison is correct, the next state will be In Frame. Data is only valid in the Frame state

Errored Frame State
Once the Errored Frame state has been reached, if the next comparison is incorrect, the next state will be OOF i.e., after two transitions are missed, the state machine goes into the OOF state which will also generate an alarm. Otherwise, if the comparison correct, the next state will be In Frame. Also, when the framer detects an errored frame it increments an A1/A2 frame error counter register accessible from the system bus. The counter can be monitored by a processor to compile performance status on the quality of the backplane.

B1 Parity Error Check
The B1 parity error check block receives byte-wide scrambled byte-wide parallel data and a frame sync from the framer. The B1 error check calculation block computes a BIP-8 (bit interleaved parity 8 bits) code, using even parity over all bits of the current STS-12 frame before descrambling.

The same calculation had previous been done for the previous STS-12 frame. The value obtained then is checked against the B1 byte of the current frame after descrambling. A per-stream B1 error counter is incremented for each bit that is in error. The error counter register is accessible from the system bus.

Descrambler
The received streams from the framer are descrambled using a frame synchronous descrambler with the same polynomial ($1 + x^6 + x^7$) that was used in the transmit path. If the incoming data is not scrambled, the descrambling function can be disabled by setting a control register bit (0x3000C). The A1/A2 framing bytes, the section trace byte (C1/J0) and the growth bytes (Z0) are not descrambled.

AIS-L Insertion
The Alarm Indication Signal (AIS) is a continuous stream of unframed 1s sent to alert downstream equipment that the near-end terminal has failed, lost its signal source, or has been temporarily taken out of service. AIS-L is inserted into the received frame by writing all ones for all bytes of the descrambled stream under two conditions:

1. If a force AIS_L state is enabled by a bit in the AIS-L force register, AIS-L is inserted into the received frame continuously. This will cause all bytes within a STS-12 frame to be FF

2. If an AIS-L Insertion on Out-Of-Frame enabled via a register, AIS-L is inserted into the received frame when the framer indicates that an out-of-frame condition exists.

Since this occurs after the overhead processing block, all Transport Overhead can continue to byte read and B1 can still be used to monitor link integrity.

Alignment FIFO and Multi-Channel Alignment
The alignment FIFO in the ORT8850 performs two functions, clock domain transfer and multi-channel alignment. The depth of the alignment FIFO is 10 bit words which allows it to absorb channel timing differences of up to 18 clock cycles. Multi-channel alignment is based on the incoming A1/A2 bytes.

The alignment FIFO is always written from the SONET framer using the per channel recovered clock. The FIFO is always read using the local reference clock (FPGA_SYSCLK). For this reason when doing multi-channel alignment there must be 0 ppm between the transmit ORT8850 reference clock and the receiving ORT8850 reference clock. This can only be accomplished by using a single clock source for both the transmitting and receiving devices.

The alignment FIFO has several alarm and control indicators that are accessible via control and alarm registers available via the system bus or the MPI. The default alignment threshold values for the alignment FIFO are set in registers at 0x3000A and 0x3000B. Here the min and max threshold values can be programmed. The default min is set to 2 clocks and the max default is set to 15. If the alignment FIFO determines that these thresholds have been

condition. It is also possible during operation for the channel to go into OOF. This may occur due to the removal of either the frame pulse or the cable. If this is the case, AND is is part of a multi-channel alignment group, the realignment procedure must be re-executed once the channel goes back into frame.

When a channel goes from the OOF state to the In-Frame state the OOF alarm bit is set per channel. The OOF alarm bit is a per channel bit contained in the channel alarm register. It takes the receiver at least 4 full SONET frames for the state machine to declare the In-Frame state. When the OOF bit is high the channel is in OOF. When the OOF bit changes to a '0' then the channel is back in frame and the realignment procedure should be executed.

Table 11 lists the register values to set up the ORT8850 for alignment FIFO sync realignment. The order is specific. The values are given from the PowerPC point of view. If using the MPI to write data to the ORT8850, the value given in the table is the value that should be used. If using the UMI of the system bus, the data value would need to be byte flipped. The following setup procedures should be followed after the enabled channels have a valid frame pulse, and are in the Frame state:

Table 11. Alignment FIFO Synch Realignment

Register Address	Value (Binary)	Description
0x30020, bit 6	1	Force AIS-L in all channels of the group to be synchronized.
0x30038, bit 6	1	
0x30050, bit 6	1	
0x30068, bit 6	1	
0x30080, bit 6	1	
0x30098, bit 6	1	
0x300B0, bit 6	1	
0x300C8, bit 6	1	
Wait for 4 SONET Frames (~500µs)		
0x30017, specific bits	1	Issue FIFO realignment commands.
0x30018, specific bits	1	
Wait for Another 4 SONET Frames (~500µs)		
0x30017, specific bits	0	Clear FIFO alignment command register bits written in previous steps.
0x30018, specific bits	0	
0x30020, bit 6	0	Release AIS-L in all channels of the group to allow normal data flow through the reveiver.
0x30038, bit 6	0	
0x30050, bit 6	0	
0x30068, bit 6	0	
0x30080, bit 6	0	
0x30098, bit 6	0	
0x300B0, bit 6	0	
0x300C8, bit 6	0	

RX Serial TOH Processing

Transport overhead is extracted from the receive data stream by the TOH extract block. The incoming data gets loaded into a 36-byte shift register on the system clock domain. This, in turn, is clocked onto the TOH clock domain at the start of the SPE time, where it can be clocked out.

The TOH processor is responsible for serializing all received TOH bytes of each channel through that channel's corresponding serial TOH data port. The TOH serial ports are synchronized to the TOH clock (the same clock that is being used by the serial ports on the transmitter side). This free-running TOH clock is provided to the core by external circuitry and operates at a minimum frequency of 25 MHz and a maximum frequency of 77.76 MHz. Data is transferred over serial links in a bursty fashion as controlled by the RX TOH clock enable signal, and is common

Table 13. Valid Starting Positions for and STS MC (Continued)

STS-1 Number	STS-3cSPE	STS-6cSPE	STS-9cSPE	STS-12cSPE	STS-15cSPE	STS-18c to STS-48c SPEs
46	Yes	No	No	No	No	No

Note:
Yes = STS-Mc SPE can start in that STS-1.
No = STS-Mc SPE cannot start in that STS-1.
- = Yes or no, depending on the particular value of M.

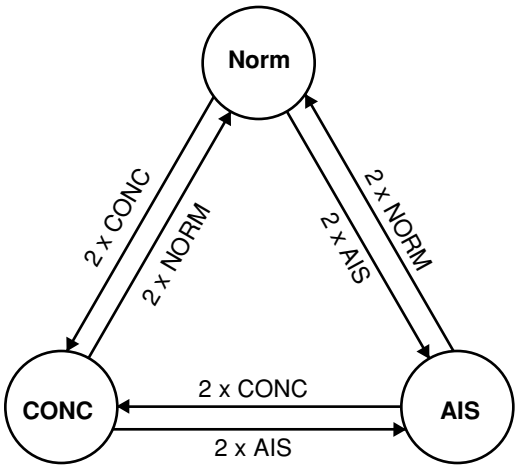
A pointer action byte (H3) is allocated for SPE frequency justification purposes. Frequency justification is discussed in a later section. The H3 byte is used in all STS-1s within an STS-N to carry the extra SPE byte in the event of a negative pointer adjustment. The value contained in this byte when it's not used to carry the SPE byte is undefined.

Pointer Interpreter State Machine.
The pointer interpreter's highest priority is to maintain accurate data flow (i.e., valid SPE only) into the elastic store. This will ensure that any errors in the pointer value will be corrected by a standard, fully SONET compliant, pointer interpreter without any data hits. This means that error checking for increment, decrement, and new data flag (NDF) (i.e., 8 of 10) is maintained in order to ensure accurate data flow. A single valid pointer (i.e., 0-782) that differs from the current pointer will be ignored. Two consecutive incoming valid pointers that differ from the current pointer will cause a reset of the J1 location to the latest pointer value (the generator will then produce an NDF). This block is designed to handle single bit errors without affecting data flow or changing state.

The pointer interpreter has only three states (NORM, AIS, and CONC). NORM state will begin whenever two consecutive NORM pointers are received. If two consecutive NORM pointers that both differ from the current offset are received, then the current offset will be reset to the last received NORM pointer. When the pointer interpreter changes its offset, it causes the pointer generator to receive a J1 value in a new position. When the pointer generator gets an unexpected J1, it resets its offset value to the new location and declares an NDF. The interpreter is only looking for two consecutive pointers that are different from the current value. These two consecutive NORM pointers do not have to have the same value. For example, if the current pointer is ten and a NORM pointer with offset of 15 and a second NORM pointer with offset of 25 are received, then the interpreter will change the current pointer to 25.

If the data is concatenated, the receipt of two consecutive CONC pointers causes CONC state to be entered. Once in this state, offset values from the head of the concatenation chain are used to determine the location of the STS SPE for each STS in the chain. Finally, if two consecutive AIS pointers cause the AIS state to occur. Any two consecutive normal or concatenation pointers will end this AIS state. This state will cause the data leaving the pointer generator to be overwritten with 0xFF.

Figure 22. Pointer Mover State Machine



SPE and C1J1 Identification

In the ORT8850 each frame can be considered as 12 STS-1s. In the SPE region, there are 12 J1 pulses for each STS-1s. There is one C1(J0, new SONET specifications use J0 instead of C1 as section trace to identify each STS-1 in an STS-N) pulse in the TOH area for one frame. Thus, for non concatenated data there are a total of 12 J1 pulses and one C1(J0) pulse per frame. The C1(J0) pulse is coincident with the J0 of STS-1 #1.

The pointer interpreter identifies the payload area of each frame. The SPE flag is active when the data stream is in SPE area. SPE behavior is dependent on pointer movement and concatenation. Note that in the TOH area, H3 can also carry valid data. When valid SPE data is carried in this H3 slot, SPE is high in this particular TOH time slot. In the SPE region, if there is no valid data during any SPE column, the SPE signal will be set to low. SPE allows a pointer processor to extract payload without interpreting the pointers.

Figure 23. SPE and C1J1 Functionality for STS -12

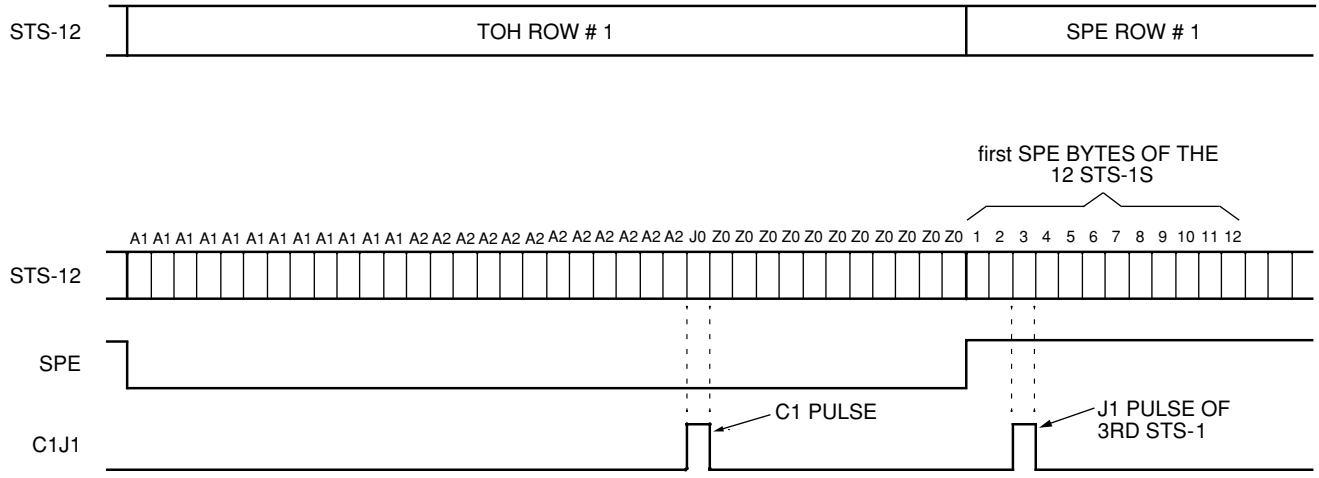
SPE	C1J1	Description
0	0	TOH information excluding C1(J0) of STS-1 #1.
0	1	Position of C1(J0) of STS-1 #1 (one per frame). Typically used to provide a unique link identification (256 possible unique links) to help ensure cards are connected into the backplane correctly or cables are connected correctly.
1	0	SPE information excluding the 12 J1 bytes.
1	1	Position of the 12 J1 bytes.

The following rules are observed for generating SPE and C1J1 signals:

- On occurrence of AIS-P on any of the STS-1, there is no corresponding J1 pulse.
- In case of concatenated payloads (up to STS48c), only the head STS-1 of the group has an associated J1 pulse.
- The C1J1 signal tracks any pointer movements.

This behavior is illustrated in the following figure. Note that the actual bit positions are dependent on the actual payload configuration and offset.

Figure 24. SPE and C1J1 Signals



Pointer Mover

After the pointer interpreter comes the pointer mover block. There is a separate pointer mover for the two SONET framer quads, A and B, each of which handles up to one STS-48 (four channels) The K1/K2 bytes and H1-SS bits are also passed through to the pointer generator so that the FPGA can receive them. The pointer mover handles both concatenations inside the STS-12, and to other STS-12s inside the core. Use of this block is optional, as discussed in a later section.

phases (i.e., received and system) are determined. This latch point is then stable unless the relative framing changes and the received H byte times collide with the system F1 or E2 times, in which case the latch point would be switched to the collision-free byte time.

There is no restriction on how many or how often increments and decrements are processed. Any received increment or decrement is immediately passed to the generator for implementation regardless of when the last pointer adjustment was made. The responsibility for meeting the SONET criteria for maximum frequency of pointer adjustments is left to an upstream pointer processor.

Receive Bypass Options

Not all of the blocks in the receive direction are required to be used. The following bypass options are valid in the receive (backplane → FPGA) direction:

- STM Pointer Mover bypass:
  - In this mode, data from the alignment FIFOs is transferred to the FPGA logic. All channels are synchronous to the FPGA_SYSCLK signals driven to the FPGA logic, as is also the case when the pointer mover is not bypassed. During bypass SPE, C1J1, and data parity signals are not valid. When the pointer mover is bypassed, eight frame pulses (DOUTxx_FP) from aligned channels are provided by the embedded core to the FPGA.
  - When the pointer mover is used, the FPGA logic provides the frame pulse on the LINE_FP (recall: there is only one LINE_FP just like there is only one SYS_FP) signal essential for the Pointer Mover to move the data. The FPGA gets eight channels of SONET data with the A1 byte position of each channel of the TOH arbitrarily offset from the LINE_FP. The DOUTxx_FP signals are not valid when the pointer mover is used.
- STM Pointer Mover and Alignment FIFO bypass:
  - In this mode, data from the framer block is transferred to the FPGA logic. All channels supply data and frame pulses synchronous with their individual recovered clock (CDR_CLK_xx) per channel. During bypass, SPE, C1J1, and data parity signals are not valid. Additionally, no serial TOH_OUT_xx data and frame pulse signals will be available. The DOUTxx_FP signals are aligned with the A1 byte position of each channel, as shown in Figure 26.

Figure 26. Pointer Mover and Alignment FIFO Bypass Timing

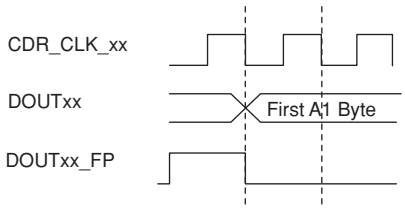


Table 14 shows the register settings to enable the bypass modes.

Table 14. Register Settings for Bypass Mode

Register Address	Value	Description
0x3000C	0x04	Turn off the SONET scrambler/descrambler
0x30020	0x07	Channel AA in functional mode
0x30038	0x07	Channel AB in functional mode
0x30050	0x07	Channel AC in functional mode
0x30068	0x07	Channel AD in functional mode
0x30080	0x07	Channel BA in functional mode
0x30098	0x07	Channel BB in functional mode
0x300B0	0x07	Channel BC in functional mode
0x300C8	0x07	Channel BD in functional mode

Table 16. Operating Modes and Data Paths - SONET Logic Block

Case	Data (Note: xx =[AA, …BD])	Data Path	Embedded Core Clock Launch/Latch	FPGA Clock Launch/Latch	Clock/Route
1	DOUTxx[7:0]	Core to FPGA	Falling Edge	Falling Edge	CDR_CLK_xx/Secondary
2	DOUTxx[7:0]	Core to FPGA	Falling Edge	Rising Edge	FPGA_SYSCLK/Primary
3	DINxx[7:0]	FPGA to Core	Rising Edge	Rising Edge	FPGA_SYSCLK/Primary
4	TOH_OUTxx	Core to FPGA	Rising Edge	Rising Edge	From FPGA/Secondary
5	TOH_INxx	FPGA to Core	Falling Edge	Rising Edge	From FPGA/Secondary

All timing is referenced to the clock signal at the FPGA/Core interface. Data is also timed for signals at the FPGA/Core interface. There will be additional time delays until the interface signals reach the capturing latch. The primary or secondary path delay is controlled, as noted earlier, and the clock timing at the capture latch can be predicted. The data delay, however, may be unique to each interconnect routing.

The timing diagrams provide a quantitative picture of the relative importance of setup and hold margins for the cases discussed. In the diagrams, the launch and capture times and the time difference between the launching and capturing clock edges are identified. As the time between launch and capture increases (up to a full clock period), the possibility of a setup time problem decreases. Also, the possibility of a setup time problem decreases for smaller maximum propagation delay values.

If capture occurs before the next data is launched, a hold time problem cannot occur. In nearly all cases, the difference between the launch and capture clock edges will be nearly a full clock cycle and the data will be captured before the next data is launched. This is not guaranteed, however, and ispLEVER timing analysis should be done for each application.

The general rules used for the FPGA/Core interface are as follows:

1. If possible, transfers across the FPGA/Core interface should be direct register to register transfers with minimal or preferably no intervening logic.

2. Use positive (rising) edge flip-flops in the FPGA for both input and output unless a timing diagram (case 1) explicitly indicates otherwise, or a special case (long routing path, etc.) is being considered.

3. Attempt to ‘locate’ the FPGA side flip-flops reasonably close to the interface unless other timing constraints prevent this. This ‘locate’ is typically achieved by placing a frequency constraint on the FPGA_CLK signal. In most cases, up the 3 ns of data path delay through the FPGA logic in the ORT8850 is acceptable.

4. Pay attention to the clock routing resource recommended (these are fixed on the ORT8850), and to the delay and skew limits and the clock source points.

5. Run Trace setup and hold checks in ispLEVER on the routed design taking the environmental constraints into account. (See ispLEVER Application Note for details).

For the cases where parallel data is output from the core, the reference clock is also output from the core and the effects of propagation delay variation are included in the discussion. Propagation delay is defined relative to the interface signals and thus is the time from the enabling (falling) edge of the clock from the core to the time that data is guaranteed to be valid at the interface. As an example, for the first case discussed, the minimum (tprop_min) and maximum (tprop_max) propagation delays are 0.8 ns. and 4.7 ns. respectively. Therefore the data outputs are stable for 6.1 ns. (10 ns. - 3.9 ns.) of each clock cycle. The data must be captured during this stable period, i.e., the data signals must arrive at the capturing latch with adequate setup and hold margins versus the clock signal at the latch.

In the first case, Figure 27, the alignment FIFO is assumed to be bypassed and all timing is with respect to the recovered clock. The FPGA is latched on the falling edge of the clock, an exception to the general recommenda-

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
3000C	[0:3]	R/W	number of consecutive A1 A2 errors to generate [0:3]	00	If a particular channel's "A1 A2 error insert command" control bit is set to the value 1 then the "A1 and A2 error insert values" will be inserted into that channels respective A1 and A2 bytes. The number of consecutive frames to be corrupted is determined by the "number of consecutive A1 A2 errors to generate [0:3]" control bits. MSB is bit 3
	[4]	R/W	backplane side loopback control	0	0 = No loopback. 1 = RX to TX loopback on backplane side. Serial input is run through SERDES and SONET block, then looped back in parallel to SERDES and out serial.
	[5]	R/W	DINxx/DOUTxx parallel bus parity control	1	0 = Odd parity 1 = Even parity
	[6]	R/W	scrambler/descrambler	1	0 = no RX direction, descramble / TX direction scramble 1 = In RX direction, descramble channel after the SONET frame recovery. In TX direction, scramble data just before parallel-to-serial conversion
	[7]	-	Not Used	0	
3000D	[0:7]	R/W	A1 error insert value [0:7]	00	Value of the A1 byte for error insert
3000E	[0:7]	R/W	A2 error insert value [0:7]	00	Value of the A2 byte for error insert
3000F	[0:7]	R/W	transmit B1 error insert mask [0:7]	00	0 = No error insertion. 1 = Invert corresponding bit in B1 byte.
30010	[0]	R	AA alarm	0	Consolidation alarm for channel AA 1 = alarm 0 = no alarm.
	[1]	R	AB alarm	0	Consolidation alarm for channel AB 1 = alarm 0 = no alarm.
	[2]	R	AC alarm	0	Consolidation alarm for channel AC 1 = alarm 0 = no alarm.
	[3]	R	AD alarm	0	Consolidation alarm for channel AD 1 = alarm 0 = no alarm.
	[4-7]	-	Not Used	0	
30011	[0]	R/W	AA/BA alarm enable/mask register	0	AA and BA enable 1 = enabled 0 = not enabled
	[1]	R/W	AB/BB alarm enable/mask register	0	AB and BB enable 1 = enabled 0 = not enabled
	[2]	R/W	AC/BC alarm enable/mask register	0	AC and BC enable 1 = enabled 0 = not enabled
	[3]	R/W	AD/BD alarm enable/mask register	0	AD and BD enable 1 = enabled 0 = not enabled
	[4-7]	-	Not Used	0	

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
30017	[0]	R/W	BD resync	0	Channel BD alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO. Write “0” for normal operation
	[1]	R/W	BC resync	0	Channel BC alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO. Write “0” for normal operation
	[2]	R/W	BB resync	0	Channel BB alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO. Write “0” for normal operation
	[3]	R/W	BA resync	0	Channel BA alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO. Write “0” for normal operation
	[4]	R/W	AD resync	0	Channel AD alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO.Write “0” for normal operation
	[5]	R/W	AC resync	0	Channel AC alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO.Write “0” for normal operation
	[6]	R/W	AB resync	0	Channel AB alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO.Write “0” for normal operation
	[7]	R/W	AA resync	0	Channel AA alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO.Write “0” for normal operation
30018	[0]	R/W	AD/BD resync	0	2-link AD/BD alignment FIFO resync. Write “1” to resync this link. Write “0” for normal operation.
	[1]	R/W	AC/BC resync	0	2-link AC/BC alignment FIFO resync. Write “1” to resync this link. Write “0” for normal operation.
	[2]	R/W	AB/BB resync	0	2-link AB/BB alignment FIFO resync. Write “1” to resync this link. Write “0” for normal operation.
	[3]	R/W	AA/BA resync	0	2-link AA/BA alignment FIFO resync. Write “1” to resync this link. Write “0” for normal operation.
	[4]	R/W	STM B resync	0	Quad B alignment resync. Write “0” for normal operation.
	[5]	R/W	STM A resync	0	Quad A alignment FIFO resync Write “0” for normal operation.
	[6]	R/W	All 8 resync	0	All 8 channel alignment FIFO resync. Write “0” for normal operation.
	[7]	-	Not Used	N/A	

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
30023* 3003B 30053 3006B 30083 3009B 300B3 300CB	[0]	R/W	A1 A2 error insert command	0	0 = Do not insert error. 1 = Insert error for number of frames in register 0x3000C. The error insertion is based on a rising edge detector. As such, the control must be set to value 0 before trying to indicate a second A1, A2 corruption
	[1]	R/W	B1 error insert command	0.	0 = Do not insert error 1 = Insert error marked in register 0x3000F. The error insertion is based on a rising edge detector. As such, the control must be set to value 0 before trying to initiate a second B1 corruption.
	[2]	R/W	disable B1 insert	0	0 = B1 is inserted in the transmit direction by the SONET block 1 = B1 is not inserted in the transmit direction
	[3]	R/W	disable A1/A2 insert	0	0 = A1/A2 is inserted in the transmit direction by the SONET block 1 = A1/A2 is not inserted in the transmit direction
	[4-7]	-	Not Used	0	
30024* 3003C 30054 3006C 30084 3009C 300B4 300CC	[0:3]	R	concat indication 3, 6, 9, 12	0	The value 1 in any bit location indicates that STS# is in CONCAT mode. 0 = Not in concatenation mode or is the head of concatenated group 1 = indicates the channel is concatenated
	[4-7]	-	Not Used	0	
30025* 3003D 30055 3006D 30085 3009D 300B5 300CD	[0:7]	R	concat indication 1, 4, 7, 10, 2, 5, 8, 11	0	The value 1 in any bit location indicates that STS# is in CONCAT mode. 0 = Not in concatenation mode or is the head of concatenated group 1 = indicates the channel is concatenated
30026* 3003E 30056 3006E 30086 3009E 300B6 300CE	[0]	R	Channel alarm bit	0	Set when any of the alarms in the channel alarm register (0x30028) are set and the alarm is enabled. This alarm is enabled in 0x30027 bit 0 for channel AA etc.
	[1]	R	AIS-P flag	0	Set when any alarm for AIS-P is set and the corresponding enable is set.
	[2]	R	Pointer mover elastic store overflow flag	0	Set when the elastic store in the pointer mover write and read address is within 1 byte. Alarm enable is 0x30027 bit 2.
	[3-7]	-	Not Used	0	

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
30027* 0303F 30057 3006F 30087 3009F 300B7 300CF	[0]	R/W	enable channel alarm	0	Channel alarm bit (30026, ...) enable. Set to 1 to enable alarm bit to propagate to alarm 0x30010
	[1]	R/W	enable AIS-P flag	0	AIS -P flag alarm enable. Set to 1 to enable alarm bit to propagate to alarm 0x30010
	[2]		enable pointer mover elastic store overflow flag	0	Pointer mover elastic store overflow flag enable. Set to 1 to enable alarm bit to propagate to 0x30010
	[3-7]	-	Not Used	0	
30028* 30040 30058 30070 30088 300A0 300B8 300D0	[0]	R	FIFO aligner threshold error flag	00	Alarm is set to 1 if either the min or max FIFO threshold levels are violated, the min and max threshold levels can be set in address 0x3000A and 0x300B. Alarm enable is 0x30029 bit 0. Write 1 to clear this alarm bit This alarm is only valid when FIFO OOS flag is also set.
	[1]		RX internal path parity error flag		Alarm indicator on receive path internal parity error. Alarm is enabled in 0x30029 bit 1. Write 1 to clear
	[2]		OOF flag		Alarm indicator channel is OOF. Alarm enable is 0x30029 bit 2. Write 1 to clear.
	[3]		LVDS link B1 parity error flag		Alarm indicator that channel has found a B1 parity error. Alarm enable is 0x30029 bit 3. Write 1 to clear.
	[4]		DINxx parallel bus parity error flag	0	Alarm indicator channel has found a parity error on the DINxx input from the FPGA.Alarm enable is 0x30029 bit 4. Write 1 to clear.
	[5]		TOH serial input port parity error flag	0	Alarm indicator channel has found a parity error on the TOH_INxx input from the FPGA. Write 1 to clear this alarm. Alarm enable is 0x30028 bit 5.
	[6]		FIFO OOS error flag	0	Alarm indicates channel group is out of sync. Write 1 to clear. Alarm enable is 0x30028.
	[7]	-	Not Used	0	
30029* 30041 30059 30071 30089 300A1 300B9 300D1	[0:6]	R/W	channel alarm enable	00	Enable bits for channel alarm register 0x30028. Set to 1 to enable and to propagate the alarm to register 0x30026 bit 0.
	[7]	-	Not Used	0	
3002A* 30042 3005A 30072 3008A 300A2 300BA 300D2	[0:3]	R	AIS alarm flags 3, 6, 9, 12	0	These are the AIS-P alarm flags. 1 if the LVDS input STS # contains AIS.
	[4-7]	-	Not Used	0	

Electrical Characteristics

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The *ORCA* Series 4 FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Table 20. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_{stg}	-65	150	°C
Power Supply Voltage with Respect to Ground	V_{DD33}[2]	-0.3	4.2	V
	V_{DDIO}	-0.3	4.2	V
	V_{DD15}	-0.3	2.0	V
	V_{DDA_STM}[1]	-0.3	2.0	V
Input Signal with Respect to Ground	—	-0.3	V_{DDIO} + 0.3	V
Signal Applied to High-impedance Output	—	-0.3	V_{DDIO} + 0.3	V
Maximum Package Body (Soldering) Temperature	—	—	220	°C

Recommended Operating Conditions

Table 21. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage with Respect to Ground*	V_{DD33}[2]	2.7	3.6	V
	V_{DD15}	1.425	1.575	V
	V_{DDA_STM}[1]	1.425	1.575	V
Input Voltages	V_{IN}	-0.3	V_{DDIO} + 0.3	V
Junction Temperature	T_J	-40	125	°C

For FPGA Recommended Operating Conditions and Electrical Characteristics, see the Recommended Operating Conditions and Electrical Characteristics tables in the ORCA Series 4 FPGA data sheet (ORT8850L: OR4E02, ORT8850H: OR4E06) and the ORCA Series 4 I/O Buffer Technical Note. FPSC Standby Currents (I_{DD}SB15 and I_{DD}SB33) are tested with the Embedded Core in the powered down state.

Notes:
1. V_{DDA_STM} is an analog power supply input which needs to be isolated from other power supplies on the board.
2. V_{DD33} is an analog power supply for the FPGA PLLs and needs to be isolated from other power supplies on the board.

HSI Electrical and Timing Characteristics

Table 22. Maximum Power Dissipation

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Dissipation	SERDES, scrambler/descrambler, framer, FIFO alignment, pointer mover, and I/O (per channel), 622 Mbtis/s	—	—	125	mW

1. With all channels operating, 1.575 V and 3.6 V supplies, 85ºC.

Table 23. Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{DD}15$ Supply Voltage	—	1.425	—	1.575	V
Junction Temperature	T_J	–40	—	125	°C

Table 24. Receiver Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Data					
Stream of Nontransitions [1]	—	—	—	72	bits
Phase Change, Input Signal	Over a 200 ns time interval [2]	—	—	100	ps
Eye Opening[3]	—	0.4	—	—	UIp-p
Jitter Tolerance @ 622 Mbits/s, Worst Case	300 MV diff eye[4]	—	—	0.6	UIp-p
Jitter Tolerance @ 155 Mbits/s, Worst Case	250 MV diff eye[5]	—	—	0.85	UIp-p

1. This sequence should not occur more than once per minute.
2. Translates to a frequency change of 500 ppm.
3. A unit interval for 622.08 Mbits/s data is 1.6075 ns.
4. With STS-12 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., TA=0°C to 85°C, 1.425 V to 1.575 V supply. Jitter measured with a Wavecrest SIA-3000.
5. With STS-3 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., TA=0°C to 85°C, 1.425 V to 1.575 V supply. Jitter measured with a Wavecrest SIA-3000.

Table 32. FPGA Common-Function Pin Descriptions (Continued)

Symbol	I/O	Description
$\overline{\text{MPI\_BDIP}}$	I	$\overline{\text{MPI\_BDIP}}$ is driven by the *PowerPC* processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	O	During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_ACK	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_CLK	I	This is the *PowerPC* synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the embedded system bus. If MPI is used this will be the *AMBA* bus clock.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_TEA	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_RTRY	O	This pin requests the MPC860 to relinquish the bus and retry the cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
D[0:31]	I/O	Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{\text{WR}}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	O	D[7:3] output internal status for asynchronous peripheral mode when $\overline{\text{RD}}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.*
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.*
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.*
TESTCFG	I	During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user programmable I/O pin.*
LVDS_R	—	Reference resistor connection for controlled impedance termination of Series 4 FPGA LVDS inputs.

1. The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
AK12	6 (BL)	9	IO	PB8A	PB13A	—	L23T_D3
AP9	6 (BL)	9	IO	PB8B	PB13B	—	L23C_D3
AL31	—	—	VSS	VSS	VSS	—	—
AN10	6 (BL)	9	IO	PB8C	PB13C	D23	L24T_D1
AL12	6 (BL)	9	IO	PB8D	PB13D	D24	L24C_D1
AM11	6 (BL)	9	IO	PB9A	PB14A	—	L25T_D1
AP10	6 (BL)	9	IO	PB9B	PB14B	—	L25C_D1
AP3	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AK13	6 (BL)	9	IO	PB9C	PB14C	VREF_6_09	L26T_D2
AN11	6 (BL)	9	IO	PB9D	PB14D	D25	L26C_D2
AL13	6 (BL)	9	IO	PB10A	PB15C	—	L27T_D0
AK14	6 (BL)	9	IO	PB10B	PB15D	—	L27C_D0
AM3	—	—	VSS	VSS	VSS	—	—
AN12	6 (BL)	10	IO	PB10C	PB16C	D26	L28T_D1
AL14	6 (BL)	10	IO	PB10D	PB16D	D27	L28C_D1
AP12	6 (BL)	10	IO	PB11A	PB17C	—	L29T_D0
AN13	6 (BL)	10	IO	PB11B	PB17D	—	L29C_D0
AP13	6 (BL)	10	IO	PB11C	PB18C	VREF_6_10	L30T_D3
AK15	6 (BL)	10	IO	PB11D	PB18D	D28	L30C_D3
AL15	6 (BL)	11	IO	PB12A	PB19C	D29	L31T_D0
AK16	6 (BL)	11	IO	PB12B	PB19D	D30	L31C_D0
AM13	—	—	VSS	VSS	VSS	—	—
AP14	6 (BL)	11	IO	PB12C	PB20C	VREF_6_11	L32T_D2
AL16	6 (BL)	11	IO	PB12D	PB20D	D31	L32C_D2
AN15	5 (BC)	1	IO	PB13C	PB21A	—	—
AP15	5 (BC)	1	IO	PB14A	PB21C	—	L1T_D3
AK17	5 (BC)	1	IO	PB14B	PB21D	—	L1C_D3
Y15	—	—	VSS	VSS	VSS	—	—
AM16	5 (BC)	1	IO	PB14C	PB22A	—	—
AN16	5 (BC)	1	IO	PB15A	PB22C	VREF_5_01	L2T_D1
AL17	5 (BC)	1	IO	PB15B	PB22D	—	L2C_D1
AM12	5 (BC)	—	VDDIO5	VDDIO5	VDDIO5	—	—
AP16	5 (BC)	2	IO	PB15C	PB23A	—	L3T_D1
AM17	5 (BC)	2	IO	PB15D	PB23B	—	L3C_D1
AN17	5 (BC)	2	IO	PB16A	PB23C	PBCK0T	L4T_D1
AL18	5 (BC)	2	IO	PB16B	PB23D	PBCK0C	L4C_D1
AN18	5 (BC)	2	IO	PB16C	PB24A	—	L5T_A0
AM18	5 (BC)	2	IO	PB16D	PB24B	—	L5C_A0
AN19	5 (BC)	2	IO	PB17A	PB24C	VREF_5_02	L6T_D2
AK18	5 (BC)	2	IO	PB17B	PB24D	—	L6C_D2
Y20	—	—	VSS	VSS	VSS	—	—
AM19	5 (BC)	2	IO	PB17C	PB25C	—	L7T_A0

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
P13	—	—	VSS	VSS	VSS	—	—
AL25	—	—	O	TXDAC_P_N	TXDAC_P_N	—	L3N_A0
AL26	—	—	O	TXDAC_P_P	TXDAC_P_P	—	L3P_A0
B32	—	—	VDD33	VDD33	VDD33	—	—
AM26	—	—	O	TXDAD_P_N	TXDAD_P_N	—	L4N_A0
AM27	—	—	O	TXDAD_P_P	TXDAD_P_P	—	L4P_A0
P14	—	—	VSS	VSS	VSS	—	—
AN28	—	—	O	Reserved	Reserved	—	L5N_D0
AP29	—	—	O	Reserved	Reserved	—	L5P_D0
C31	—	—	VDD33	VDD33	VDD33	—	—
AL27	—	—	O	TXCLK_P_N	TXCLK_P_N	—	L6N_A0
AK27	—	—	O	TXCLK_P_P	TXCLK_P_P	—	L6P_A0
P15	—	—	VSS	VSS	VSS	—	—
AL28	—	—	O	TXDBA_P_N	TXDBA_P_N	—	L7N_A0
AK28	—	—	O	TXDBA_P_P	TXDBA_P_P	—	L7P_A0
C33	—	—	VDD33	VDD33	VDD33	—	—
AM28	—	—	O	TXDBB_P_N	TXDBB_P_N	—	L8N_D0
AN29	—	—	O	TXDBB_P_P	TXDBB_P_P	—	L8P_D0
P20	—	—	VSS	VSS	VSS	—	—
AL29	—	—	O	TXDBC_P_N	TXDBC_P_N	—	L9N_A0
AK29	—	—	O	TXDBC_P_P	TXDBC_P_P	—	L9P_A0
C34	—	—	VDD33	VDD33	VDD33	—	—
AP30	—	—	O	TXDBD_P_N	TXDBD_P7_N	—	L10N_D0
AN30	—	—	O	TXDBD_P_P	TXDBD_P_P	—	L10P_D0
P21	—	—	VSS	VSS	VSS	—	—
AM29	—	—	I	DAUTREC	DAUTREC	—	—
AP31	—	—	I	TSTCLK	TSTCLK	—	—
D32	—	—	VDD33	VDD33	VDD33	—	—
AM30	—	—	I	TESTRST	TESTRST	—	—
AN31	—	—	I	TSTSHFTLD	TSTSHFTLD	—	—
P22	—	—	VSS	VSS	VSS	—	—
R13	—	—	VSS	VSS	VSS	—	—
R14	—	—	VSS	VSS	VSS	—	—
E30	—	—	VDD33	VDD33	VDD33	—	—
AL30	—	—	I	RESETTX	RESETTX	—	—
E31	—	—	VDD33	VDD33	VDD33	—	—
AH30	—	—	I	ETOGGLE	ETOGGLE	—	—
AJ30	—	—	I	ELSEL	ELSEL	—	—
R15	—	—	VSS	VSS	VSS	—	—
AL33	—	—	I	EXDNUP	EXDNUP	—	—
AH31	—	—	I	MRESET	MRESET	—	—
L34	—	—	VDD33	VDD33	VDD33	—	—

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
C11	0 (TL)	2	IO	PT9A	PT13C	MPI_TEA_N	L6T_D0
B10	0 (TL)	3	IO	PT8D	PT12D	—	L7C_D0
A9	0 (TL)	3	IO	PT8C	PT12C	—	L7T_D0
C10	0 (TL)	3	IO	PT8B	PT11D	VREF_0_03	L8C_D0
B9	0 (TL)	3	IO	PT8A	PT11C	—	L8T_D0
A8	0 (TL)	3	IO	PT7D	PT10D	D0	L9C_D2
D10	0 (TL)	3	IO	PT7C	PT10C	TMS	L9T_D2
B1	—	—	VSS	VSS	VSS	—	—
C9	0 (TL)	4	IO	PT7B	PT9D	A20/MPI_BDIP_N	L10C_D0
B8	0 (TL)	4	IO	PT7A	PT9C	A19/MPI_TSZ1	L10T_D0
A7	0 (TL)	4	IO	PT6D	PT8D	A18/MPI_TSZ0	L11C_D4
E12	0 (TL)	4	IO	PT6C	PT8C	D3	L11T_D4
B3	0 (TL)	—	VDDIO0	VDDIO0	VDDIO0	—	—
D9	0 (TL)	4	IO	PT6B	PT7D	VREF_0_04	L12C_D0
C8	0 (TL)	4	IO	PT6A	PT7C	—	L12T_D0
E11	0 (TL)	5	IO	PT5D	PT6D	D1	L13C_D3
B7	0 (TL)	5	IO	PT5C	PT6C	D2	L13T_D3
B2	—	—	VSS	VSS	VSS	—	—
A6	0 (TL)	5	IO	PT5B	PT5D	—	L14C_D2
D8	0 (TL)	5	IO	PT5A	PT5C	VREF_0_05	L14T_D2
C7	0 (TL)	5	IO	PT4D	PT4D	TDI	L15C_D1
A5	0 (TL)	5	IO	PT4C	PT4C	TCK	L15T_D1
C1	0 (TL)	—	VDDIO0	VDDIO0	VDDIO0	—	—
E10	0 (TL)	5	IO	PT4B	PT4B	—	L16C_D2
D7	0 (TL)	5	IO	PT4A	PT4A	—	L16T_D2
A4	0 (TL)	6	IO	PT3D	PT3D	—	L17C_D4
E9	0 (TL)	6	IO	PT3C	PT3C	VREF_0_06	L17T_D4
B33	—	—	VSS	VSS	VSS	—	—
B6	0 (TL)	6	IO	PT3B	PT3B	—	L18C_A0
C6	0 (TL)	6	IO	PT3A	PT3A	—	L18T_A0
B5	0 (TL)	6	IO	PT2D	PT2D	PLL_CK1C/PPLL	L19C_D1
D6	0 (TL)	6	IO	PT2C	PT2C	PLL_CK1T/PPLL	L19T_D1
C2	0 (TL)	—	VDDIO0	VDDIO0	VDDIO0	—	—
C5	0 (TL)	6	IO	PT2B	PT2B	—	L20C_D0
B4	0 (TL)	6	IO	PT2A	PT2A	—	L20T_D0
E8	—	—	O	PCFG_MPI_IRQ	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	—

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
P17	—	—	VDD15	VDD15	VDD15	—	—
P18	—	—	VDD15	VDD15	VDD15	—	—
N16	—	—	VDD15	VDD15	VDD15	—	—
N17	—	—	VDD15	VDD15	VDD15	—	—
N18	—	—	VDD15	VDD15	VDD15	—	—
N19	—	—	VDD15	VDD15	VDD15	—	—
P16	—	—	VDD15	VDD15	VDD15	—	—
P19	—	—	VDD15	VDD15	VDD15	—	—
R16	—	—	VDD15	VDD15	VDD15	—	—
R17	—	—	VDD15	VDD15	VDD15	—	—
R18	—	—	VDD15	VDD15	VDD15	—	—
R19	—	—	VDD15	VDD15	VDD15	—	—
T13	—	—	VDD15	VDD15	VDD15	—	—
T14	—	—	VDD15	VDD15	VDD15	—	—
T15	—	—	VDD15	VDD15	VDD15	—	—
T20	—	—	VDD15	VDD15	VDD15	—	—
T21	—	—	VDD15	VDD15	VDD15	—	—
U13	—	—	VDD15	VDD15	VDD15	—	—
U14	—	—	VDD15	VDD15	VDD15	—	—
U15	—	—	VDD15	VDD15	VDD15	—	—
U20	—	—	VDD15	VDD15	VDD15	—	—
U21	—	—	VDD15	VDD15	VDD15	—	—
V13	—	—	VDD15	VDD15	VDD15	—	—
V14	—	—	VDD15	VDD15	VDD15	—	—
V15	—	—	VDD15	VDD15	VDD15	—	—
V20	—	—	VDD15	VDD15	VDD15	—	—
V21	—	—	VDD15	VDD15	VDD15	—	—
W13	—	—	VDD15	VDD15	VDD15	—	—
W14	—	—	VDD15	VDD15	VDD15	—	—
W15	—	—	VDD15	VDD15	VDD15	—	—
W20	—	—	VDD15	VDD15	VDD15	—	—
W21	—	—	VDD15	VDD15	VDD15	—	—
Y17	—	—	VDD15	VDD15	VDD15	—	—
Y18	—	—	VDD15	VDD15	VDD15	—	—
Y19	—	—	VDD15	VDD15	VDD15	—	—
AA16	—	—	VDD15	VDD15	VDD15	—	—
AA17	—	—	VDD15	VDD15	VDD15	—	—
AA18	—	—	VDD15	VDD15	VDD15	—	—
AA19	—	—	VDD15	VDD15	VDD15	—	—
AB16	—	—	VDD15	VDD15	VDD15	—	—
AB17	—	—	VDD15	VDD15	VDD15	—	—
AB18	—	—	VDD15	VDD15	VDD15	—	—

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: θ_{JA}, ψ_{JC}, and θ_{JC}. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

θJA

This is the thermal resistance from junction to ambient (theta-JA, R-theta, etc.).

$$\theta_{JA} = \frac{T_J - T_A}{Q} \quad (1)$$

where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, θJA is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that θJA is expressed in units of °C/watt.

ΨJC

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance, and it is defined by:

$$\Psi_{JC} = \frac{T_J - T_C}{Q} \quad (2)$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the θJA measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψJC is also expressed in units of °C/W.

θJC

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\theta_{JC} = \frac{T_J - T_C}{Q} \quad (3)$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates θJC from ψJC. θJC is a true thermal resistance and is expressed in units of °C/W.

θJB

This is the thermal resistance from junction to board (ΘJL). It is defined by:

$$\theta_{JB} = \frac{T_J - T_B}{Q} \quad (4)$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads. Note that θJB is expressed in units of °C/W and that this parameter and the way it is measured are still being discussed by the JEDEC committee.