Lattice Semiconductor Corporation - ORT8850H-2BM680C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	16192
Total RAM Bits	151552
Number of I/O	297
Number of Gates	899000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort8850h-2bm680c

- New 200 MHz embedded quad-port RAM blocks, two read ports, two write ports, and two sets of byte lane enables. Each embedded RAM block can be configured as:
  - One—512 x 18 (quad-port, two read/two write) with optional built-in arbitration.
  - One—256 x 36 (dual-port, one read/one write).
  - One—1K x 9 (dual-port, one read/one write).
  - Two—512 x 9 (dual-port, one read/one write for each).
  - Two RAM with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - Supports joining of RAM blocks.
  - Two 16 x 8-bit Content Addressable Memory (CAM) support.
  - FIFO 512 x 18, 256 x 36, 1K x 9, or dual 512 x 9.
  - Constant multiply (8 x 16 or 16 x 8).
  - Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, MicroProcessor Interface (MPI), embedded RAM blocks, and embedded backplane transceiver blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.
- Built-in testability:
  - Full boundary scan (*IEEE* 1149.1 and Draft 1149.2 JTAG).
  - Programming and readback through boundary scan port compliant to *IEEE* Draft 1532:D1.7.
  - TS_ALL testability function to 3-state all I/O pins.
  - New temperature-sensing diode.
- Cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also supports compliance with many setup/hold and clock to out I/O specifications and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved *PowerPC/Power QUICC MPC860* and *PowerPC* II *MPC8260* high-speed synchronous MicroProcessor Interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded backplane transceiver blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space provided.
- New embedded *AMBA*™ specification 2.0 AHB system bus (*ARM*® processor) facilitates communication among the MicroProcessor Interface, configuration logic, embedded block RAM, FPGA logic, and backplane transceiver logic.
- New network PLLs meet ITU-T G.811 specifications and provide clock conditioning for DS-1/E-1 and STS-3/STM-1 applications.
- Variable size bused readback of configuration data capability with the built-in MicroProcessor Interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E04).
- New local clock routing structures allow creation of localized clock trees.
- Two new edge clock routing structures allow up to six high-speed clocks on each edge of the device for improved setup/hold and clock-to-out performance.
- New Double-Data Rate (DDR) and Zero-Bus Turn-around (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced speed internal logic.

- Meets Universal Test and Operations PHY Interface for ATM (UTOPIA) Levels 1, 2, and 3. Also meets proposed specifications for UTOPIA Level 4 POS-PHY, Level 3 (2.5 Gbits/s), and POS-PHY 4 (10 Gbits/s) interface standards for Packet-over-SONET as defined by the Saturn Group.
- ispLEVER development system software. Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.

Description

What is an FPSC?

FPSCs, or Field Programmable System-on-a-Chip devices, are devices that combine field-programmable logic with ASIC or mask-programmed logic on a single device. FPSCs provide the time to market and the flexibility of FPGAs, the design effort savings of using soft Intellectual Property (IP) cores, and the speed, design density, and economy of ASICs.

FPSC Overview

Lattice's Series 4 FPSCs are created from Series 4 *ORCA* FPGAs. To create a Series 4 FPSC, several columns of Programmable Logic Cells (see FPGA Logic Overview section for FPGA logic details) are added to an embedded logic core. Other than replacing some FPGA gates with ASIC gates, at greater than 10:1 efficiency, none of the FPGA functionality is changed—all of the Series 4 FPGA capability is retained: embedded block RAMs, MPI, PCMs, boundary scan, etc. Columns of programmable logic are replaced on one side of the device, allowing pins from the replaced columns to be used as I/O pins for the embedded core. The remainder of the device pins retain their FPGA functionality.

FPSC Gate Counting

The total gate count for an FPSC is the sum of its embedded core (standard-cell/ASIC gates) and its FPGA gates. Because FPGA gates are generally expressed as a usable range with a nominal value, the total FPSC gate count is sometimes expressed in the same manner. Standard-cell ASIC gates are, however, 10 to 25 times more silicon-area efficient than FPGA gates. Therefore, an FPSC with an embedded function is gate equivalent to an FPGA with a much larger gate count.

FPGA/Embedded Core Interface

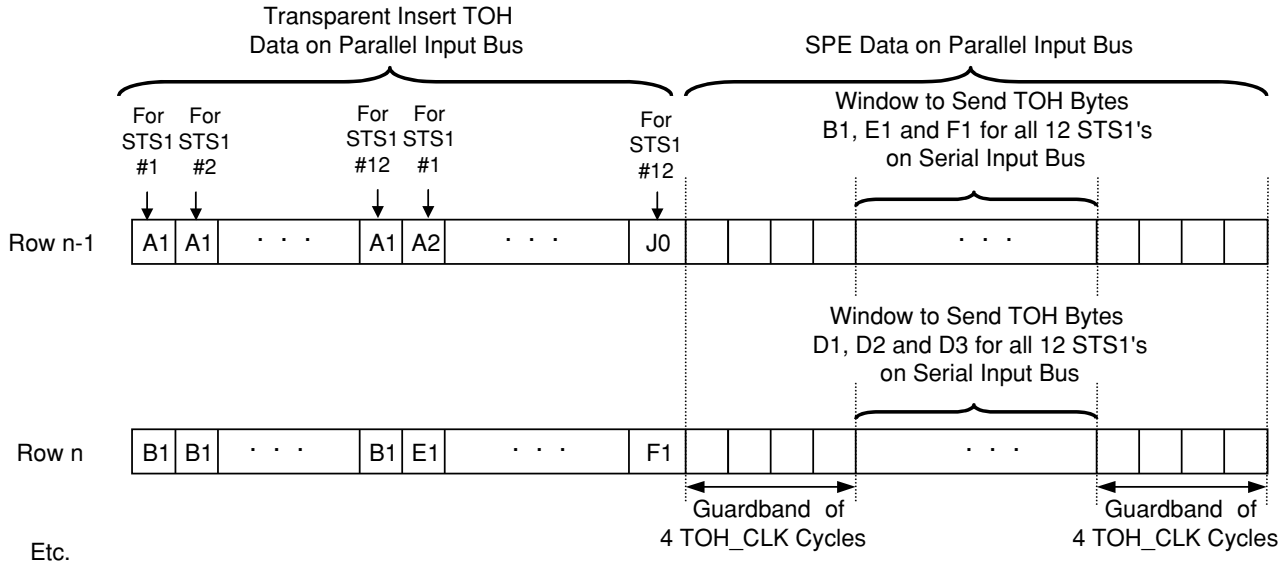
The interface between the FPGA logic and the embedded core has been enhanced to provide a greater number of interface signals than on previous FPSC architectures. Compared to bringing embedded core signals off-chip, this on-chip interface is much faster and requires less power.

Series 4 based FPSCs expand this interface by providing a link between the embedded block and the multi-master 32-bit system bus in the FPGA logic. This system bus allows the core easy access to many of the FPGA logic functions including the embedded block RAMs and the MicroProcessor Interface.

Clock spines also can pass across the FPGA/embedded core boundary. This allows fast, low-skew clocking between the FPGA and the embedded core. Many of the special signals from the FPGA, such as DONE and global set/reset, are also available to the embedded core, making it possible to fully integrate the embedded core with the FPGA as a system.

For even greater system flexibility, FPGA configuration RAMs are available for use by the embedded core. This supports user-programmable options in the embedded core, in turn allowing greater flexibility. Multiple embedded core configurations may be designed into a single device with user-programmable control over which configurations are implemented, as well as the capability to change core functionality simply by reconfiguring the device.

Figure 15. TOH Serial Port Input Framing Signals (FPGA to Core)



Although all TOH bytes from the 12 STS-1s are transferred into the device from each serial port, not all of them get inserted in the frame. There are three hard coded exceptions to the TOH byte insertion:

- Framing bytes (A1/A2 of all STS-1s) are not inserted from the serial input bus. Instead, they can always be regenerated.
- Parity byte (B1 of STS#1) is not inserted from the serial input bus. Instead, it is always recalculated (the 11 bytes following B1 are replaced with all zeros).
- Pointer bytes (H1/H2/H3 of all STS-1s) are not inserted from the serial input bus. Instead, they always flow transparently from parallel input to LVDS output.

Except for the above hardcode exceptions, the source of some TOH bytes can be controlled by bits in the control registers. The 12 STS-1 bytes forming a single STS-12 TOH header block are controlled as a whole. When configured to be in the transparent mode, the specific bytes must flow transparently from the parallel input. The 15 overhead bytes that can be controlled on a per STS-1 basis are the following:

- K1 and K2 bytes of the 12 STS-1s (24 bytes)
- S1 and M0 bytes of the 12 STS-1s (24 bytes)
- E1, F1, E2 bytes of the STS-1s (36 bytes)
- D1 through D12 bytes of the STS-1s (144 bytes)

The C1(J0) and B2 bytes (unshaded in the following table) are also passed through transparently from the parallel bus to the serial link.

Table 10 shows the order in which data is transferred to the serial LVDS output, starting with the most significant bit of the first A1 byte. The first bit of the first byte is replaced by an even parity check bit over all TOH bytes from the previous TOH frame. The source for the TOH bytes in the Serial TOH insert mode is summarized in the table.

violated a per channel alarm bit will be set indicating that this channel has exceeded the threshold, as well as a FIFO out-of-sync alarm bit to indicate the channel is not longer in sync with the reset of the alignment group.

The incoming data can be considered as 4 STS-12 channels (A, B, C, and D) per quad. Thus we have STS-12 channels AA to AD from quad A of the STM and STS-12 channels BA to BD of quad B. The 8 channels of parallel SONET data can be grouped into an alignment group by 2, by 4 or all 8 channels. As the serial data is run through the backplane and SERDES the parallel data can be slightly varied. The alignment FIFO can absorb this difference in the channels and create a byte aligned grouping.

These streams can be frame aligned in the following patterns. Streams can be aligned on a twin STS-12 basis as shown in Figure 18. In STS-48 mode, all four STS-12s of each STM quad are aligned with each other (i.e. AA, AB, AC, AD) as shown in Figure 19. Optionally in STS-48 mode all eight STS-12s (STMs A and B) can be aligned which allows hitless switching since all streams will be byte aligned (Figure 20). Multiple ORT8850 devices can be aligned with each other using a common system frame pulse to enable STS-192 or higher modes.

Figure 18. Twin Channel Alignment

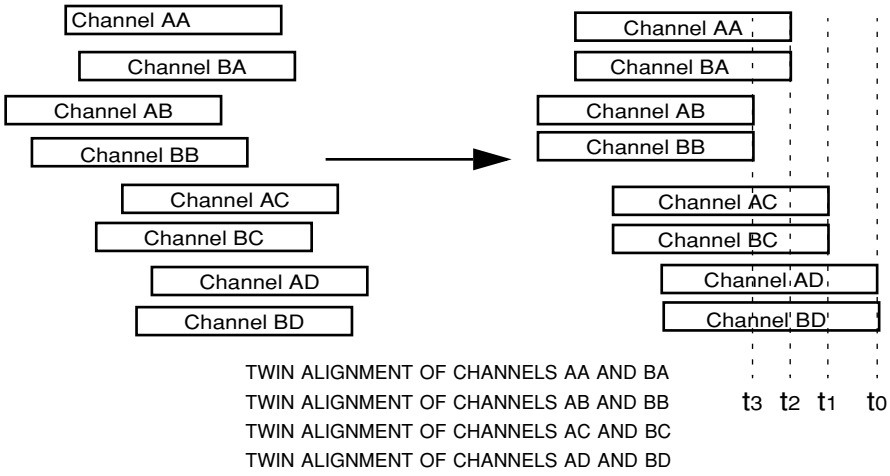
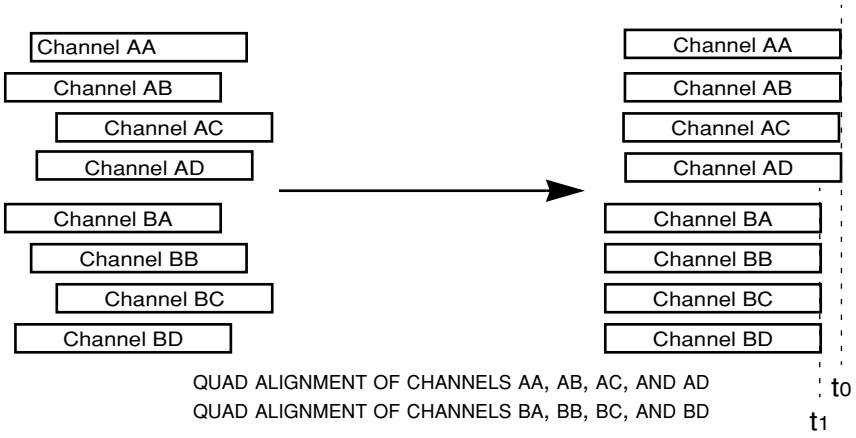


Figure 19. Alignment of SERDES Quads A and B



SPE and C1J1 Identification

In the ORT8850 each frame can be considered as 12 STS-1s. In the SPE region, there are 12 J1 pulses for each STS-1s. There is one C1(J0, new SONET specifications use J0 instead of C1 as section trace to identify each STS-1 in an STS-N) pulse in the TOH area for one frame. Thus, for non concatenated data there are a total of 12 J1 pulses and one C1(J0) pulse per frame. The C1(J0) pulse is coincident with the J0 of STS-1 #1.

The pointer interpreter identifies the payload area of each frame. The SPE flag is active when the data stream is in SPE area. SPE behavior is dependent on pointer movement and concatenation. Note that in the TOH area, H3 can also carry valid data. When valid SPE data is carried in this H3 slot, SPE is high in this particular TOH time slot. In the SPE region, if there is no valid data during any SPE column, the SPE signal will be set to low. SPE allows a pointer processor to extract payload without interpreting the pointers.

Figure 23. SPE and C1J1 Functionality for STS -12

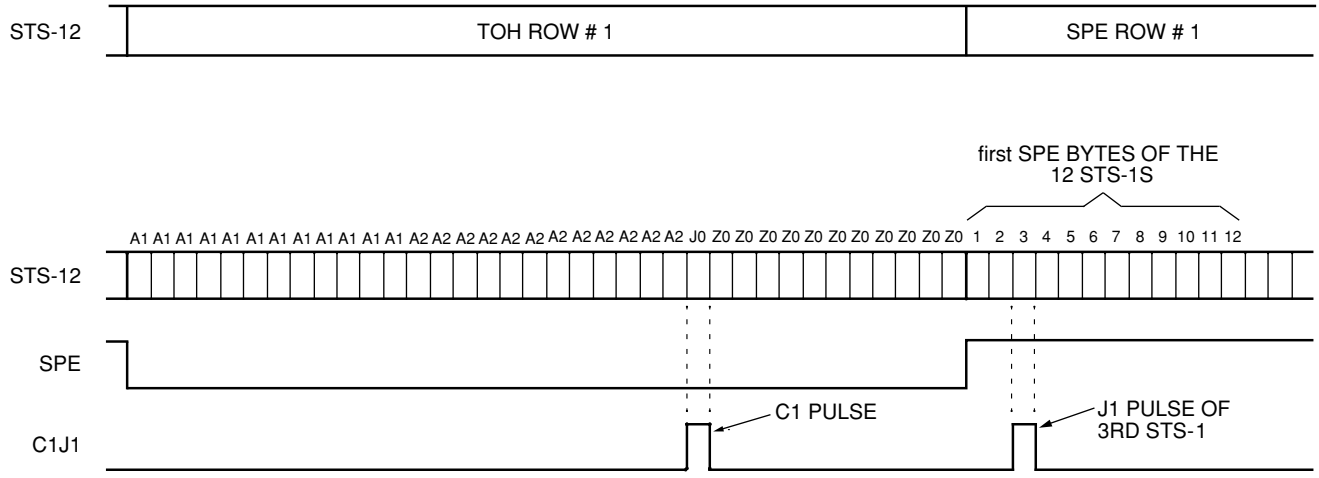
SPE	C1J1	Description
0	0	TOH information excluding C1(J0) of STS-1 #1.
0	1	Position of C1(J0) of STS-1 #1 (one per frame). Typically used to provide a unique link identification (256 possible unique links) to help ensure cards are connected into the backplane correctly or cables are connected correctly.
1	0	SPE information excluding the 12 J1 bytes.
1	1	Position of the 12 J1 bytes.

The following rules are observed for generating SPE and C1J1 signals:

- On occurrence of AIS-P on any of the STS-1, there is no corresponding J1 pulse.
- In case of concatenated payloads (up to STS48c), only the head STS-1 of the group has an associated J1 pulse.
- The C1J1 signal tracks any pointer movements.

This behavior is illustrated in the following figure. Note that the actual bit positions are dependent on the actual payload configuration and offset.

Figure 24. SPE and C1J1 Signals



Pointer Mover

After the pointer interpreter comes the pointer mover block. There is a separate pointer mover for the two SONET framer quads, A and B, each of which handles up to one STS-48 (four channels) The K1/K2 bytes and H1-SS bits are also passed through to the pointer generator so that the FPGA can receive them. The pointer mover handles both concatenations inside the STS-12, and to other STS-12s inside the core. Use of this block is optional, as discussed in a later section.

phases (i.e., received and system) are determined. This latch point is then stable unless the relative framing changes and the received H byte times collide with the system F1 or E2 times, in which case the latch point would be switched to the collision-free byte time.

There is no restriction on how many or how often increments and decrements are processed. Any received increment or decrement is immediately passed to the generator for implementation regardless of when the last pointer adjustment was made. The responsibility for meeting the SONET criteria for maximum frequency of pointer adjustments is left to an upstream pointer processor.

Receive Bypass Options

Not all of the blocks in the receive direction are required to be used. The following bypass options are valid in the receive (backplane → FPGA) direction:

- STM Pointer Mover bypass:
  - In this mode, data from the alignment FIFOs is transferred to the FPGA logic. All channels are synchronous to the FPGA_SYSCLK signals driven to the FPGA logic, as is also the case when the pointer mover is not bypassed. During bypass SPE, C1J1, and data parity signals are not valid. When the pointer mover is bypassed, eight frame pulses (DOUTxx_FP) from aligned channels are provided by the embedded core to the FPGA.
  - When the pointer mover is used, the FPGA logic provides the frame pulse on the LINE_FP (recall: there is only one LINE_FP just like there is only one SYS_FP) signal essential for the Pointer Mover to move the data. The FPGA gets eight channels of SONET data with the A1 byte position of each channel of the TOH arbitrarily offset from the LINE_FP. The DOUTxx_FP signals are not valid when the pointer mover is used.
- STM Pointer Mover and Alignment FIFO bypass:
  - In this mode, data from the framer block is transferred to the FPGA logic. All channels supply data and frame pulses synchronous with their individual recovered clock (CDR_CLK_xx) per channel. During bypass, SPE, C1J1, and data parity signals are not valid. Additionally, no serial TOH_OUT_xx data and frame pulse signals will be available. The DOUTxx_FP signals are aligned with the A1 byte position of each channel, as shown in Figure 26.

Figure 26. Pointer Mover and Alignment FIFO Bypass Timing

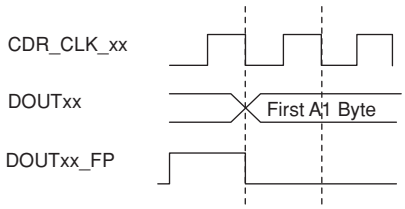


Table 14 shows the register settings to enable the bypass modes.

Table 14. Register Settings for Bypass Mode

Register Address	Value	Description
0x3000C	0x04	Turn off the SONET scrambler/descrambler
0x30020	0x07	Channel AA in functional mode
0x30038	0x07	Channel AB in functional mode
0x30050	0x07	Channel AC in functional mode
0x30068	0x07	Channel AD in functional mode
0x30080	0x07	Channel BA in functional mode
0x30098	0x07	Channel BB in functional mode
0x300B0	0x07	Channel BC in functional mode
0x300C8	0x07	Channel BD in functional mode

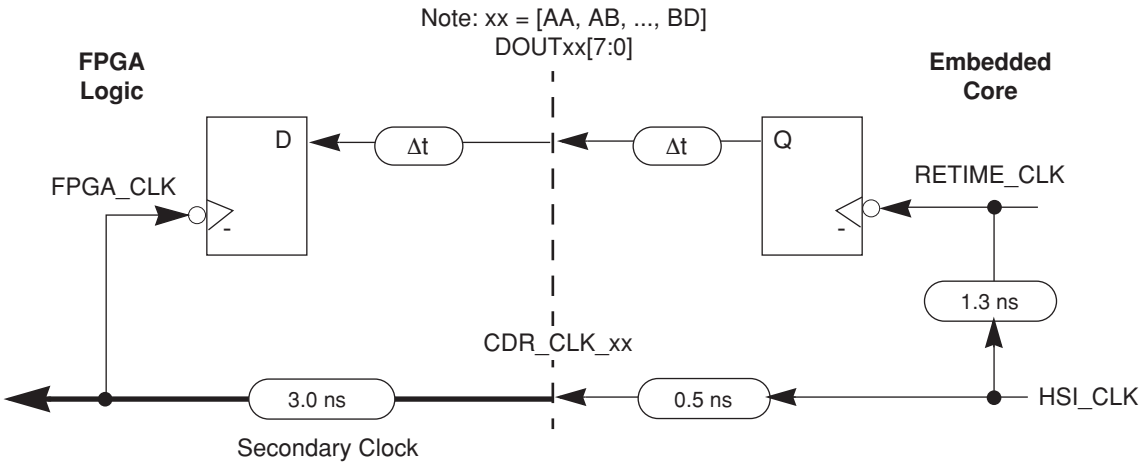
Table 15. FPGA/Embedded Core Interface Signals (Continued)

ORT8850 FPGA/Embedded Core Interface Signals - SONET Blocks		
FPGA/Embedded Core Interface Signal Name xx=[AA,…,BD]	**Input (I) to or Output (O) from Core**	**Signal Description**
SYS_FP	I	System frame pulse generated inside the FPGA logic. This is a single clock pulse of FPGA_SYSCLK every 9720 clock cycles. For a 77.76 MHz reference clock the system frame pulse is at the SONET standard of 8 KHz. All the eight Transmit channels' first A1 byte should be aligned to the SYS_FP. Internally SYS_FP is used when Far end loopback (line side loopback) needs to be performed. This loopback can only be performed when Pointer Mover is not bypassed.
LINE_FP	I	User-provided frame pulse used by only the Pointer Mover block in the receive direction. The Pointer Mover moves the data to align it with the LINE_FP. If the Pointer Mover is bypassed, LINE_FP is not used.
TOH_CLK	I	Clock driven from the FPGA to clock the TOH processor. This clock can be in the range from 25MHz to 77.76MHz. If not using the TOH communication channel this signal can be connected to GND.
Signals to TX Logic Blocks		
DINxx[7:0]	I	Byte wide data for channel xx. This data is ultimately preset on the serial LVDS pin TXDxx_W_[P:N] (work) and TXDxx_P_[P:N] (protect).
DINxx_PAR	I	Parity input for byte wide data DINxx. Odd or even parity selection is controlled by a bit in the control register at 0x3000C.
Signals from RX Logic Blocks		
DOUTxx[7:0]	O	Byte wide data for channel AA
DOUTxx_PAR	O	Parity output for byte wide data DOUTxx[7:0]. Odd/Even is controlled by control register at 0x3000C.
DOUTxx_FP	O	Frame pulse output from the SONET framer. A single clock pulse to indicate the start of the SONET frame. If bypassing the pointer mover/interpreter this pulse will line up directly with the first A1 on DOUTxx[7:0]. If using the pointer interpreter/mover DOUTxx_FP will fall several clock cycles before the A1 on DOUTxx[7:0] due to the latency from the pointer mover.
DOUTxx_SPE	O	When '1' indicates SPE bytes are on the DOUTxx[7:0] lines. Only available when using the pointer interpreter/mover
DOUTxx_C1J1	O	When '1' indicates the C1J1 bytes are on the DOUTxx[7:0] lines. Only available when using the pointer interpreter/mover.
DOUTxx_EN	O	Indicates the state of register setting for DOUTxx_EN.
CDR_CLK_xx	O	Recovered clock from the Channel xx SERDES. If not using the alignment FIFO all of the parallel data from Channel xx will be clocked from this clock.
Signals to TOH Logic Blocks (Note: These signals are active only in the serial TOH insertion mode)		
TX_TOH_CK_EN	I	Active-hi TOH_CLK enable. If using serial TOH insertion this enable must be active.
TOH_INxx	I	Serial TOH insertion port for channel xx.
Signals from TOH Logic Blocks (Note: These signals are active only in the serial TOH insertion mode)		
RX_TOH_CK_EN	O	When '1' indicates a control register bit has been set to enable the TOH clock and frame pulse.
RX_TOH_FP	O	Single clock frame pulse to indicate the serial link frame pulse.
TOH_CK_FP_EN	O	When '1' indicates the TOH serial link clock is enabled.
TOH_OUTxx	O	TOH serial link output from Channel xx

tions. (The clock edge on which data is latched in the core is hard wired to be the falling edge.) Since the falling edge of the clock (FPGA_CLK) at the FPGA latch occurs after the next data byte is launched, the delay from the interface to the FPGA latch must be large enough that an acceptable hold time margin is obtained. However the maximum propagation delay is fairly large, so a half cycle approach might lead to setup time problems.

Figure 27. Full Cycle, Alignment FIFO Bypass Mode Output Configuration and Timing (-1 Speed Grade)

a. Configuration



b. Timing (ns)

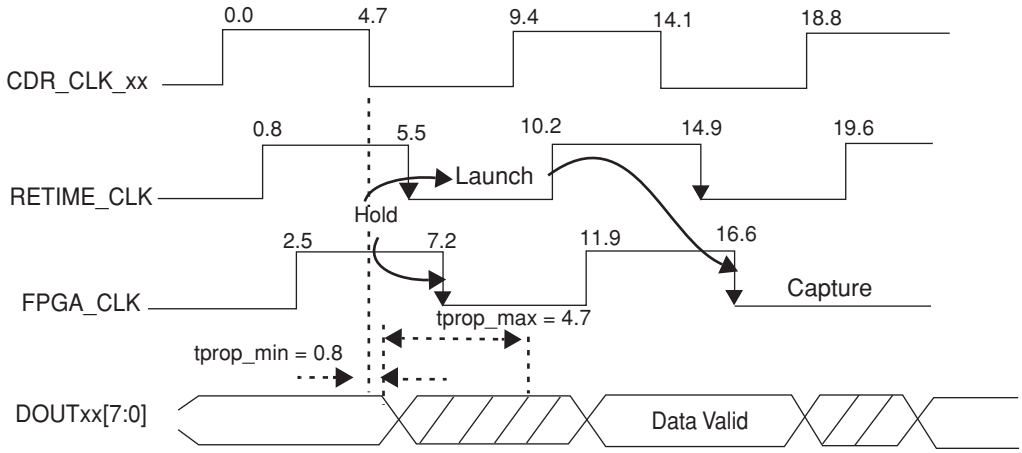
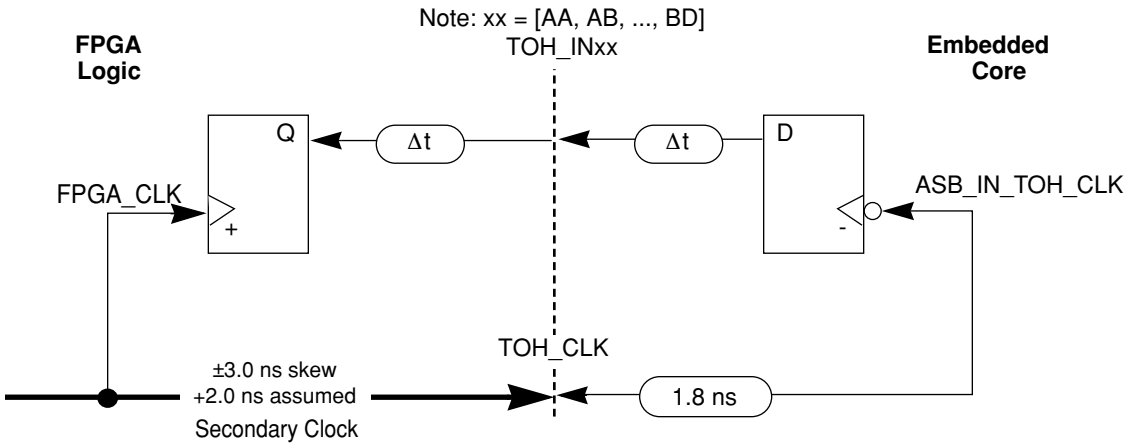


Figure 31 shows the timing for sending TOH data from the FPGA logic to the Core. As in the earlier input example, the constraints on the data are specified in terms of setup and hold times on the data at the interface relative to the clock at the interface. In the case shown, launch and capture occur on different clock edges (rising edge in the FPGA). Data is captured before the next data is launched, so there will be no hold margin problem. Launched data also has nearly a full clock period to become stable at the capture latch, so setup margin should not be a problem for the timing relationships assumed in the example. Actual timing analysis should be performed for each application because of the wide range of possible skew values.

Figure 31. Half Cycle, TOH Input Configuration and Timing (-1 Speed Grade)

a. Configuration



b. Timing (ns)

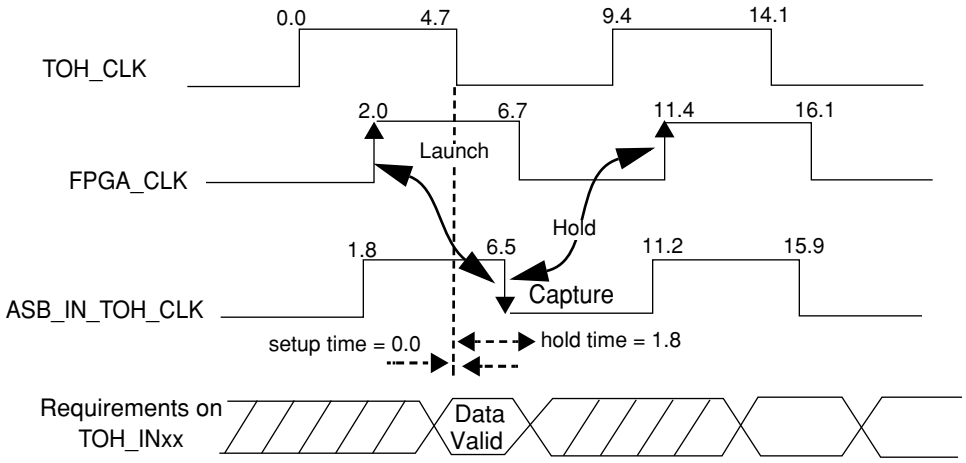


Table 18. LVDS Protection Switching (Continued)

FPGA Interface Signal	When '0'	When '1'
LVDS_PROT_BA	Channel BA gets TXD_BA_W_[P:N]	Channel BA gets TXD_BA_P_[P:N]
LVDS_PROT_BB	Channel BB gets TXD_BB_W_[P:N]	Channel BB gets TXD_BB_P_[P:N]
LVDS_PROT_BC	Channel BC gets TXD_BC_W_[P:N]	Channel BC gets TXD_BC_P_[P:N]
LVDS_PROT_BD	Channel BD gets TXD_BD_W_[P:N]	Channel BD gets TXD_BD_P_[P:N]

For software control of the LVDS protection switching there is an enable bit to enable software control, and a bit per channel which selects main or protect. The enable register is at 0x30008 in the memory map (Table 19).

Memory Map

The memory map for the ORT8850 core is only part of the full memory map of the ORT8850 device. The ORT8850 is an ORCA Series4 based device and thus uses the system bus as a communication bridge. The ORT8850 core register map contained in this data sheet only covers the embedded ASIC core of the device, not the entire device. The system bus itself, and the generic FPGA memory map, are fully documented in the MPI/System Bus Application Note. As part of the system bus, the embedded ASIC core of an FPSC is located at address offset 0x30000. The ORT8850 embedded core is an eight-bit slave interface on the Series 4 system bus.

Each ORCA device contains a device ID. This device ID is unique to each ORCA device and can be used for device identification and assist in system debugging. The device ID is located at absolute address 0x00000 - 0x00003. The ORT8850H's device ID is 0xDC0123C0 and the ORT8850L's device ID is 0xDC0121C0. More information on the device ID and other Series 4 generic registers can be found in the MPI/System Bus Application Note.

The ORT8850 core registers are clocked by the reference clock SYS_CLK_P/N. If a clock is not provided to the reference clock, the registers will fail to operate.

The ORT8850 core registers do not check for parity on a write operation. On a read operation, no parity is generated, and a "0" is passed back to the initiating bus master interface on the parity signal line.

Registers Access and General Description

The memory map comprises three address blocks:

- Generic register block: ID, revision, scratch pad, lock and reset register.
- Device register block: control and status bits, common to the eight channels in each of the two quad interfaces.
- Channel register blocks: each of the four channels in both quads have an address block. The four address blocks in both quads have the same structure, with a constant address offset between channel register blocks.

All registers are write-protected by the lock register, except for the scratch pad register. The lock register is a 16-bit read/write register. Write access is given to registers only when the key value 0x0580 is present in the lock register. An error flag will be set upon detecting a write access when write permission is denied. The default value is 0x0000.

After power-up reset or soft reset, unused register bits will be read as zeros. Unused address locations are also read as zeros. Bit in write-only registers will always be read as zeros.

This table is constructed to show the correct values when read and written via the system bus MPI interface. **When using this table while interfacing with the system bus user logic master interface, the data values will need to be byte flipped.** This is due to the opposite orientation of the MPI and master interface bus ordering. More information on this can be found in the MPI/System Bus Application Note (TN1017).

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
3000C	[0:3]	R/W	number of consecutive A1 A2 errors to generate [0:3]	00	If a particular channel's "A1 A2 error insert command" control bit is set to the value 1 then the "A1 and A2 error insert values" will be inserted into that channels respective A1 and A2 bytes. The number of consecutive frames to be corrupted is determined by the "number of consecutive A1 A2 errors to generate [0:3]" control bits. MSB is bit 3
	[4]	R/W	backplane side loopback control	0	0 = No loopback. 1 = RX to TX loopback on backplane side. Serial input is run through SERDES and SONET block, then looped back in parallel to SERDES and out serial.
	[5]	R/W	DINxx/DOUTxx parallel bus parity control	1	0 = Odd parity 1 = Even parity
	[6]	R/W	scrambler/descrambler	1	0 = no RX direction, descramble / TX direction scramble 1 = In RX direction, descramble channel after the SONET frame recovery. In TX direction, scramble data just before parallel-to-serial conversion
	[7]	-	Not Used	0	
3000D	[0:7]	R/W	A1 error insert value [0:7]	00	Value of the A1 byte for error insert
3000E	[0:7]	R/W	A2 error insert value [0:7]	00	Value of the A2 byte for error insert
3000F	[0:7]	R/W	transmit B1 error insert mask [0:7]	00	0 = No error insertion. 1 = Invert corresponding bit in B1 byte.
30010	[0]	R	AA alarm	0	Consolidation alarm for channel AA 1 = alarm 0 = no alarm.
	[1]	R	AB alarm	0	Consolidation alarm for channel AB 1 = alarm 0 = no alarm.
	[2]	R	AC alarm	0	Consolidation alarm for channel AC 1 = alarm 0 = no alarm.
	[3]	R	AD alarm	0	Consolidation alarm for channel AD 1 = alarm 0 = no alarm.
	[4-7]	-	Not Used	0	
30011	[0]	R/W	AA/BA alarm enable/mask register	0	AA and BA enable 1 = enabled 0 = not enabled
	[1]	R/W	AB/BB alarm enable/mask register	0	AB and BB enable 1 = enabled 0 = not enabled
	[2]	R/W	AC/BC alarm enable/mask register	0	AC and BC enable 1 = enabled 0 = not enabled
	[3]	R/W	AD/BD alarm enable/mask register	0	AD and BD enable 1 = enabled 0 = not enabled
	[4-7]	-	Not Used	0	

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
30017	[0]	R/W	BD resync	0	Channel BD alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO. Write “0” for normal operation
	[1]	R/W	BC resync	0	Channel BC alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO. Write “0” for normal operation
	[2]	R/W	BB resync	0	Channel BB alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO. Write “0” for normal operation
	[3]	R/W	BA resync	0	Channel BA alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO. Write “0” for normal operation
	[4]	R/W	AD resync	0	Channel AD alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO.Write “0” for normal operation
	[5]	R/W	AC resync	0	Channel AC alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO.Write “0” for normal operation
	[6]	R/W	AB resync	0	Channel AB alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO.Write “0” for normal operation
	[7]	R/W	AA resync	0	Channel AA alignment FIFO resync. Write “1” to resync this channel. When no alignment is used, this resets the read pointer to the middle of the FIFO.Write “0” for normal operation
30018	[0]	R/W	AD/BD resync	0	2-link AD/BD alignment FIFO resync. Write “1” to resync this link. Write “0” for normal operation.
	[1]	R/W	AC/BC resync	0	2-link AC/BC alignment FIFO resync. Write “1” to resync this link. Write “0” for normal operation.
	[2]	R/W	AB/BB resync	0	2-link AB/BB alignment FIFO resync. Write “1” to resync this link. Write “0” for normal operation.
	[3]	R/W	AA/BA resync	0	2-link AA/BA alignment FIFO resync. Write “1” to resync this link. Write “0” for normal operation.
	[4]	R/W	STM B resync	0	Quad B alignment resync. Write “0” for normal operation.
	[5]	R/W	STM A resync	0	Quad A alignment FIFO resync Write “0” for normal operation.
	[6]	R/W	All 8 resync	0	All 8 channel alignment FIFO resync. Write “0” for normal operation.
	[7]	-	Not Used	N/A	

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
30027* 0303F 30057 3006F 30087 3009F 300B7 300CF	[0]	R/W	enable channel alarm	0	Channel alarm bit (30026, ...) enable. Set to 1 to enable alarm bit to propagate to alarm 0x30010
	[1]	R/W	enable AIS-P flag	0	AIS -P flag alarm enable. Set to 1 to enable alarm bit to propagate to alarm 0x30010
	[2]		enable pointer mover elastic store overflow flag	0	Pointer mover elastic store overflow flag enable. Set to 1 to enable alarm bit to propagate to 0x30010
	[3-7]	-	Not Used	0	
30028* 30040 30058 30070 30088 300A0 300B8 300D0	[0]	R	FIFO aligner threshold error flag	00	Alarm is set to 1 if either the min or max FIFO threshold levels are violated, the min and max threshold levels can be set in address 0x3000A and 0x300B. Alarm enable is 0x30029 bit 0. Write 1 to clear this alarm bit This alarm is only valid when FIFO OOS flag is also set.
	[1]		RX internal path parity error flag		Alarm indicator on receive path internal parity error. Alarm is enabled in 0x30029 bit 1. Write 1 to clear
	[2]		OOF flag		Alarm indicator channel is OOF. Alarm enable is 0x30029 bit 2. Write 1 to clear.
	[3]		LVDS link B1 parity error flag		Alarm indicator that channel has found a B1 parity error. Alarm enable is 0x30029 bit 3. Write 1 to clear.
	[4]		DINxx parallel bus parity error flag	0	Alarm indicator channel has found a parity error on the DINxx input from the FPGA.Alarm enable is 0x30029 bit 4. Write 1 to clear.
	[5]		TOH serial input port parity error flag	0	Alarm indicator channel has found a parity error on the TOH_INxx input from the FPGA. Write 1 to clear this alarm. Alarm enable is 0x30028 bit 5.
	[6]		FIFO OOS error flag	0	Alarm indicates channel group is out of sync. Write 1 to clear. Alarm enable is 0x30028.
	[7]	-	Not Used	0	
30029* 30041 30059 30071 30089 300A1 300B9 300D1	[0:6]	R/W	channel alarm enable	00	Enable bits for channel alarm register 0x30028. Set to 1 to enable and to propagate the alarm to register 0x30026 bit 0.
	[7]	-	Not Used	0	
3002A* 30042 3005A 30072 3008A 300A2 300BA 300D2	[0:3]	R	AIS alarm flags 3, 6, 9, 12	0	These are the AIS-P alarm flags. 1 if the LVDS input STS # contains AIS.
	[4-7]	-	Not Used	0	

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
3002B* 30043 3005B 30073 3008B 300A3 300BB 300D3	[0:7]	R	AIS alarm flags 1, 4, 7, 10, 2, 5, 8, 11	00	These are the AIS-P alarm flags. 1 if the LVDS input STS # contains AIS.
3002C* 30044 3005C 30074 3008C 300A4 300BC 300D4	[0:3]	R/W	enable AIS alarm 3, 6, 9, 12	0	Enable bits for AIS alarms. Set to 1 to enable and propagate the alarm to register 0x30026.
	[4-7]	-	Not Used	0	
3002D* 30045 3005D 30075 3008D 300A5 300BD 300D5	[0:7]	R/W	AIS alarm enable 1, 4, 7, 10, 2, 5, 8, 11	00	Enable bits for AIS alarms. Set to 1 to enable and propagate the alarm to register 0x30026.
3002E* 30046 3005E 30076 3008E 300A6 300BE 300D6	[0:3]	R	Pointer mover elastic store overflow flags 12, 9, 6, 3	0	Per STS-1 pointer mover elastic store overflow alarm flags. This alarm will propagate to 0x30026 bit 2 when enabled
	[4-7]	-	Not Used	0	
3002F* 30047 3005F 30077 3008F 300A7 300BF 300D7	[0:7]	R	Pointer mover elastic store overflow flags 4, 7, 10, 2, 5, 8, 11	00	Per STS-1 pointer mover elastic store overflow alarm flags. This alarm will propagate to 0x30026 bit 2 when enabled
30030* 30048 30060 30078 30090 300A8 300C0 300D8	[0:3]	R/W	enable elastic store overflow flag 12, 9, 6, 3	0	Enable Bit for elastic store alarms. Set 1 to enable alarm and propagate alarm to register 0x30026
	[4-7]	-	Not Used	0	

Electrical Characteristics

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The *ORCA* Series 4 FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Table 20. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_{stg}	-65	150	°C
Power Supply Voltage with Respect to Ground	V_{DD33}[2]	-0.3	4.2	V
	V_{DDIO}	-0.3	4.2	V
	V_{DD15}	-0.3	2.0	V
	V_{DDA_STM}[1]	-0.3	2.0	V
Input Signal with Respect to Ground	—	-0.3	V_{DDIO} + 0.3	V
Signal Applied to High-impedance Output	—	-0.3	V_{DDIO} + 0.3	V
Maximum Package Body (Soldering) Temperature	—	—	220	°C

Recommended Operating Conditions

Table 21. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage with Respect to Ground*	V_{DD33}[2]	2.7	3.6	V
	V_{DD15}	1.425	1.575	V
	V_{DDA_STM}[1]	1.425	1.575	V
Input Voltages	V_{IN}	-0.3	V_{DDIO} + 0.3	V
Junction Temperature	T_J	-40	125	°C

For FPGA Recommended Operating Conditions and Electrical Characteristics, see the Recommended Operating Conditions and Electrical Characteristics tables in the ORCA Series 4 FPGA data sheet (ORT8850L: OR4E02, ORT8850H: OR4E06) and the ORCA Series 4 I/O Buffer Technical Note. FPSC Standby Currents (I_{DD}SB15 and I_{DD}SB33) are tested with the Embedded Core in the powered down state.

Notes:
1. V_{DDA_STM} is an analog power supply input which needs to be isolated from other power supplies on the board.
2. V_{DD33} is an analog power supply for the FPGA PLLs and needs to be isolated from other power supplies on the board.

Table 32. FPGA Common-Function Pin Descriptions (Continued)

Symbol	I/O	Description
Special-Purpose Pins		
M[3:0]	I	During power-up and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.*
PLL_CK[0:7][TC]	I	Semi-dedicated PLL clock pins. During configuration they are 3-stated with a pull up.
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user-programmable I/O, if not used for clock inputs.
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O in boundary scan is not used.*
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration this pin is a user-programmable I/O pin.*
HDC	O	High during configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{LDC}}$	O	$\overline{\text{Low during configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.*
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
$\overline{\text{WR}}$/MPI_RW	I	$\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{\text{WR}}$/MPI_RW is a user-programmable I/O pin.*
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the *PowerPC* bus master utilizing the least-significant bits of the *PowerPC* 32-bit address.
$\overline{\text{MPI\_BURST}}$	I	$\overline{\text{MPI\_BURST}}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.

1. The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Table 35. ORT8850H Pins That Are Unused in ORT8850L

BGA Ball Bonds	ORT8850H PIOs
K4	PL11A
M5	PL13A
R5	PL20A
T5	PL21A
W4	PL27A
AA2	PL28A
Y4	PL29A
AC4	PL35A
AD5	PL37A
AG1	PL38A
AP4	PB3A
AK10	PB9A
AK11	PB10A
AM9	PB11A
AN9	PB12A
AM14	PB19A
AN14	PB20A
D11	PT12A
E13	PT11A

Users should avoid using these pins if they plan to migrate their ORT8850H design to an ORT8850L.

Package Pinouts

Table 36 provides the package pin and pin function for the ORT8850 FPSC and packages. The bond pad name is identified in the PIO nomenclature used in the *ispLEVER* design editor. The Bank column provides information as to which output voltage level bank the given pin is in. The Group column provides information as to the group of pins the given pin is in. This is used to show which VREF pin is used to provide the reference voltage for single-ended limited-swing I/Os. If none of these buffer types (such as SSTL, GTL, HSTL) are used in a given group, then the VREF pin is available as an I/O pin.

When the number of FPGA bond pads exceeds the number of package pins, bond pads are unused. When the number of package pins exceeds the number of bond pads, package pins are left unconnected (no connects). When a package pin is to be left as a no connect for a specific die, it is indicated as a note in the device column for the FPGA. The tables provide no information on unused pads.

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
P17	—	—	VDD15	VDD15	VDD15	—	—
P18	—	—	VDD15	VDD15	VDD15	—	—
N16	—	—	VDD15	VDD15	VDD15	—	—
N17	—	—	VDD15	VDD15	VDD15	—	—
N18	—	—	VDD15	VDD15	VDD15	—	—
N19	—	—	VDD15	VDD15	VDD15	—	—
P16	—	—	VDD15	VDD15	VDD15	—	—
P19	—	—	VDD15	VDD15	VDD15	—	—
R16	—	—	VDD15	VDD15	VDD15	—	—
R17	—	—	VDD15	VDD15	VDD15	—	—
R18	—	—	VDD15	VDD15	VDD15	—	—
R19	—	—	VDD15	VDD15	VDD15	—	—
T13	—	—	VDD15	VDD15	VDD15	—	—
T14	—	—	VDD15	VDD15	VDD15	—	—
T15	—	—	VDD15	VDD15	VDD15	—	—
T20	—	—	VDD15	VDD15	VDD15	—	—
T21	—	—	VDD15	VDD15	VDD15	—	—
U13	—	—	VDD15	VDD15	VDD15	—	—
U14	—	—	VDD15	VDD15	VDD15	—	—
U15	—	—	VDD15	VDD15	VDD15	—	—
U20	—	—	VDD15	VDD15	VDD15	—	—
U21	—	—	VDD15	VDD15	VDD15	—	—
V13	—	—	VDD15	VDD15	VDD15	—	—
V14	—	—	VDD15	VDD15	VDD15	—	—
V15	—	—	VDD15	VDD15	VDD15	—	—
V20	—	—	VDD15	VDD15	VDD15	—	—
V21	—	—	VDD15	VDD15	VDD15	—	—
W13	—	—	VDD15	VDD15	VDD15	—	—
W14	—	—	VDD15	VDD15	VDD15	—	—
W15	—	—	VDD15	VDD15	VDD15	—	—
W20	—	—	VDD15	VDD15	VDD15	—	—
W21	—	—	VDD15	VDD15	VDD15	—	—
Y17	—	—	VDD15	VDD15	VDD15	—	—
Y18	—	—	VDD15	VDD15	VDD15	—	—
Y19	—	—	VDD15	VDD15	VDD15	—	—
AA16	—	—	VDD15	VDD15	VDD15	—	—
AA17	—	—	VDD15	VDD15	VDD15	—	—
AA18	—	—	VDD15	VDD15	VDD15	—	—
AA19	—	—	VDD15	VDD15	VDD15	—	—
AB16	—	—	VDD15	VDD15	VDD15	—	—
AB17	—	—	VDD15	VDD15	VDD15	—	—
AB18	—	—	VDD15	VDD15	VDD15	—	—

FPSC Maximum Junction Temperature

Once the power dissipated by the FPSC has been determined, the maximum junction temperature of the FPSC can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Using the maximum ambient temperature, T_{Amax}, and the power dissipated by the device, Q (expressed in °C), the maximum junction temperature is approximated by:

$T_{Jmax} = T_{Amax} + (Q \bullet \theta_{JA})$

Table 37 lists the thermal characteristics for the package used with the *ORCA* ORT8850 Series of FPSCs.

Package Thermal Characteristics

Table 37. ORCA ORT8850 Plastic Package Thermal Guidelines

Package	ΘJA (°C/W)			Maximum Power (W)
	0 fpm	200 fpm	500 fpm	T = 70 °C Max, TJ = 125 °C Max, 0 fpm
680-Pin PBGAM*	13.4	11.5	10.5	4.10

* The 680-Pin PBGAM package includes 2 oz. copper plates.

Heat Sink Information

The estimated worst-case power requirements for the ORT8850 are in the 4 W to 5 W range. Consequently, for most applications an external heat sink will be required. The following table lists, in alphabetical order, heat sink vendors who advertise heat sinks aimed at the BGA market.

Table 38. Heat Sink Vendors

Vendor	Location	Phone
Aavid Thermalloy	Concord, NH	(603) 224-9988
Chip Coolers (Tyco Electronics)	Harrisburg, PA	(800) 468-2023
IERC (CTS Corp.)	Burbank, CA	(818) 842-7277
R-Theta	Buffalo, NY	(800) 388-5428
Sanyo Denki	Torrance, CA	(310) 783-5400
Wakefield Thermal Solutions	Pelham, NH	(603) 635-2800

Package Coplanarity

The coplanarity limits of the Lattice packages are as follows:

- PBGAM: 8.0 mils

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 39 lists eight parasitics associated with the *ORCA* packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

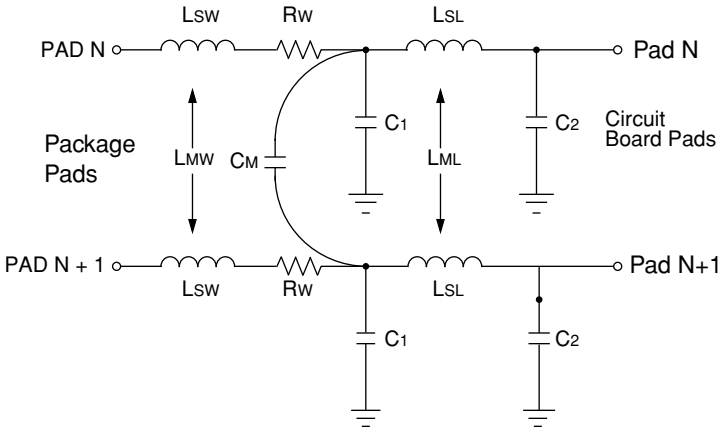
Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 39 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.

Table 39. ORCA ORT8850 Package Parasitics

Package Type	L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
680-Pin PBGAM	3.8	1.3	250	1.0	1.0	0.3	2.8 - 5.0	0.5 - 1.0

Figure 39. Package Parasitics



Package Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP): When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.