Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

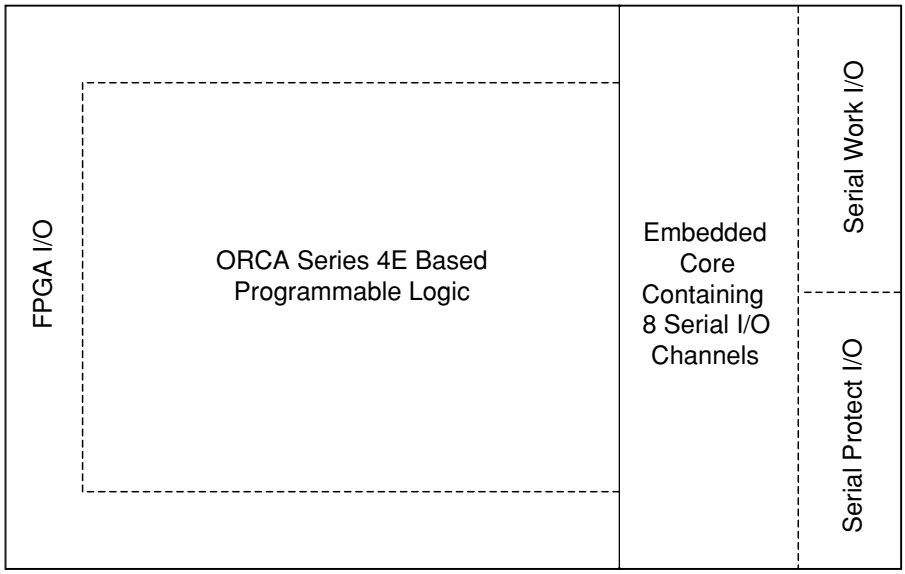
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	4992
Total RAM Bits	75776
Number of I/O	278
Number of Gates	397000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort8850l-1bm680i

ORT8850 Overview

The ORT8850 FPSCs provide high-speed backplane transceivers combined with FPGA logic. There are two devices in the ORT8850 family. The ORT8850L device is based on 1.5 V OR4E02 ORCA FPGA and has a 26 x 24 array of Programmable Logic Cells (PLCs). The ORT8850H device is based on 1.5V OR4E06 ORCA FPGA and has a 46 x 44 array. The embedded core which contains the backplane transceivers is attached to the right side of the device and is integrated directly into the FPGA array. A top level diagram of the basic chip configuration is shown in Figure 1.

Figure 1. ORT8850 Top Level Diagram



Embedded Core Overview

The ORT8850 embedded core contains a pseudo-SONET block for backplane or intra-board, chip-to-chip communication. The SONET block includes a High-Speed Interface (HSI) macrocell and a Synchronous Transport Module (STM) macrocell. It supports eight full-duplex channels and performs data transfer, scrambling/descrambling and SONET framing at the maximum rate of 850 Mbits/s. Figure 2 shows a top level diagram of the ORT8850 and the basic data flows through the device.

LVDS Reference Clock

The reference clock for the ORT8850 SERDES is an LVDS input (SYS_CLK_[P:N]). This reference clock can run in the range from 63.00 MHz to 106.25 MHz and is used to clock the entire Embedded Core. This clock is also available in the FPGA interface as the output signal FPGA_SYSCLK at the Embedded Core/FPGA Logic interface.

The supported range of reference clock frequencies will drive the internal and link serial rates from 504 MHz to 850 MHz. For standard SONET applications a reference clock rate of 77.76 MHz will allow the ORT8850 to communicate with standard SONET devices. If the ORT8850 is communicating with another ORT8850, the reference clock can run anywhere in the defined range. When using a non 77.76 MHz reference clock, the frame pulse will now need to be derived from the non standard rate thus making the frame pulse rate not 8 kHz, but rather a single clock pulse every 9720 clock cycles.

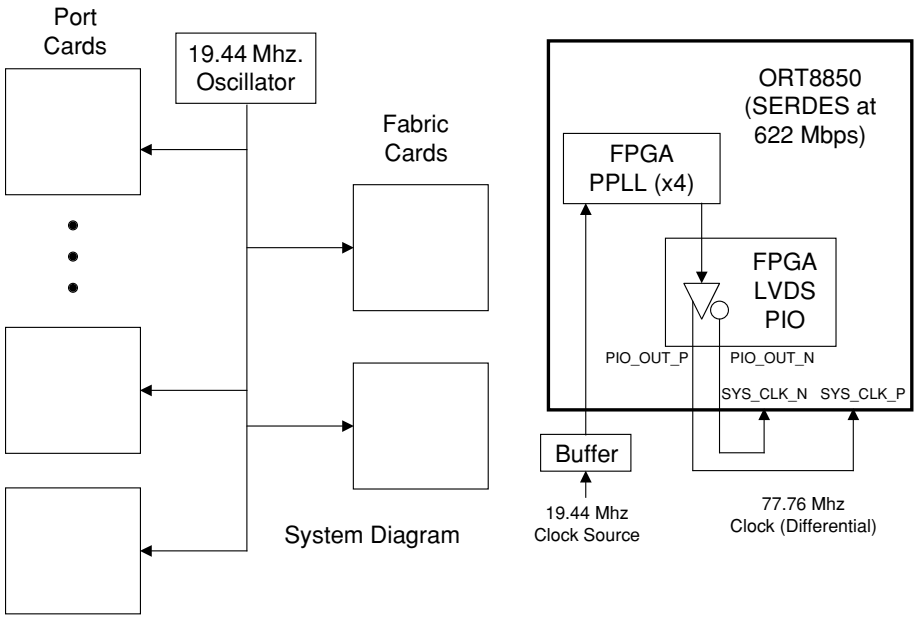
System Considerations for Reference Clock Distribution

There are two main system clocking architectures that can be used with the ORT8850 at the system level to provide the LVDS reference clocks. The recommended approach is to distribute a single reference clock to all boards. However, independent clocks can be used on each board provided that they are matched with sufficient accuracy and the alignment is not used. These two approaches are summarized in the following paragraphs

Distributed Clocking

A distributed clock architecture, shown in Figure 5, uses a single source for the system reference clock. This single source drives all devices on both the line and switch sides of the backplane. Typically this is a lower speed clock such as a 19.44 MHz signal. An external PLL on each board or and internal ORT8850 FPGA PLL is then used to multiply the clock to the desired reference clock rate (i.e. by 4x to 77.76 MHz if the distributed clock is at 19.44 MHz). Using this type of clock architecture the ORT8850 data channels are fully synchronous and no domain transfer is required from the transmitter to the receiver.

Figure 5. Distributed Clock Architecture



Independent Clocking

An independent clock architecture uses independent clock sources on each ORT8850 board. With this architecture, for the SERDES to sample correctly the independent oscillators must be within reference clock tolerance requirements for the Clock and Data Recovery (CDR) to correctly sample the incoming data and recover data and clock. The local reference clock and the recovered clock will not be synchronous since they are created from a different source. The alignment FIFO uses the recovered clock for write and the local reference clock for read. Due to

Pointer Mover Performance Monitoring: There is Pointer Mover performance monitoring in the Receiver section. Alarm Indication Signals (AIS-P) and elastic store overflows are reported. AIS-P is implemented as a per STS-1 alarm bit. Elastic store overflow will cause an alarm bit to be set on a per STS-1 basis.

FIFO Aligner Monitoring: There is monitoring of the FIFO aligner operating point, and upon deviating from the nominal operating point of the FIFO by more than user programmable threshold values (min and max threshold values), an alarm bit is set. Threshold values are defined per device; alarm flags are per channel.

Frame Offset Monitoring: There is monitoring of the frame offset between all enabled channels (disabled channels do not interfere with the monitoring). Monitoring is performed continuously. Upon exceeding the maximum allowed frame offset (18 bytes) between all enabled channels, an alarm bit is set.

Error Insertion

A1/A2 Error Insert: There is a Frame Error inject feature in the transmitter section, allowing the user to replace framing bytes A1/A2 (only last A1 byte and first A2 byte) with a selectable A1/A2 byte value for a selectable number of consecutive frames. The number of consecutive frames to alter is specified by a 4-bit field, while A1/A2 value is specified by two 8-bit fields. The error insert feature is on a per channel basis, A1/ A2 values and 4-bit frame count value are on a per device basis.

B1 Error Insert: There is a B1 error insert feature in the transmitter section, allowing the user to insert errors on user selectable bits in the B1 byte. Errors are created by simply inverting bit values. Bits to invert are specified through an 8-bit control. To insert an error, software will first set the bits in the "transmitter B1 error insert mask". Then, on a per channel basis software will write a one to the "B1 error insert command". The insertion circuitry performs a rising edge detect on the bit, and will issue a corruption signal for the next frame, for one frame only. This feature is on a per channel basis.

TOH Serial Output Port Parity Error Insert: There is a Parity error inject feature, in the receive section, allowing the user to invert the parity bit of each serial output port. This feature inserts a single error. This feature is on a per channel basis.

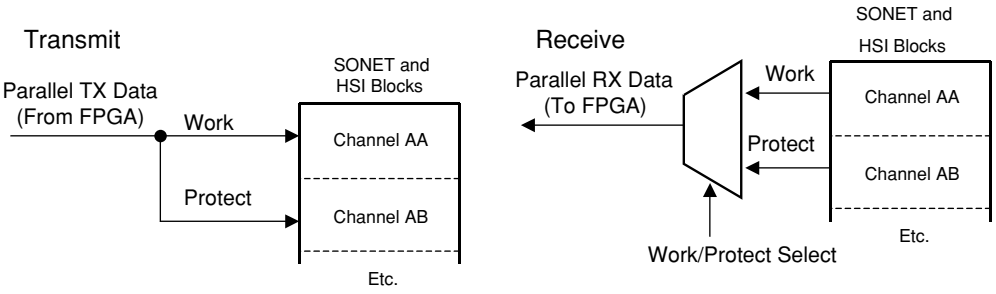
Parallel Output Bus Parity Error Insert: There is a Parity error inject feature, in the receive section, allowing the user to invert parity lines (DOUTxx_PAR) associated with each output parallel busses (DOUTxx[7:0]). This feature inserts a single error. This feature is on a per channel basis. This feature supports both 'even' and 'odd' parities.

Loopback

There are two types of loopback that can be utilized inside the embedded ASIC core of the ORT8850, near end loopback and far end (line side) loopback. Both of these loopbacks are controlled by control registers inside the ORT8850 core, which are accessible from the system bus and the MicroProcessor Interface (MPI). In both loopback modes, all channels are placed with a single control. The data paths in the two loopback modes are shown in Figure 8.

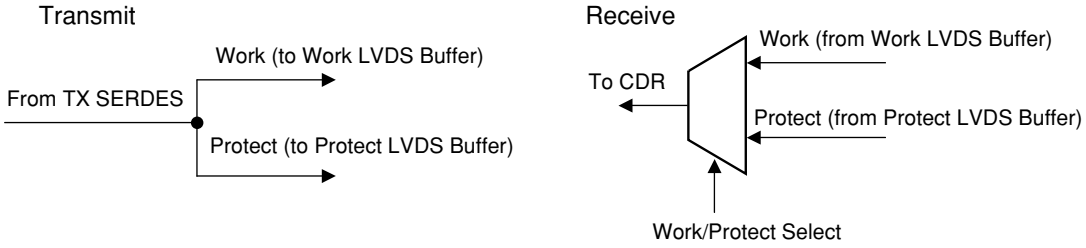
AA. This same scheme is used for channels groupings of AC/AD, BA/BB, and BC/BD. For quad protection when the alignment FIFOs are to be used, the protection switching must be done in FPGA logic.

Figure 9. Parallel Protection Switching



LVDS protection switching (Figure 10) takes place at the LVDS buffer before the serial data is sent into the CDR. The selection is between the main LVDS buffer and the protect LVDS buffer. The main LVDS buffer provide the main receive data on RXDxx_W_[P:N] while the protect LVDS buffers provide protection receive data on RXDxx_P_[P:N]. When operating using the main LVDS buffers (default) no status information is available on the protect LVDS buffers since the serial stream must reach the SONET framer before status information is available on the data stream. The same is also true for the main LVDS buffers when operating with the protect buffers.

Figure 10. LVDS Protection Switching



See Table 17 and Table 18 and the accompanying text for details and register settings for the protection switching options.

FPSC Configuration - Overview

Configuration of the ORT8850 occurs in two stages: FPGA bit stream configuration and embedded core setup.

FPGA Configuration - Overview

Prior to becoming operational, the FPGA goes through a sequence of states, including power-up, initialization, configuration, start-up, and operation. The FPGA logic is configured by the standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet. The options for the embedded core are set via registers that are accessed through the FPGA system bus. The system bus can be driven by an external PPC compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block, that drives the system by using the user interface and uses very little FPGA logic, is available in the *MPI/System Bus* technical note (TN1017). This IP block sets up the embedded core via a state machine and allows the ORT8850 to work in an independent system without an external MicroProcessor Interface.

Embedded Core Setup

All options for the operation of the core are configured according to the memory map shown in Table 19.

During the power-up sequence, the ORT8850 device (FPGA programmable circuit and the core) is held in reset. All the LVDS output buffers and other output buffers are held in 3-state. All Flip-Flops in the core area are in reset state, with the exception of the boundry-scan shift registers, which can only be reset by boundary-scan reset. After power-up reset, the FPGA can start configuration. During FPGA configuration, the ORT8850 core will be held in

reset and all the local bus interface signals forced high, but the following active-high signals, PROT_SWITCH_AA, PROT_SWITCH_AC, PROT_SWITCH_BA, PROT_SWITCH_BC, TX_TOH_CK_EN, SYS_FP, LINE_FP, will be forced low. The CORE_READY signal sent from the embedded core to FPGA is held low, indicating that the core is not ready to interact with FPGA logic. At the end of the FPGA configuration sequence, the CORE_READY signal will be held low for six SYS_CLK cycles after DONE, TRI_IO and RST_N (core global reset) are high. Then it will go active-high, indicating the embedded core is ready to function and interact with FPGA programmable circuit. During FPGA reconfiguration when DONE and TRI_IO are low, the CORE_READY signal sent from the core to FPGA will be held low again to indicate the embedded core is not ready to interact with FPGA logic. During FPGA partial configuration, CORE_READY stays active. The same FPGA configuration sequence described previously will repeat again.

The initialization of the embedded core consists of two steps: register configuration and synchronization of the alignment FIFO. The steps to configure the ORT8850 device for normal operation are listed in Table 4 and Table 5.

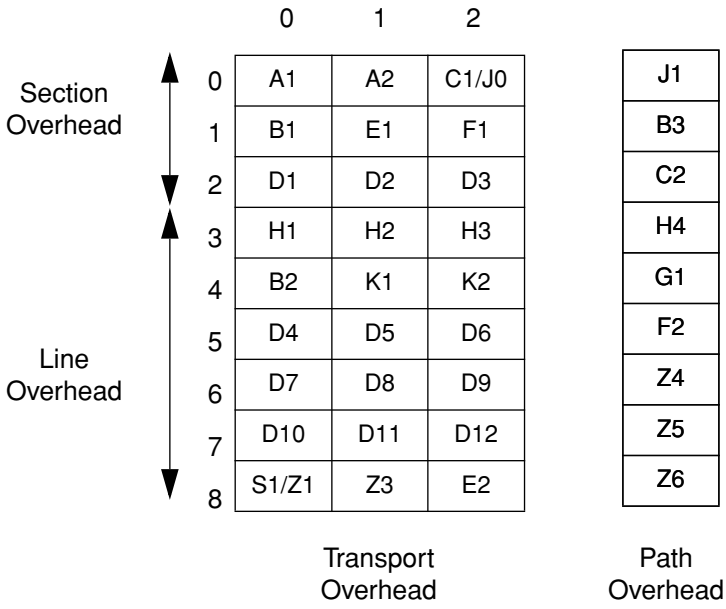
Generic Backplane Transceiver Application

Independent Channels, Transparent TOH: Table 4 lists the register values to setup the ORT8850 as eight independent SONET channels (no alignment) using transparent TOH. The order is specific. The values are given from the PowerPC point of view. If using the MPI to write data to the ORT8850, the value given in the table is the value that should be used. If using the UMI of the system bus, the data value would need to be byte flipped.

Table 4. Independent Channels, Transparent TOH

Register Address	Value	Description
0x30004	0x05	Lock register. This value must be written to allow writing to any other ORT8850 core register
0x30005	0x80	Lock register. This value must be written to allow writing to any other ORT8850 core register
0x30020	0x07	Turn on Channel AA in functional mode
0x30021	0xFF	Channel AA - Transparent TOH from parallel data
0x30022	0xFF	Channel AA - Transparent TOH from parallel data
0x30038	0x07	Turn on Channel AB in functional mode
0x30030	0xFF	Channel AB - Transparent TOH from parallel data
0x3003A	0xFF	Channel AB - Transparent TOH from parallel data
0x30050	0x07	Turn on Channel AC function mode
0x30051	0xFF	Channel AC - Transparent TOH from parallel data
0x30052	0xFF	Channel AB - Transparent TOH from parallel data
0x30068	0x07	Turn on Channel AD in functional mode
0x30069	0xFF	Channel AD - Transparent TOH from parallel data
0x3006A	0xFF	Channel AD - Transparent TOH from parallel data
0x30080	0x07	Turn on Channel BA functional mode
0x30081	0xFF	Channel BA- Transparent TOH from parallel data
0x30082	0xFF	Channel AD - Transparent TOH from parallel data
0x30098	0x07	Turn on Channel BB in functional mode
0x30099	0xFF	Channel BB- Transparent TOH from parallel data
0x3009A	0xFF	Channel BB- Transparent TOH from parallel data
0x300B0	0x07	Turn on Channel BC in functional mode
0x300B1	0xFF	Channel BC- Transparent TOH from parallel data
0x300B2	0xFF	Channel BC - Transparent TOH from parallel data
0x300C8	0x07	Turn on Channel BD in functional mode
0x300C9	0xFF	Channel BD - Transparent TOH from parallel data
0x300CA	0xFF	Channel BD - Transparent TOH from parallel data

Figure 13. SONET Overhead Bytes



When used in true SONET applications, most TOH bytes would be generated in the FPGA logic or by an external device. The TOH bytes have the following functions. Table 9 and Table 10 show how the Embedded Core modifies these bytes in the transmit direction and Table 12 shows how the bytes are modified in the receive direction.

Section Overhead Bytes:

- A1, A2 - These bytes are used for framing and to mark the beginning of a SONET frame. A1 has the value 0xF6 and A2 has the value 0x28.
- C1/J0 - Section Trace Message - This byte carries the section trace message. The message is interpreted to verify connectivity to a particular node in the network.
- B1 - Section Bit Interleaved Parity (BIP-8) byte - This byte carries the parity information which is used to check for transmission errors in a section. The computed parity value is transmitted in the next frame in the B1 position. It is defined only for the first STS-1 of a STS-N signal. The other bytes have a default value of 0x00 if using serial TOH insertion. In transparent TOH mode the other bytes are passed through from DINxx bus.
- E1 - Section orderwire byte - This byte carries local orderwire information, which provides for a 64 Kbits/s voice channel between two Section Termination Equipment (STE) devices.
- F1 - Section user channel byte - This byte provides a 64 Kbits/s user channel which can be used in a proprietary fashion.
- D1, D2, D3 - Section Data Communications Channel (SDCC) bytes - These bytes provide a 192 Kbits/s channel for transmission of information across STEs. This information could be for control and configuration, status monitoring, alarms, network administration data etc.

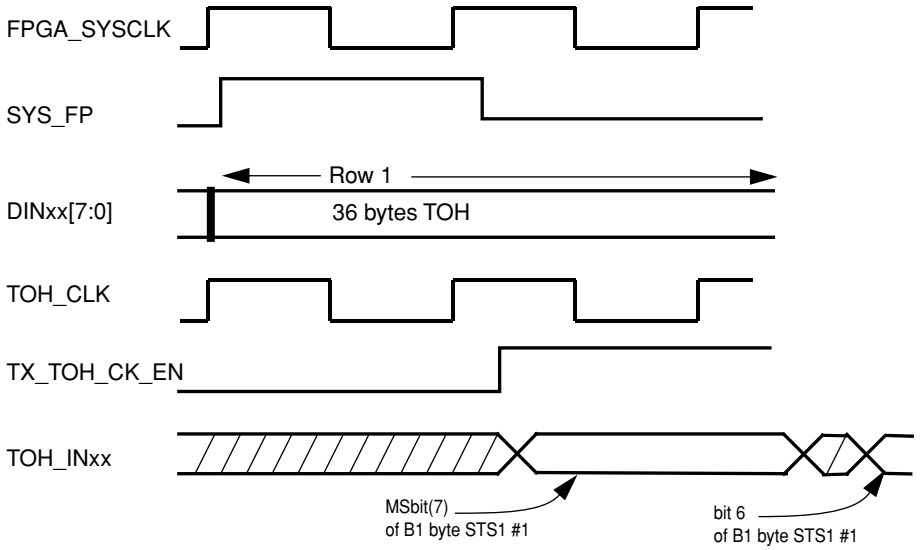
Line Overhead Bytes:

- H1, H2 - STS Payload Pointers (H1 and H2) - These bytes are used to locate the start of the SPE in a SONET frame. These two bytes contain the offset value, in bytes, between the pointer bytes and the start of the SPE. These bytes are used for all the STS-1 signals contained in an STS-N signal to indicate the individual starting positions of the SPEs. They bytes also contain justification indications, concatenation indications and path alarm indication (AIS-P).
- H3 - Pointer Action Byte (H3) - This byte is used during frequency justifications. When a negative justification is

Serial TOH Insertion Mode

In the transmit direction the SPE bytes are always transferred unaltered from the input parallel bus to the serial LVDS output. On the other hand, TOH bytes are received from the serial input port and are inserted in the STS-12 frame before being sent to the LVDS output in the Serial TOH Insertion mode. The FPGA logic must provide framing information to the Core using the TX_TOH_CK_EN Input signal. TOH data is input on a row by row basis, with a one clock cycle frame pulse delineating the start of a row, as shown in Figure 14. As shown in the figure, while the SPE bytes are being transmitted for one row, the FPGA logic must simultaneously supply the Core with the TOH data for the next row. Detailed timing for the TOH serial input is shown later in Figure 31.

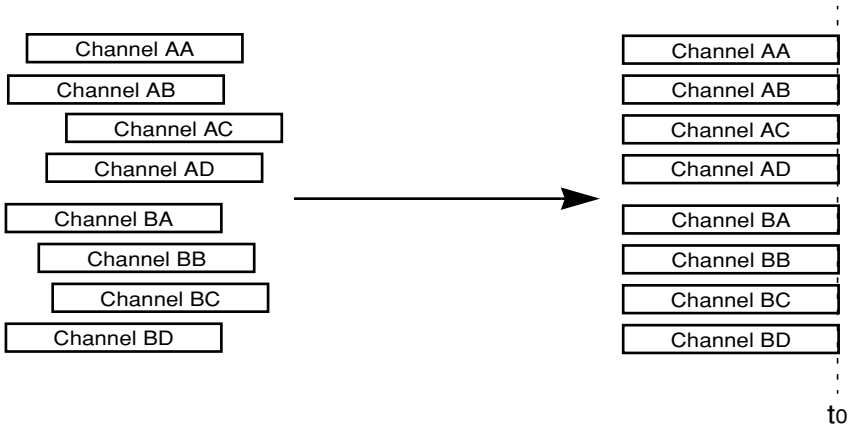
Figure 14. TOH Serial Port Input Framing Signals (FPGA to Core)



Incoming serial TOH data is synchronized initially to the free running clock, TOH_CLK. TOH_CLK can operate from a minimum frequency of 25 Mhz. to a maximum frequency of 106 MHz. TOH bytes are transferred in the order shown in Figure 15. Bytes are transferred over the serial links with the MSB first. Data should be transferred over the serial link on a row-by-row basis. With three TOH bytes/per row for each STS-1 stream and a total of 12 STS-1 streams per STS-12 frame, a total of 288 TOH bits must be transferred for each row. The 288 TOH bits per row can be sent back-to-back. In this case, TX_TO_CLK_EN will be high continuously for 288 TOH_CLK cycles.

It is the responsibility of the user to synchronize transfer of the TOH bytes to a pre-determined window of time relative to the STS-12 frame position on the parallel input bus, i.e., the 36 TOH bytes to be inserted in row number n must be transferred to the Core during the time the SPE bytes of row n-1 are being transferred to the Core over the parallel input bus. Within each SPE row, a guard band of four TOH_CLK cycles must be provided on each side of the TOH transfer window. No data may be transferred in these guard bands.

Figure 20. Alignment of all Eight SERDES Channels.



There is a provision to allow certain streams to be disabled (i.e. not producing alarms or affecting synchronization). These streams can be enabled at a later time without disrupting other streams. If the newly enabled stream needs to be a part of a bigger group the entire group must be resynchronized unless the affected stream was active when the initial synchronization was performed. As long as all streams to be aligned were active when the most recent synchronization was performed, individual streams may be enabled or disabled without affecting synchronization.

It is recommended that users select the smallest possible groups for channel alignment. If an application only requires that two channels be aligned then it is best to use by-2 grouping. All of the channels in a group will affect the group's total alignment. If a channel in a group fails or is shut down it will not affect any of the other channels in the group. This channel will simply be removed from the alignment algorithm. When the channel is re-enabled into a working group it will be out of alignment with the rest of the group. It will be necessary to perform a FIFO realignment procedure to realign the group. During a FIFO realignment data will not pass through any of the channels in the alignment group.

Alignment FIFO Algorithm

The algorithm controlling writes to the alignment FIFO and reads from it operates as follows: Prior to detecting the first frame pulse for a link being aligned, each link in the group continually writes to address 0 within its own FIFO (each link has a FIFO). When the first link in the group receives a frame pulse from Framer block the write pointer for the corresponding FIFO increments to next write address on each clock cycle. L inks that have not received a frame pulse continue to write into their respective FIFOs. When any link receives a frame pulse, the write address for that FIFO will be reset to '0'

The operation of the alignment algorithm requires a wait of several clocks from the first arriving frame pulse before reading of FIFO data begins. In this case, when all frame pulses arrive together the alignment algorithm initiates reads after 9 clocks cycles. If, however, the first to last arriving frame pulses are separated by multiple clock cycles, there will be additional clock cycles between the first frame pulse and the first read. If all links in the group have not reported a valid frame pulse signal after 18 clock cycles, an out of sync state is entered and an alarm is generated.

After all links have received frame pulses and are incrementing their write addresses while writing into their FIFOs, data is then read out of each link's FIFO one byte at a time. All aligned links are now Frame/byte/bit synchronous.

FIFO Alignment Procedure

The FIFO alignment block has the ability to be realigned by changing the value of bits in the alignment control registers. This may be done in the FPGA logic or under the control of an external device through the system bus or MPI. Alignment must take place after the stream has settled with valid data to guarantee proper channel alignment and uncorrupted data transmission.

Channel realignment must occur when a channel goes from the Out-Of-Frame (OOF) state to the In-Frame state. This happens when the channels are first powered up and given a valid frame pulse. This is the obvious known

Table 19. Memory Map Descriptions

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
30000	[0:7]	R	-	05	Internal device revision
30001	[0:7]	R	-	80	Internal device revision
30002	[0:7]	R	-	80	Internal device revision
30003	[0:7]	R/W	scratch pad	00	The scratch pad has no function and is not used anywhere in the core. However, this register can be written to and read from for debugging purposes.
30004	[0:7]	R/W	lockreg MSB	00	In order to write to registers in memory locations 0x30006 to 0x300FF, lockreg MSB and lockreg LSB must be respectively set to the values of 05 and 80. If the MSB and LSB lockreg values are not set to {05, 80}, then any values written to the registers in memory locations 0x30006 to 0x300FF will be ignored. After reset (both hard and soft), the core is in a write locked mode. The core needs to be unlocked before it can be written to. Also note that the scratch pad register (0 x 30003) can always be written to as it is unaffected by write lock mode.
30005	[0:7]	R/W	lockreg LSB	00	
30006	[0]	R/W	global reset	0	The global reset is a soft (software initiated) reset which will have the exact reset effect as a hard (RST_N pin) reset.This is a pulse register and does not have to be cleared.
	[1-7]	-	Not Used	0	
30007	[0:7]	-	Not Used	00	
Device Register Blocks					
30008	[0]	R/W	LVDS loopback control	0	0 = No Loopback 1 = LVDS loopback, transmit to receive. TX serial data is looped back to the RX serial input. TX data is still available at the TX pins
	[1]	-	Not Used	0	
	[2]	-	Not Used	0	
	[3]	R/W	LVDS Protection Switch enable	0	0 = Protection switching performed via bit settings in registers 0x30037 etc. 1 = Protection switching performed via hardware pins LVDS_PROT_SWITCH_xx
	[4]	R/W	TOH RX serial enable	0	TOH_CK_FP_EN signal
	[5-7]	-	Not Used	0	

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
30019	[0:7]	-	Not Used	00	
Channel Register Blocks					
30020* 30038 30050 30068 30080 30098 300B0 300C8	[0]	R/W	AIS-L insert in OOF	0	0 = When RX direction OOF occurs, do not insert AIS-L. 1 = When RX direction OOF occurs, insert AIS-L.
	[1]	R/W	AIS-L control	0	0 = Do not force AIS-L insert 1 = Always force AIS-L insert
	[2]	R/W	TOH output parity error insert	0	0 = Do not insert a parity error 1 = Insert parity error in parity bit of receive TOH serial output for as long as this bit is set
	[3]	R/W	RX K1/K2 source select	0	0 = Set receive direction K1 K2 bytes to 0. 1 = Pass receive direction K1 K2 through pointer mover.
	[4]	R/W	DOUTxx bus parity error insert	0	0 = Do not insert parity error. 1 = Insert parity error in DOUTxx_PAR for as long as this bit is set.
	[5]	R/W	channel enable/disable control	0	0 = Power down CDR channels 1 = Functional mode.
	[6]	R/W	DOUTxx_EN	0	DOUTxx_EN signal
	[7]	R/W	TOH_EN	0	TOHxx_EN signal
30021* 30039 30051 30069 30081 30099 300B1 300C9	[0]	R/W	D9 source select	0	0 = Insert D9 from TOH_INxx 1 = Pass through D9 from DINxx
	[1]	R/W	D10 source select	0	0 = Insert D10 from TOH_INxx 1 = Pass through D10 from DINxx
	[2]	R/W	D11 source select	0	0 = Insert D11 from TOH_INxx 1 = Pass through D11 from DINxx
	[3]	R/W	D12 source select	0	0 = Insert D12 from TOH_INxx 1 = Pass through D12 from DINxx
	[4]	R/W	K1 K2 source select	0	0 = Insert K1, K2 from TOH_INxx 1 = Pass through K1, K2 from DINxx
	[5]	R/W	S1 M0 source select	0	0 = Insert S1, M0, from TOH_INxx 1 = Pass through S1 M0 of DINxx
	[6]	R/W	E1 F1 E2 source select		0 = Insert E1, F1, E2 from TOH_INxx on FPGA interface 1 = Pass through E1, F1, E2 TOH bytes of DINxx
	[7]	R/W	TOH source select	0	0 = Insert TOH from TOH_INxx on FPGA interface for transmit 1 = Pass through all TOH DINxx for transmit
30022* 3003A 30052 3006A 30082 3009A 300B2 300CA	[0:7]	R/W	D1~D8 source select	00	0 = Insert TOH for transmit from TOH_INxx from the FPGA interface. 1 = Pass through D1~D8 TOH bytes from DINxx.

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
3002B* 30043 3005B 30073 3008B 300A3 300BB 300D3	[0:7]	R	AIS alarm flags 1, 4, 7, 10, 2, 5, 8, 11	00	These are the AIS-P alarm flags. 1 if the LVDS input STS # contains AIS.
3002C* 30044 3005C 30074 3008C 300A4 300BC 300D4	[0:3]	R/W	enable AIS alarm 3, 6, 9, 12	0	Enable bits for AIS alarms. Set to 1 to enable and propagate the alarm to register 0x30026.
	[4-7]	-	Not Used	0	
3002D* 30045 3005D 30075 3008D 300A5 300BD 300D5	[0:7]	R/W	AIS alarm enable 1, 4, 7, 10, 2, 5, 8, 11	00	Enable bits for AIS alarms. Set to 1 to enable and propagate the alarm to register 0x30026.
3002E* 30046 3005E 30076 3008E 300A6 300BE 300D6	[0:3]	R	Pointer mover elastic store overflow flags 12, 9, 6, 3	0	Per STS-1 pointer mover elastic store overflow alarm flags. This alarm will propagate to 0x30026 bit 2 when enabled
	[4-7]	-	Not Used	0	
3002F* 30047 3005F 30077 3008F 300A7 300BF 300D7	[0:7]	R	Pointer mover elastic store overflow flags 4, 7, 10, 2, 5, 8, 11	00	Per STS-1 pointer mover elastic store overflow alarm flags. This alarm will propagate to 0x30026 bit 2 when enabled
30030* 30048 30060 30078 30090 300A8 300C0 300D8	[0:3]	R/W	enable elastic store overflow flag 12, 9, 6, 3	0	Enable Bit for elastic store alarms. Set 1 to enable alarm and propagate alarm to register 0x30026
	[4-7]	-	Not Used	0	

HSI Electrical and Timing Characteristics

Table 22. Maximum Power Dissipation

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Dissipation	SERDES, scrambler/descrambler, framer, FIFO alignment, pointer mover, and I/O (per channel), 622 Mbtis/s	—	—	125	mW

1. With all channels operating, 1.575 V and 3.6 V supplies, 85ºC.

Table 23. Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{DD}15$ Supply Voltage	—	1.425	—	1.575	V
Junction Temperature	T_J	–40	—	125	°C

Table 24. Receiver Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Data					
Stream of Nontransitions [1]	—	—	—	72	bits
Phase Change, Input Signal	Over a 200 ns time interval [2]	—	—	100	ps
Eye Opening[3]	—	0.4	—	—	UIp-p
Jitter Tolerance @ 622 Mbits/s, Worst Case	300 MV diff eye[4]	—	—	0.6	UIp-p
Jitter Tolerance @ 155 Mbits/s, Worst Case	250 MV diff eye[5]	—	—	0.85	UIp-p

1. This sequence should not occur more than once per minute.
2. Translates to a frequency change of 500 ppm.
3. A unit interval for 622.08 Mbits/s data is 1.6075 ns.
4. With STS-12 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., TA=0°C to 85°C, 1.425 V to 1.575 V supply. Jitter measured with a Wavecrest SIA-3000.
5. With STS-3 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., TA=0°C to 85°C, 1.425 V to 1.575 V supply. Jitter measured with a Wavecrest SIA-3000.

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
AB1	7 (CL)	6	IO	PL17A	PL29C	A7/PPC_A21	L20T_D3
AA5	7 (CL)	6	IO	PL18D	PL30D	A6/PPC_A20	L21C_A1
AA3	7 (CL)	6	IO	PL18C	PL30C	A5/PPC_A19	L21T_A1
U1	7 (CL)	—	VDDIO7	VDDIO7	VDDIO7	—	—
AB2	7 (CL)	7	IO	PL18B	PL31D	—	—
AA4	7 (CL)	7	IO	PL19D	PL32D	WR_N/MPI_RW	L22C_D2
AC1	7 (CL)	7	IO	PL19C	PL32C	VREF_7_07	L22T_D2
AB5	7 (CL)	7	IO	PL19B	PL33D	—	L23C_D2
AC2	7 (CL)	7	IO	PL19A	PL33C	—	L23T_D2
AB4	7 (CL)	8	IO	PL20D	PL34D	A4/PPC_A18	L23C_D0
AC5	7 (CL)	8	IO	PL20C	PL34C	VREF_7_08	L23T_D0
W1	7 (CL)	—	VDDIO7	VDDIO7	VDDIO7	—	—
AD2	7 (CL)	8	IO	PL20B	PL35D	A3/PPC_A17	L23C_D0
AE1	7 (CL)	8	IO	PL20A	PL35C	A2/PPC_A16	L23T_D0
AD3	7 (CL)	8	IO	PL21D	PL36D	A1/PPC_A15	L24C_D0
AE2	7 (CL)	8	IO	PL21C	PL36C	A0/PPC_A14	L24T_D0
AF1	7 (CL)	8	IO	PL21B	PL37D	DP0	L25C_D2
AD4	7 (CL)	8	IO	PL21A	PL37C	DP1	L25T_D2
AE3	6 (BL)	1	IO	PL22D	PL38D	D8	L1C_D0
AF2	6 (BL)	1	IO	PL22C	PL38C	VREF_6_01	L1T_D0
AB13	—	—	VSS	VSS	VSS	—	—
AE4	6 (BL)	1	IO	PL22B	PL39D	D9	L2C_D0
AF3	6 (BL)	1	IO	PL22A	PL39C	D10	L2T_D0
AE5	6 (BL)	2	IO	PL23D	PL40D	—	L3C_D1
AG2	6 (BL)	2	IO	PL23C	PL40C	VREF_6_02	L3T_D1
AK5	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AH1	6 (BL)	2	IO	PL23B	PL41D	—	L4C_D3
AF5	6 (BL)	2	IO	PL23A	PL41C	—	L4T_D3
AF4	6 (BL)	3	IO	PL24D	PL42D	D11	L5C_D0
AG3	6 (BL)	3	IO	PL24C	PL42C	D12	L5T_D0
AB14	—	—	VSS	VSS	VSS	—	—
AH2	6 (BL)	3	IO	PL24B	PL43D	—	L6C_D0
AJ1	6 (BL)	3	IO	PL24A	PL43C	—	L6T_D0
AG4	6 (BL)	3	IO	PL25D	PL44D	VREF_6_03	L7C_A0
AG5	6 (BL)	3	IO	PL25C	PL44C	D13	L7T_A0
AL3	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AH3	6 (BL)	4	IO	PL25B	PL44B	—	—
AK1	6 (BL)	4	IO	PL25A	PL45A	—	—
AJ2	6 (BL)	4	IO	PL26D	PL45D	—	L8C_D2
AH5	6 (BL)	4	IO	PL26C	PL45C	VREF_6_04	L8T_D2
AB15	—	—	VSS	VSS	VSS	—	—
AH4	6 (BL)	4	IO	PL26B	PL46D	—	—

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
AJ3	6 (BL)	4	IO	PL26A	PL46A	—	—
AK2	6 (BL)	4	IO	PL27D	PL47D	PLL_CK7C/HPPLL	L9C_D0
AL1	6 (BL)	4	IO	PL27C	PL47C	PLL_CK7T/HPPLL	L9T_D0
AB20	—	—	VSS	VSS	VSS	—	—
AJ5	6 (BL)	4	IO	PL27B	PL47B	—	L10C_A0
AJ4	6 (BL)	4	IO	PL27A	PL47A	—	L10T_A0
AB21	—	—	VSS	VSS	VSS	—	—
AK3	—	—	I	PTEMP	PTEMP	PTEMP	—
AM1	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AL2	—	—	IO	LVDS_R	LVDS_R	LVDS_R	—
AK4	—	—	VDD33	VDD33	VDD33	—	—
AB22	—	—	VSS	VSS	VSS	—	—
AK6	—	—	VDD33	VDD33	VDD33	—	—
AL5	6 (BL)	5	IO	PB2A	PB2A	DP2	L11T_D1
AN4	6 (BL)	5	IO	PB2B	PB2B	—	L11C_D1
AM2	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AM5	6 (BL)	5	IO	PB2C	PB2C	PLL_CK6T/PPLL	L12T_D1
AK7	6 (BL)	5	IO	PB2D	PB2D	PLL_CK6C/PPLL	L12C_D1
AL6	6 (BL)	5	IO	PB3A	PB3C	—	L13T_D1
AN5	6 (BL)	5	IO	PB3B	PB3D	—	L13C_D1
AM4	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AM6	6 (BL)	5	IO	PB3C	PB4C	VREF_6_05	L14T_D0
AL7	6 (BL)	5	IO	PB3D	PB4D	DP3	L14C_D0
AK8	6 (BL)	6	IO	PB4A	PB5C	—	L15T_D3
AP5	6 (BL)	6	IO	PB4B	PB5D	—	L15C_D3
AB32	—	—	VSS	VSS	VSS	—	—
AK9	6 (BL)	6	IO	PB4C	PB6C	VREF_6_06	L16T_D2
AN6	6 (BL)	6	IO	PB4D	PB6D	D14	L16C_D2
AM7	6 (BL)	6	IO	PB5A	PB7C	—	L17T_D1
AP6	6 (BL)	6	IO	PB5B	PB7D	—	L17C_D1
AN3	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AL8	6 (BL)	7	IO	PB5C	PB8C	D15	L18T_D1
AN7	6 (BL)	7	IO	PB5D	PB8D	D16	L18C_D1
AM8	6 (BL)	7	IO	PB6A	PB9C	D17	L19T_D0
AL9	6 (BL)	7	IO	PB6B	PB9D	D18	L19C_D0
AL4	—	—	VSS	VSS	VSS	—	—
AP7	6 (BL)	7	IO	PB6C	PB10C	VREF_6_07	L20T_D0
AN8	6 (BL)	7	IO	PB6D	PB10D	D19	L20C_D0
AL10	6 (BL)	8	IO	PB7A	PB11C	D20	L21T_D2
AP8	6 (BL)	8	IO	PB7B	PB11D	D21	L21C_D2
AL11	6 (BL)	8	IO	PB7C	PB12C	VREF_6_08	L22T_D0
AM10	6 (BL)	8	IO	PB7D	PB12D	D22	L22C_D0

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
AK12	6 (BL)	9	IO	PB8A	PB13A	—	L23T_D3
AP9	6 (BL)	9	IO	PB8B	PB13B	—	L23C_D3
AL31	—	—	VSS	VSS	VSS	—	—
AN10	6 (BL)	9	IO	PB8C	PB13C	D23	L24T_D1
AL12	6 (BL)	9	IO	PB8D	PB13D	D24	L24C_D1
AM11	6 (BL)	9	IO	PB9A	PB14A	—	L25T_D1
AP10	6 (BL)	9	IO	PB9B	PB14B	—	L25C_D1
AP3	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AK13	6 (BL)	9	IO	PB9C	PB14C	VREF_6_09	L26T_D2
AN11	6 (BL)	9	IO	PB9D	PB14D	D25	L26C_D2
AL13	6 (BL)	9	IO	PB10A	PB15C	—	L27T_D0
AK14	6 (BL)	9	IO	PB10B	PB15D	—	L27C_D0
AM3	—	—	VSS	VSS	VSS	—	—
AN12	6 (BL)	10	IO	PB10C	PB16C	D26	L28T_D1
AL14	6 (BL)	10	IO	PB10D	PB16D	D27	L28C_D1
AP12	6 (BL)	10	IO	PB11A	PB17C	—	L29T_D0
AN13	6 (BL)	10	IO	PB11B	PB17D	—	L29C_D0
AP13	6 (BL)	10	IO	PB11C	PB18C	VREF_6_10	L30T_D3
AK15	6 (BL)	10	IO	PB11D	PB18D	D28	L30C_D3
AL15	6 (BL)	11	IO	PB12A	PB19C	D29	L31T_D0
AK16	6 (BL)	11	IO	PB12B	PB19D	D30	L31C_D0
AM13	—	—	VSS	VSS	VSS	—	—
AP14	6 (BL)	11	IO	PB12C	PB20C	VREF_6_11	L32T_D2
AL16	6 (BL)	11	IO	PB12D	PB20D	D31	L32C_D2
AN15	5 (BC)	1	IO	PB13C	PB21A	—	—
AP15	5 (BC)	1	IO	PB14A	PB21C	—	L1T_D3
AK17	5 (BC)	1	IO	PB14B	PB21D	—	L1C_D3
Y15	—	—	VSS	VSS	VSS	—	—
AM16	5 (BC)	1	IO	PB14C	PB22A	—	—
AN16	5 (BC)	1	IO	PB15A	PB22C	VREF_5_01	L2T_D1
AL17	5 (BC)	1	IO	PB15B	PB22D	—	L2C_D1
AM12	5 (BC)	—	VDDIO5	VDDIO5	VDDIO5	—	—
AP16	5 (BC)	2	IO	PB15C	PB23A	—	L3T_D1
AM17	5 (BC)	2	IO	PB15D	PB23B	—	L3C_D1
AN17	5 (BC)	2	IO	PB16A	PB23C	PBCK0T	L4T_D1
AL18	5 (BC)	2	IO	PB16B	PB23D	PBCK0C	L4C_D1
AN18	5 (BC)	2	IO	PB16C	PB24A	—	L5T_A0
AM18	5 (BC)	2	IO	PB16D	PB24B	—	L5C_A0
AN19	5 (BC)	2	IO	PB17A	PB24C	VREF_5_02	L6T_D2
AK18	5 (BC)	2	IO	PB17B	PB24D	—	L6C_D2
Y20	—	—	VSS	VSS	VSS	—	—
AM19	5 (BC)	2	IO	PB17C	PB25C	—	L7T_A0

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
T32	—	—	O	TXDAA_W_N	TXDAA_W_N	—	L32N_D1
R34	—	—	O	TXDAA_W_P	TXDAA_W_P	—	L32P_D1
AM33	—	—	VDD33	VDD33	VDD33	—	—
U30	—	—	O	TXDAB_W_N	TXDAB_W_N	—	L33N_D0
T31	—	—	O	TXDAB_W_P	TXDAB_W_P	—	L33P_D0
V17	—	—	VSS	VSS	VSS	—	—
R33	—	—	O	TXDAC_W_N	TXDAC_W_N	—	L34N_D0
P34	—	—	O	TXDAC_W_P	TXDAC_W_P	—	L34P_D0
AM34	—	—	VDD33	VDD33	VDD33	—	—
P33	—	—	O	TXDAD_W_N	TXDAD_W_N	—	L35N_D0
N34	—	—	O	TXDAD_W_P	TXDAD_W_P	—	L35P_D0
V18	—	—	VSS	VSS	VSS	—	—
T30	—	—	O	Reserved	Reserved	—	L36N_D0
R31	—	—	O	Reserved	Reserved	—	L36P_D0
AN32	—	—	VDD33	VDD33	VDD33	—	—
P32	—	—	O	Reserved	Reserved	—	L37N_D1
R30	—	—	O	Reserved	Reserved	—	L37P_D1
V19	—	—	VSS	VSS	VSS	—	—
N33	—	—	O	TXDBA_W_N	TXDBA_W_N	—	L38N_D0
M34	—	—	O	TXDBA_W_P	TXDBA_W_P	—	L38P_D0
AP32	—	—	VDD33	VDD33	VDD33	—	—
P31	—	—	O	TXDBB_W_N	TXDBB_W_N	—	L39N_D1
M33	—	—	O	TXDBB_W_P	TXDBB_W_P	—	L39P_D1
V34	—	—	VSS	VSS	VSS	—	—
N31	—	—	O	TXDBC_W_N	TXDBC_W_N	—	L40N_D0
P30	—	—	O	TXDBC_W_P	TXDBC_W_P	—	L40P_D0
L33	—	—	O	TXDBD_W_N	TXDBD_W_N	—	L41N_D0
K34	—	—	O	TXDBD_W_P	TXDBD_W_P	—	L41P_D0
W16	—	—	VSS	VSS	VSS	—	—
M31	—	—	I	Reserved	Reserved	—	L42N_D0
L32	—	—	I	Reserved	Reserved	—	L42P_D0
K33	—	—	I	Reserved	Reserved	—	—
W17	—	—	VSS	VSS	VSS	—	—
N30	—	—	VDDA_PDI	Reserved	Reserved	—	—
L30	—	—	VSSA_PDI	Reserved	Reserved	—	—
W18	—	—	VSS	VSS	VSS	—	—
M30	—	—	I	Reserved	Reserved	—	L43N_D0
L31	—	—	I	Reserved	Reserved	—	L43P_D0
W19	—	—	VSS	VSS	VSS	—	—
J34	—	—	I	Reserved	Reserved	—	L44N_D1
K32	—	—	I	Reserved	Reserved	—	L44P_D1
J33	—	—	I	Reserved	Reserved	—	—

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
D19	1 (TC)	4	IO	PT19C	PT26C	—	L11T_D0
C19	1 (TC)	4	IO	PT19B	PT25D	—	L12C_A0
B19	1 (TC)	4	IO	PT19A	PT25C	—	L12T_A0
N3	—	—	VSS	VSS	VSS	—	—
E19	1 (TC)	4	IO	PT18D	PT24D	—	L13C_D0
D18	1 (TC)	4	IO	PT18C	PT24C	VREF_1_04	L13T_D0
A17	1 (TC)	—	VDDIO1	VDDIO1	VDDIO1	—	—
B18	1 (TC)	4	IO	PT18B	PT24B	—	L14C_A0
C18	1 (TC)	4	IO	PT18A	PT24A	—	L14T_A0
B17	1 (TC)	5	IO	PT17D	PT23D	PTCK1C	L15C_A0
C17	1 (TC)	5	IO	PT17C	PT23C	PTCK1T	L15T_A0
N13	—	—	VSS	VSS	VSS	—	—
A16	1 (TC)	5	IO	PT17B	PT23B	—	L16C_D2
D17	1 (TC)	5	IO	PT17A	PT23A	—	L16T_D2
B16	1 (TC)	5	IO	PT16D	PT22D	PTCK0C	L17C_A0
C16	1 (TC)	5	IO	PT16C	PT22C	PTCK0T	L17T_A0
D16	1 (TC)	5	IO	PT16A	PT22A	—	—
E18	1 (TC)	5	IO	PT15D	PT21D	VREF_1_05	L18C_D3
A15	1 (TC)	5	IO	PT15C	PT21C	—	L18T_D3
A19	1 (TC)	—	VDDIO1	VDDIO1	VDDIO1	—	—
B15	1 (TC)	5	IO	PT15A	PT21A	—	—
D15	1 (TC)	6	IO	PT14D	PT20D	—	L19C_D2
A14	1 (TC)	6	IO	PT14C	PT20C	—	L19T_D2
N14	—	—	VSS	VSS	VSS	—	—
B14	1 (TC)	6	IO	PT14A	PT20A	—	—
E17	1 (TC)	6	IO	PT13D	PT19D	—	L20C_D2
C14	1 (TC)	6	IO	PT13C	PT19C	VREF_1_06	L20T_D2
D14	1 (TC)	6	IO	PT13A	PT19A	—	—
N15	—	—	VSS	VSS	VSS	—	—
E16	0 (TL)	1	IO	PT11D	PT18D	MPI_RTRY_N	L1C_D3
A13	0 (TL)	1	IO	PT11C	PT18C	MPI_ACK_N	L1T_D3
B13	0 (TL)	1	IO	PT11B	PT17D	—	L2C_D0
A12	0 (TL)	1	IO	PT11A	PT17C	VREF_0_01	L2T_D0
B12	0 (TL)	1	IO	PT10D	PT16D	M0	L3C_D1
D13	0 (TL)	1	IO	PT10C	PT16C	M1	L3T_D1
A34	—	—	VSS	VSS	VSS	—	—
E15	0 (TL)	2	IO	PT10B	PT15D	MPI_CLK	L4C_D3
B11	0 (TL)	2	IO	PT10A	PT15C	A21/MPI_BURST_N	L4T_D3
A10	0 (TL)	2	IO	PT9D	PT14D	M2	L5C_D3
E14	0 (TL)	2	IO	PT9C	PT14C	M3	L5T_D3
A3	0 (TL)	—	VDDIO0	VDDIO0	VDDIO0	—	—
D12	0 (TL)	2	IO	PT9B	PT13D	VREF_0_02	L6C_D0

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: θ_{JA}, ψ_{JC}, and θ_{JC}. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

θJA

This is the thermal resistance from junction to ambient (theta-JA, R-theta, etc.).

$$\theta_{JA} = \frac{T_J - T_A}{Q} \quad (1)$$

where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, θJA is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that θJA is expressed in units of °C/watt.

ΨJC

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance, and it is defined by:

$$\Psi_{JC} = \frac{T_J - T_C}{Q} \quad (2)$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the θJA measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψJC is also expressed in units of °C/W.

θJC

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\theta_{JC} = \frac{T_J - T_C}{Q} \quad (3)$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates θJC from ψJC. θJC is a true thermal resistance and is expressed in units of °C/W.

θJB

This is the thermal resistance from junction to board (ΘJL). It is defined by:

$$\theta_{JB} = \frac{T_J - T_B}{Q} \quad (4)$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads. Note that θJB is expressed in units of °C/W and that this parameter and the way it is measured are still being discussed by the JEDEC committee.

Ordering Information

Figure 41. Part Number Description

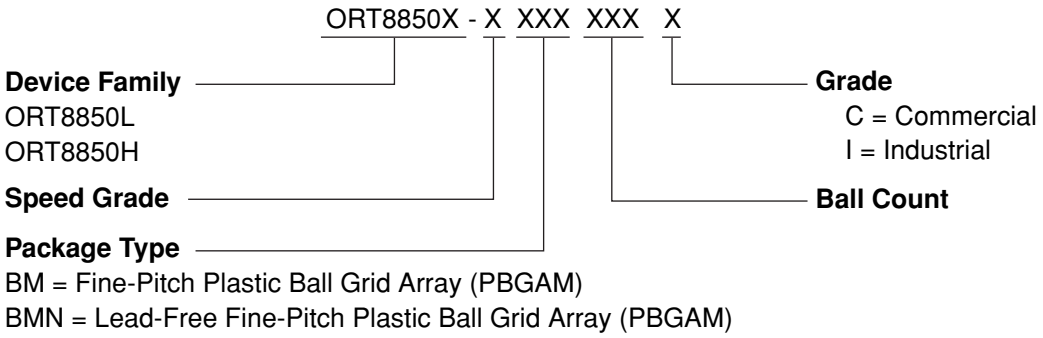


Table 40. Device Type Options

Device	Voltage
ORT8850L	1.5 V internal 3.3 V/2.5 V/1.8 V/1.5 V I/O
ORT8850H	1.5 V internal 3.3 V/2.5 V/1.8 V/1.5 V I/O

Table 41. Temperature Range

Symbol	Description	Ambient Temperature	Junction Temperature
C	Commercial	0 ˚C to +70 ˚C	0 ˚C to +85 ˚C
I	Industrial	–40 ˚C to +85 ˚C	–40 ˚C to +100 ˚C

Table 42. Conventional Packaging – Commercial Ordering Information[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT8850L	ORT8850L-3BM680C	3	PBGAM (fpBGA)	680	C
	ORT8850L-2BM680C	2	PBGAM (fpBGA)	680	C
	ORT8850L-1BM680C	1	PBGAM (fpBGA)	680	C
ORT8850H	ORT8850H-2BM680C	2	PBGAM (fpBGA)	680	C
	ORT8850H-1BM680C	1	PBGAM (fpBGA)	680	C

Table 43. Conventional Packaging – Industrial Ordering Information[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT8850L	ORT8850L-2BM680I	2	PBGAM (fpBGA)	680	I
	ORT8850L-1BM680I	1	PBGAM (fpBGA)	680	I
ORT8850H	ORT8850H-1BM680I	1	PBGAM (fpBGA)	680	I

1.For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.

Table 44. Lead-Free Packaging – Commercial Ordering Information[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT8850L	ORT8850L-3BMN680C	3	Lead-Free PBGAM (fpBGA)	680	C
	ORT8850L-2BMN680C	2	Lead-Free PBGAM (fpBGA)	680	C
	ORT8850L-1BMN680C	1	Lead-Free PBGAM (fpBGA)	680	C
ORT8850H	ORT8850H-2BMN680C	2	Lead-Free PBGAM (fpBGA)	680	C
	ORT8850H-1BMN680C	1	Lead-Free PBGAM (fpBGA)	680	C

Table 45. Lead-Free Packaging – Industrial Ordering Information[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT8850L	ORT8850L-2BMN680I	2	Lead-Free PBGAM (fpBGA)	680	I
	ORT8850L-1BMN680I	1	Lead-Free PBGAM (fpBGA)	680	I
ORT8850H	ORT8850H-1BMN680I	1	Lead-Free PBGAM (fpBGA)	680	I

1.For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.

Revision History

Date	Version	Change Summary
–	8	Previous Lattice releases.
January 2004	8.1	Added lead-free package designator.
August 2004	9	Added lead-free package ordering part numbers (OPNs).
October 2005	10	Added clarification to the STM Pointer Mover bypass. Added clarification to the signal description for LINE_FP.
April 2006	11	Added clarification to the B1, section bit interleavered parity (BIP-8) byte. Added clarification to B1 processing.
February 2008	11.1	Corrected name of Register 30009, Bits 5 & 6 in Memory Map Description table.