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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	4992
Total RAM Bits	75776
Number of I/O	278
Number of Gates	397000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort8850l-2bm680i

- Meets Universal Test and Operations PHY Interface for ATM (UTOPIA) Levels 1, 2, and 3. Also meets proposed specifications for UTOPIA Level 4 POS-PHY, Level 3 (2.5 Gbits/s), and POS-PHY 4 (10 Gbits/s) interface standards for Packet-over-SONET as defined by the Saturn Group.
- ispLEVER development system software. Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.

Description

What is an FPSC?

FPSCs, or Field Programmable System-on-a-Chip devices, are devices that combine field-programmable logic with ASIC or mask-programmed logic on a single device. FPSCs provide the time to market and the flexibility of FPGAs, the design effort savings of using soft Intellectual Property (IP) cores, and the speed, design density, and economy of ASICs.

FPSC Overview

Lattice's Series 4 FPSCs are created from Series 4 *ORCA* FPGAs. To create a Series 4 FPSC, several columns of Programmable Logic Cells (see FPGA Logic Overview section for FPGA logic details) are added to an embedded logic core. Other than replacing some FPGA gates with ASIC gates, at greater than 10:1 efficiency, none of the FPGA functionality is changed—all of the Series 4 FPGA capability is retained: embedded block RAMs, MPI, PCMs, boundary scan, etc. Columns of programmable logic are replaced on one side of the device, allowing pins from the replaced columns to be used as I/O pins for the embedded core. The remainder of the device pins retain their FPGA functionality.

FPSC Gate Counting

The total gate count for an FPSC is the sum of its embedded core (standard-cell/ASIC gates) and its FPGA gates. Because FPGA gates are generally expressed as a usable range with a nominal value, the total FPSC gate count is sometimes expressed in the same manner. Standard-cell ASIC gates are, however, 10 to 25 times more silicon-area efficient than FPGA gates. Therefore, an FPSC with an embedded function is gate equivalent to an FPGA with a much larger gate count.

FPGA/Embedded Core Interface

The interface between the FPGA logic and the embedded core has been enhanced to provide a greater number of interface signals than on previous FPSC architectures. Compared to bringing embedded core signals off-chip, this on-chip interface is much faster and requires less power.

Series 4 based FPSCs expand this interface by providing a link between the embedded block and the multi-master 32-bit system bus in the FPGA logic. This system bus allows the core easy access to many of the FPGA logic functions including the embedded block RAMs and the MicroProcessor Interface.

Clock spines also can pass across the FPGA/embedded core boundary. This allows fast, low-skew clocking between the FPGA and the embedded core. Many of the special signals from the FPGA, such as DONE and global set/reset, are also available to the embedded core, making it possible to fully integrate the embedded core with the FPGA as a system.

For even greater system flexibility, FPGA configuration RAMs are available for use by the embedded core. This supports user-programmable options in the embedded core, in turn allowing greater flexibility. Multiple embedded core configurations may be designed into a single device with user-programmable control over which configurations are implemented, as well as the capability to change core functionality simply by reconfiguring the device.

ispLEVER Development System

The ispLEVER development system is used to process a design from a netlist to a configured FPGA. This system is used to map a design onto the *ORCA* architecture and then place and route it using ispLEVER's timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

The ispLEVER development system interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points in the design flow, the design entry and the bit stream generation stage. Recent improvements in ispLEVER allow the user to provide timing requirement information through logical preferences only; thus, the designer is not required to have physical knowledge of the implementation.

Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPGA. A floor planner is available for layout feedback and control. A static timing analysis tool is provided to determine design speed, and a back-annotated netlist can be created to allow simulation and timing.

Timing and simulation output files from ispLEVER are also compatible with many third-party analysis tools. A bit stream generator is then used to generate the configuration data which is loaded into the FPGAs internal configuration RAM, embedded block RAM, and/or FPSC memory.

When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, ispLEVER produces configuration data that implements the various logic and routing options discussed in this data sheet.

FPSC Design Kit

Development is facilitated by an FPSC design kit which, together with ispLEVER software and third-party synthesis and simulation engines, provides all software and documentation required to design and verify an FPSC implementation. Included in the kit are the FPSC configuration manager, *Synopsys Smart Model*®, and/or compiled *Verilog*® simulation model, *HSPICE*® and/or IBIS models for I/O buffers, and complete online documentation. The kit's software couples with ispLEVER software, providing a seamless FPSC design environment. More information can be obtained by visiting the Lattice website at www.latticesemi.com or contacting a local sales office.

FPGA Logic Overview

The ORCA Series 4 architecture is a new generation of SRAM-based programmable devices from Lattice. It includes enhancements and innovations geared toward today's high-speed systems on a single chip. Designed with networking applications in mind, the Series 4 family incorporates system-level features that can further reduce logic requirements and increase system speed. ORCA Series 4 devices contain many new patented enhancements and are offered in a variety of packages and speed grades.

The hierarchical architecture of the logic, clocks, routing, RAM, and system-level blocks create a seamless merge of FPGA and ASIC designs. Modular hardware and software technologies enable System-on-a-Chip integration with true plug-and-play design implementation.

The architecture consists of four basic elements: Programmable Logic Cells (PLCs), Programmable I/O cells (PIOs), Embedded Block RAMs (EBRs) and system-level features. These elements are interconnected with a rich routing fabric of both global and local wires. An array of PLCs are surrounded by common interface blocks which provide an abundant interface to the adjacent PLCs or system blocks. Routing congestion around these critical blocks is eliminated by the use of the same routing fabric implemented within the programmable logic core. Each PLC contains a PFU, SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PIOs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, uplink and downlink functions, and other functions on two output signals. Large blocks of 512 x 18 quad-port RAM complement the existing distributed PFU memory. The RAM blocks can be used to implement RAM, ROM, FIFO, multiplier, and CAM. Some of the other system-level functions include the MicroProcessor Interface (MPI), Phase-Locked Loops (PLLs), and the Embedded System Bus (ESB).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/flip-flops, and one additional Flip-Flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion; two sets of four LUTs and flip-flops that can be controlled independently. Each PFU has two independent programmable clocks, clock enables, local SET/RESET, and data selects. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth flip-flop for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The flip-flops (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The flip-flops also have programmable clock polarity, clock enables, and local SET/RESET.

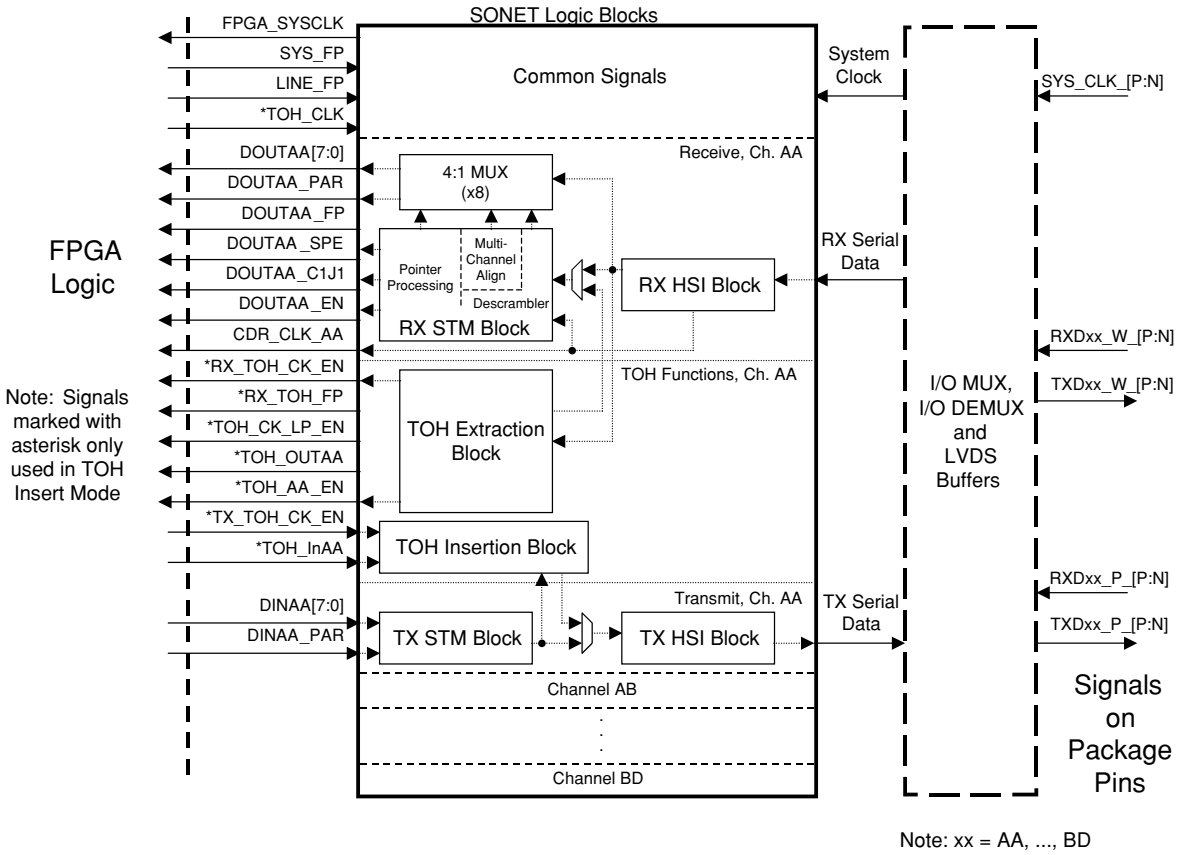
The SLIC is connected from PLC routing resources and from the outputs of the PFU. It contains eight 3-state, bidirectional buffers, and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections from the PFU outputs make fast, true, 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Programmable I/O

The Series 4 PIO addresses the demand for the flexibility to select I/Os that meet system interface requirements. I/Os can be programmed in the same manner as in previous *ORCA* devices, with the additional new features which allow the user the flexibility to select new I/O types that support High-Speed Interfaces.

Each PIO contains four Programmable I/O pads and is interfaced through a common interface block to the FPGA array. The PIO is split into two pairs of I/O pads with each pair having independent clock enables, local SET/RESET, and global SET/RESET. On the input side, each PIO contains a programmable latch/Flip-Flop which enables very fast latching of data from any pad. The combination provides very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer with a PFU. On the output side of each PIO, an output from the PLC array can be routed to each output flip-flop, and logic can be associated

Figure 3. Top Level Block Diagram ORT8850 Embedded Core SONET Logic Block Common Signals and Channel AA Data Flow



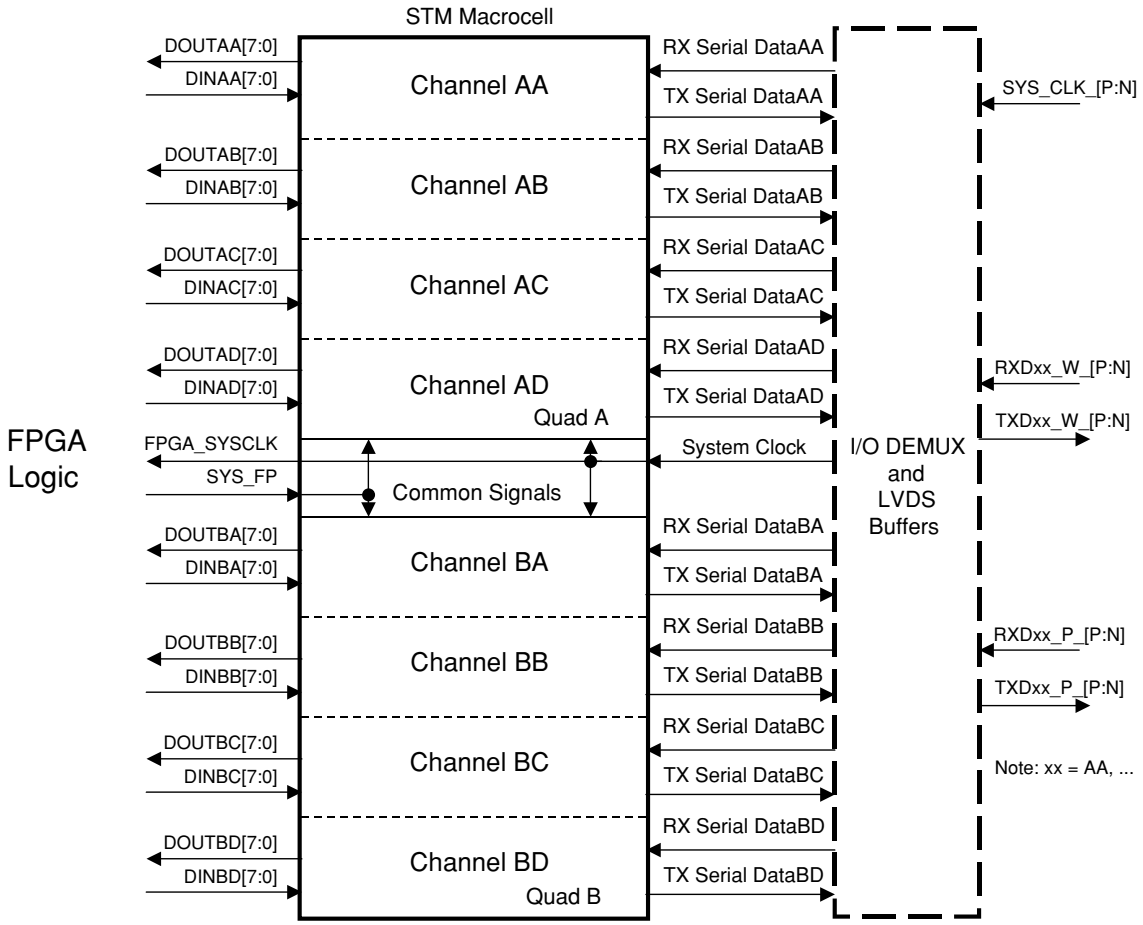
Each quad can frame independently in STS-3, STS-12 or STS-48 format. If using STS-48 format all channels in the quad will be used and be treated as a single STS-48 channel using the quad STS-12 format in which each independent channel carries entire STS-12 frames. The byte order for STS-48 must be created by the designer in the FPGA design. Note that the recovered data will always continue to be in the same order as transmitted data.

Each channel contains transmit path and receive path logic, both of which are organized around High Speed Interconnect (HSI) and Synchronous Transport Mode (STM) macrocells. Additional logic allows insertion and extraction of information in the Transport Overhead area of the SONET frame. (Support for loopback and for switching between redundant serial links is also provided but is not shown in Figure 3). The following sections will give an overview of the pseudo-SONET protocol supported by the ORT8850 and a top level overview of the Synchronous Transport Module (STM) and High Speed Interconnect (HSI) macrocells, which provide the SONET functionality.

STM Macrocells - Overview

The Synchronous Transport Module (STM) portion of the embedded core consists of two quads, STM A and B. The STM macrocells provide transmitter and receiver logic blocks on a per SERDES basis channel and are located in the data path between the FPGA interface and the HSI macrocell. The STM macrocells' main functions are framing and aligning data into standard STS-N frames as well as providing a 1's density through scrambling/descrambling.

Figure 7. STM Macrocell Partitioning



Transmit STM Macrocell Logic - Overview

In the transmit direction (FPGA interface to the backplane), each STM macrocell will receive frame aligned streams of STS-12 data (maximum of four streams) from the FPGA logic. The transmitter receive data interface is in a parallel 8-bit format. A common frame pulse for all 8 channels is provided as an input from the FPGA logic to the transmit SONET block.

On each frame pulse the A1/A2 frame alignment bytes are inserted into the data stream and will overwrite any data in this location of the frame. TOH data can be optionally inserted into the transmitted SONET frame. The SONET frame is then optionally scrambled and sent to the HSI macrocell.

TOH data can be inserted into the transmit data stream in two ways; transparently or by inserting serial TOH data from a TOH serial interface signal in the FPGA logic. In the transparent mode, the SPE and TOH data received on parallel input bus is transferred, unaltered, to the serial LVDS output. However, B1 byte of STS-1 is always replaced with a new calculated value (the 11 bytes following B1 are replaced with all zeros). Likewise, in serial and transport mode A1 and A2 bytes of all STS-1s are always regenerated. In the TOH serial insertion mode the SPE bytes are transferred unaltered from the input parallel bus to the serial LVDS output. TOH bytes, however, are received from the FPGA logic through the serial input port and are inserted in the STS- 12 frame before being sent to the LVDS

Pointer Mover Performance Monitoring: There is Pointer Mover performance monitoring in the Receiver section. Alarm Indication Signals (AIS-P) and elastic store overflows are reported. AIS-P is implemented as a per STS-1 alarm bit. Elastic store overflow will cause an alarm bit to be set on a per STS-1 basis.

FIFO Aligner Monitoring: There is monitoring of the FIFO aligner operating point, and upon deviating from the nominal operating point of the FIFO by more than user programmable threshold values (min and max threshold values), an alarm bit is set. Threshold values are defined per device; alarm flags are per channel.

Frame Offset Monitoring: There is monitoring of the frame offset between all enabled channels (disabled channels do not interfere with the monitoring). Monitoring is performed continuously. Upon exceeding the maximum allowed frame offset (18 bytes) between all enabled channels, an alarm bit is set.

Error Insertion

A1/A2 Error Insert: There is a Frame Error inject feature in the transmitter section, allowing the user to replace framing bytes A1/A2 (only last A1 byte and first A2 byte) with a selectable A1/A2 byte value for a selectable number of consecutive frames. The number of consecutive frames to alter is specified by a 4-bit field, while A1/A2 value is specified by two 8-bit fields. The error insert feature is on a per channel basis, A1/ A2 values and 4-bit frame count value are on a per device basis.

B1 Error Insert: There is a B1 error insert feature in the transmitter section, allowing the user to insert errors on user selectable bits in the B1 byte. Errors are created by simply inverting bit values. Bits to invert are specified through an 8-bit control. To insert an error, software will first set the bits in the "transmitter B1 error insert mask". Then, on a per channel basis software will write a one to the "B1 error insert command". The insertion circuitry performs a rising edge detect on the bit, and will issue a corruption signal for the next frame, for one frame only. This feature is on a per channel basis.

TOH Serial Output Port Parity Error Insert: There is a Parity error inject feature, in the receive section, allowing the user to invert the parity bit of each serial output port. This feature inserts a single error. This feature is on a per channel basis.

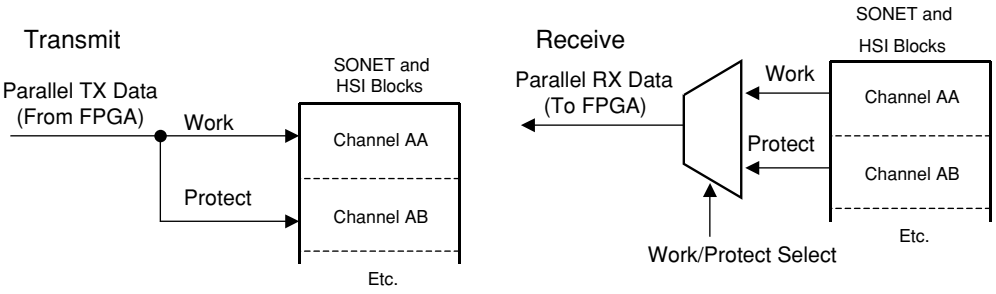
Parallel Output Bus Parity Error Insert: There is a Parity error inject feature, in the receive section, allowing the user to invert parity lines (DOUTxx_PAR) associated with each output parallel busses (DOUTxx[7:0]). This feature inserts a single error. This feature is on a per channel basis. This feature supports both 'even' and 'odd' parities.

Loopback

There are two types of loopback that can be utilized inside the embedded ASIC core of the ORT8850, near end loopback and far end (line side) loopback. Both of these loopbacks are controlled by control registers inside the ORT8850 core, which are accessible from the system bus and the MicroProcessor Interface (MPI). In both loopback modes, all channels are placed with a single control. The data paths in the two loopback modes are shown in Figure 8.

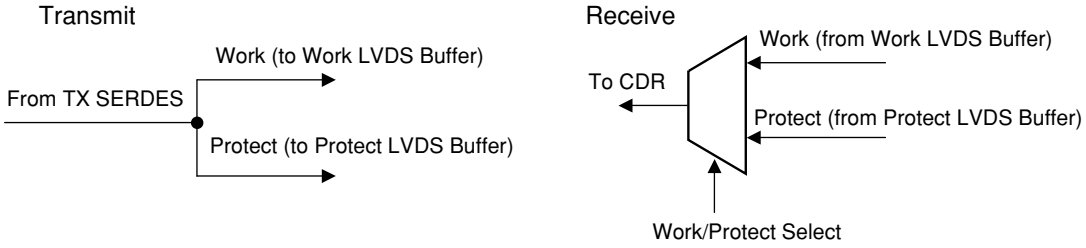
AA. This same scheme is used for channels groupings of AC/AD, BA/BB, and BC/BD. For quad protection when the alignment FIFOs are to be used, the protection switching must be done in FPGA logic.

Figure 9. Parallel Protection Switching



LVDS protection switching (Figure 10) takes place at the LVDS buffer before the serial data is sent into the CDR. The selection is between the main LVDS buffer and the protect LVDS buffer. The main LVDS buffer provide the main receive data on RXDxx_W_[P:N] while the protect LVDS buffers provide protection receive data on RXDxx_P_[P:N]. When operating using the main LVDS buffers (default) no status information is available on the protect LVDS buffers since the serial stream must reach the SONET framer before status information is available on the data stream. The same is also true for the main LVDS buffers when operating with the protect buffers.

Figure 10. LVDS Protection Switching



See Table 17 and Table 18 and the accompanying text for details and register settings for the protection switching options.

FPSC Configuration - Overview

Configuration of the ORT8850 occurs in two stages: FPGA bit stream configuration and embedded core setup.

FPGA Configuration - Overview

Prior to becoming operational, the FPGA goes through a sequence of states, including power-up, initialization, configuration, start-up, and operation. The FPGA logic is configured by the standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet. The options for the embedded core are set via registers that are accessed through the FPGA system bus. The system bus can be driven by an external PPC compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block, that drives the system by using the user interface and uses very little FPGA logic, is available in the *MPI/System Bus* technical note (TN1017). This IP block sets up the embedded core via a state machine and allows the ORT8850 to work in an independent system without an external MicroProcessor Interface.

Embedded Core Setup

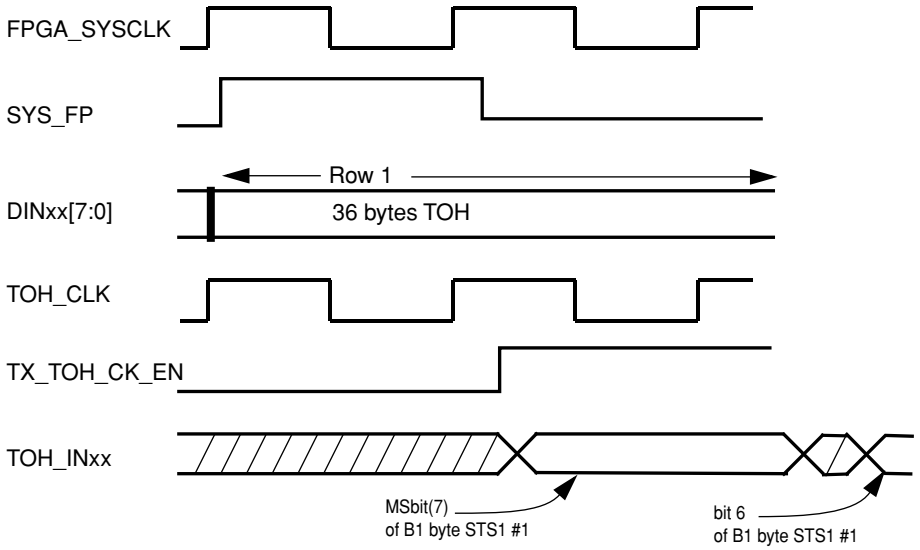
All options for the operation of the core are configured according to the memory map shown in Table 19.

During the power-up sequence, the ORT8850 device (FPGA programmable circuit and the core) is held in reset. All the LVDS output buffers and other output buffers are held in 3-state. All Flip-Flops in the core area are in reset state, with the exception of the boundry-scan shift registers, which can only be reset by boundary-scan reset. After power-up reset, the FPGA can start configuration. During FPGA configuration, the ORT8850 core will be held in

Serial TOH Insertion Mode

In the transmit direction the SPE bytes are always transferred unaltered from the input parallel bus to the serial LVDS output. On the other hand, TOH bytes are received from the serial input port and are inserted in the STS-12 frame before being sent to the LVDS output in the Serial TOH Insertion mode. The FPGA logic must provide framing information to the Core using the TX_TOH_CK_EN Input signal. TOH data is input on a row by row basis, with a one clock cycle frame pulse delineating the start of a row, as shown in Figure 14. As shown in the figure, while the SPE bytes are being transmitted for one row, the FPGA logic must simultaneously supply the Core with the TOH data for the next row. Detailed timing for the TOH serial input is shown later in Figure 31.

Figure 14. TOH Serial Port Input Framing Signals (FPGA to Core)



Incoming serial TOH data is synchronized initially to the free running clock, TOH_CLK. TOH_CLK can operate from a minimum frequency of 25 Mhz. to a maximum frequency of 106 MHz. TOH bytes are transferred in the order shown in Figure 15. Bytes are transferred over the serial links with the MSB first. Data should be transferred over the serial link on a row-by-row basis. With three TOH bytes/per row for each STS-1 stream and a total of 12 STS-1 streams per STS-12 frame, a total of 288 TOH bits must be transferred for each row. The 288 TOH bits per row can be sent back-to-back. In this case, TX_TO_CLK_EN will be high continuously for 288 TOH_CLK cycles.

It is the responsibility of the user to synchronize transfer of the TOH bytes to a pre-determined window of time relative to the STS-12 frame position on the parallel input bus, i.e., the 36 TOH bytes to be inserted in row number n must be transferred to the Core during the time the SPE bytes of row n-1 are being transferred to the Core over the parallel input bus. Within each SPE row, a guard band of four TOH_CLK cycles must be provided on each side of the TOH transfer window. No data may be transferred in these guard bands.

Powerdown Mode

Powerdown mode will be entered when the corresponding channel is disabled. Channels can be independently enabled or disabled under software control.

Parallel data bus output enable and TOH serial data output enable signals are made available to the FPGA logic. The HSI macrocell's corresponding channel is also powered down. The device will power up with all eight channels in powerdown mode.

Protection Switching

There is built-in protection switching between the SERDES channels, in the receive direction of the ORT8850. Protection switching allows pairs of SERDES channels to act as main and protect data links, and to switch between the main and protect links via a control register or FPGA interface port. There are two types of protection switches: parallel and LVDS.

Parallel protection switching takes place just before the FPGA interface ports, and after the alignment FIFO. The alignment FIFO must be used for this type of protection switching. It is possible to bypass the pointer interpreter/mover and still use the parallel protection switching. In this mode, SERDES channels AA and AB are used as main and protect. When selected for main, channel AA is used to provide data on interface ports AA. When selected for protect, channel AB is used to provide data on FPGA interface ports AA. The same scheme is used for channel groupings AC/AD, BA/BB, and BC/BD

There are two ways to control the parallel protection switching, interface signal and software control. On the FPGA interface, there are 4 input signals to the ORT8850 core that will select between a main and a protect channel. When using the interface signal to control protection switching, only the parallel data is switched; the serial TOH data outputs are not switched.

Software control will switch both the parallel data and the serial TOH data outputs to the FPGA. The software control register is found at 0x30009 in the memory map (Table 19).

Table 17. Register Settings, Parallel Protection Switching

FPGA Interface Signal	When '0'	When '1'
PROT_SWITCH_AA	Channel AB data on DOUTAA	Channel AA data on DOUTAA
PROT_SWITCH_AC	Channel AD data on DOUTAC	Channel AC data on DOUTAC
PROT_SWITCH_BA	Channel BB data on DOUTBA	Channel BA data on DOUTBA
PROT_SWITCH_BC	Channel BD data on DOUTBC	Channel BC data on DOUTBC

LVDS protection switching takes place at the LVDS buffer before the serial data is sent into the Data Recovery (CDR). The selection is between the main LVDS buffer and the protect LVDS buffer. The work LVDS buffers are TXDxx_W_[P:N], while the protect LVDS buffers are TXDxx_P_[P:N]. When operating using the LVDS buffers (default), no status information is available on the protect LVDS buffers since the serial stream must reach the SONET framer before status information is available on the data stream. The same is also true for the work LVDS buffers when operating with the protect buffers.

There are two ways to control the LVDS protection switching, interface and software control. On the FPGA interface, there are eight input signals to the ORT8850 core that will select between the work and protect LVDS buffers.

Table 18. LVDS Protection Switching

FPGA Interface Signal	When '0'	When '1'
LVDS_PROT_AA	Channel AA gets TXD_AA_W_[P:N]	Channel AA gets TXD_AA_P_[P:N]
LVDS_PROT_AB	Channel AB gets TXD_AB_W_[P:N]	Channel AB gets TXD_AB_P_[P:N]
LVDS_PROT_AC	Channel AC gets TXD_AC_W_[P:N]	Channel AC gets TXD_AC_P_[P:N]
LVDS_PROT_AD	Channel AD gets TXD_AD_W_[P:N]	Channel AD gets TXD_AD_P_[P:N]

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
3000C	[0:3]	R/W	number of consecutive A1 A2 errors to generate [0:3]	00	If a particular channel's "A1 A2 error insert command" control bit is set to the value 1 then the "A1 and A2 error insert values" will be inserted into that channels respective A1 and A2 bytes. The number of consecutive frames to be corrupted is determined by the "number of consecutive A1 A2 errors to generate [0:3]" control bits. MSB is bit 3
	[4]	R/W	backplane side loopback control	0	0 = No loopback. 1 = RX to TX loopback on backplane side. Serial input is run through SERDES and SONET block, then looped back in parallel to SERDES and out serial.
	[5]	R/W	DINxx/DOUTxx parallel bus parity control	1	0 = Odd parity 1 = Even parity
	[6]	R/W	scrambler/descrambler	1	0 = no RX direction, descramble / TX direction scramble 1 = In RX direction, descramble channel after the SONET frame recovery. In TX direction, scramble data just before parallel-to-serial conversion
	[7]	-	Not Used	0	
3000D	[0:7]	R/W	A1 error insert value [0:7]	00	Value of the A1 byte for error insert
3000E	[0:7]	R/W	A2 error insert value [0:7]	00	Value of the A2 byte for error insert
3000F	[0:7]	R/W	transmit B1 error insert mask [0:7]	00	0 = No error insertion. 1 = Invert corresponding bit in B1 byte.
30010	[0]	R	AA alarm	0	Consolidation alarm for channel AA 1 = alarm 0 = no alarm.
	[1]	R	AB alarm	0	Consolidation alarm for channel AB 1 = alarm 0 = no alarm.
	[2]	R	AC alarm	0	Consolidation alarm for channel AC 1 = alarm 0 = no alarm.
	[3]	R	AD alarm	0	Consolidation alarm for channel AD 1 = alarm 0 = no alarm.
	[4-7]	-	Not Used	0	
30011	[0]	R/W	AA/BA alarm enable/mask register	0	AA and BA enable 1 = enabled 0 = not enabled
	[1]	R/W	AB/BB alarm enable/mask register	0	AB and BB enable 1 = enabled 0 = not enabled
	[2]	R/W	AC/BC alarm enable/mask register	0	AC and BC enable 1 = enabled 0 = not enabled
	[3]	R/W	AD/BD alarm enable/mask register	0	AD and BD enable 1 = enabled 0 = not enabled
	[4-7]	-	Not Used	0	

Table 19. Memory Map Descriptions (Continued)

(0x) Absolute Address	Bit	Type	Name	Reset Value (0x)	Description
30019	[0:7]	-	Not Used	00	
Channel Register Blocks					
30020* 30038 30050 30068 30080 30098 300B0 300C8	[0]	R/W	AIS-L insert in OOF	0	0 = When RX direction OOF occurs, do not insert AIS-L. 1 = When RX direction OOF occurs, insert AIS-L.
	[1]	R/W	AIS-L control	0	0 = Do not force AIS-L insert 1 = Always force AIS-L insert
	[2]	R/W	TOH output parity error insert	0	0 = Do not insert a parity error 1 = Insert parity error in parity bit of receive TOH serial output for as long as this bit is set
	[3]	R/W	RX K1/K2 source select	0	0 = Set receive direction K1 K2 bytes to 0. 1 = Pass receive direction K1 K2 through pointer mover.
	[4]	R/W	DOUTxx bus parity error insert	0	0 = Do not insert parity error. 1 = Insert parity error in DOUTxx_PAR for as long as this bit is set.
	[5]	R/W	channel enable/disable control	0	0 = Power down CDR channels 1 = Functional mode.
	[6]	R/W	DOUTxx_EN	0	DOUTxx_EN signal
	[7]	R/W	TOH_EN	0	TOHxx_EN signal
30021* 30039 30051 30069 30081 30099 300B1 300C9	[0]	R/W	D9 source select	0	0 = Insert D9 from TOH_INxx 1 = Pass through D9 from DINxx
	[1]	R/W	D10 source select	0	0 = Insert D10 from TOH_INxx 1 = Pass through D10 from DINxx
	[2]	R/W	D11 source select	0	0 = Insert D11 from TOH_INxx 1 = Pass through D11 from DINxx
	[3]	R/W	D12 source select	0	0 = Insert D12 from TOH_INxx 1 = Pass through D12 from DINxx
	[4]	R/W	K1 K2 source select	0	0 = Insert K1, K2 from TOH_INxx 1 = Pass through K1, K2 from DINxx
	[5]	R/W	S1 M0 source select	0	0 = Insert S1, M0, from TOH_INxx 1 = Pass through S1 M0 of DINxx
	[6]	R/W	E1 F1 E2 source select		0 = Insert E1, F1, E2 from TOH_INxx on FPGA interface 1 = Pass through E1, F1, E2 TOH bytes of DINxx
	[7]	R/W	TOH source select	0	0 = Insert TOH from TOH_INxx on FPGA interface for transmit 1 = Pass through all TOH DINxx for transmit
30022* 3003A 30052 3006A 30082 3009A 300B2 300CA	[0:7]	R/W	D1~D8 source select	00	0 = Insert TOH for transmit from TOH_INxx from the FPGA interface. 1 = Pass through D1~D8 TOH bytes from DINxx.

Pin Information

This section describes the pins and signals that perform FPGA-related functions. During configuration, the user-programmable I/Os are 3-stated and pulled up with an internal resistor. If any FPGA function pin is not used (or not bonded to package pin), it is also 3-stated and pulled up after configuration.

Table 32. FPGA Common-Function Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD33	—	3.3 V positive power supply. This power supply is used for 3.3 V configuration RAMs and internal PLLs. When using PLLs, this power supply should be well isolated from all other power supplies on the board for proper operation.
VDD15	—	1.5 V positive power supply for internal logic.
VDDIO	—	Positive power supply used by I/O banks.
VSS	—	Ground.
PTEMP	I	Temperature sensing diode pin. Dedicated input.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously SET/RESET.
CCLK	O	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in.
	I	In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.*
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
$\overline{\text{PRGM}}$	I	$\overline{\text{PRGM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
$\overline{\text{RD\_CFG}}$	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
$\overline{\text{CFG\_IRQ}}$/MPI_IRQ	O	During JTAG, slave, master, and asynchronous peripheral configuration assertion on this $\overline{\text{CFG\_IRQ}}$ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output, when the MPI is used.

1. The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Table 32. FPGA Common-Function Pin Descriptions (Continued)

Symbol	I/O	Description
Special-Purpose Pins		
M[3:0]	I	During power-up and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.*
PLL_CK[0:7][TC]	I	Semi-dedicated PLL clock pins. During configuration they are 3-stated with a pull up.
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user-programmable I/O, if not used for clock inputs.
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O in boundary scan is not used.*
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration this pin is a user-programmable I/O pin.*
HDC	O	High during configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{LDC}}$	O	$\overline{\text{Low during configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.*
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
$\overline{\text{WR}}$/MPI_RW	I	$\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{\text{WR}}$/MPI_RW is a user-programmable I/O pin.*
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the *PowerPC* bus master utilizing the least-significant bits of the *PowerPC* 32-bit address.
$\overline{\text{MPI\_BURST}}$	I	$\overline{\text{MPI\_BURST}}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.

1. The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Table 35. ORT8850H Pins That Are Unused in ORT8850L

BGA Ball Bonds	ORT8850H PIOs
K4	PL11A
M5	PL13A
R5	PL20A
T5	PL21A
W4	PL27A
AA2	PL28A
Y4	PL29A
AC4	PL35A
AD5	PL37A
AG1	PL38A
AP4	PB3A
AK10	PB9A
AK11	PB10A
AM9	PB11A
AN9	PB12A
AM14	PB19A
AN14	PB20A
D11	PT12A
E13	PT11A

Users should avoid using these pins if they plan to migrate their ORT8850H design to an ORT8850L.

Package Pinouts

Table 36 provides the package pin and pin function for the ORT8850 FPSC and packages. The bond pad name is identified in the PIO nomenclature used in the *ispLEVER* design editor. The Bank column provides information as to which output voltage level bank the given pin is in. The Group column provides information as to the group of pins the given pin is in. This is used to show which VREF pin is used to provide the reference voltage for single-ended limited-swing I/Os. If none of these buffer types (such as SSTL, GTL, HSTL) are used in a given group, then the VREF pin is available as an I/O pin.

When the number of FPGA bond pads exceeds the number of package pins, bond pads are unused. When the number of package pins exceeds the number of bond pads, package pins are left unconnected (no connects). When a package pin is to be left as a no connect for a specific die, it is indicated as a note in the device column for the FPGA. The tables provide no information on unused pads.

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
AJ3	6 (BL)	4	IO	PL26A	PL46A	—	—
AK2	6 (BL)	4	IO	PL27D	PL47D	PLL_CK7C/HPPLL	L9C_D0
AL1	6 (BL)	4	IO	PL27C	PL47C	PLL_CK7T/HPPLL	L9T_D0
AB20	—	—	VSS	VSS	VSS	—	—
AJ5	6 (BL)	4	IO	PL27B	PL47B	—	L10C_A0
AJ4	6 (BL)	4	IO	PL27A	PL47A	—	L10T_A0
AB21	—	—	VSS	VSS	VSS	—	—
AK3	—	—	I	PTEMP	PTEMP	PTEMP	—
AM1	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AL2	—	—	IO	LVDS_R	LVDS_R	LVDS_R	—
AK4	—	—	VDD33	VDD33	VDD33	—	—
AB22	—	—	VSS	VSS	VSS	—	—
AK6	—	—	VDD33	VDD33	VDD33	—	—
AL5	6 (BL)	5	IO	PB2A	PB2A	DP2	L11T_D1
AN4	6 (BL)	5	IO	PB2B	PB2B	—	L11C_D1
AM2	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AM5	6 (BL)	5	IO	PB2C	PB2C	PLL_CK6T/PPLL	L12T_D1
AK7	6 (BL)	5	IO	PB2D	PB2D	PLL_CK6C/PPLL	L12C_D1
AL6	6 (BL)	5	IO	PB3A	PB3C	—	L13T_D1
AN5	6 (BL)	5	IO	PB3B	PB3D	—	L13C_D1
AM4	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AM6	6 (BL)	5	IO	PB3C	PB4C	VREF_6_05	L14T_D0
AL7	6 (BL)	5	IO	PB3D	PB4D	DP3	L14C_D0
AK8	6 (BL)	6	IO	PB4A	PB5C	—	L15T_D3
AP5	6 (BL)	6	IO	PB4B	PB5D	—	L15C_D3
AB32	—	—	VSS	VSS	VSS	—	—
AK9	6 (BL)	6	IO	PB4C	PB6C	VREF_6_06	L16T_D2
AN6	6 (BL)	6	IO	PB4D	PB6D	D14	L16C_D2
AM7	6 (BL)	6	IO	PB5A	PB7C	—	L17T_D1
AP6	6 (BL)	6	IO	PB5B	PB7D	—	L17C_D1
AN3	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AL8	6 (BL)	7	IO	PB5C	PB8C	D15	L18T_D1
AN7	6 (BL)	7	IO	PB5D	PB8D	D16	L18C_D1
AM8	6 (BL)	7	IO	PB6A	PB9C	D17	L19T_D0
AL9	6 (BL)	7	IO	PB6B	PB9D	D18	L19C_D0
AL4	—	—	VSS	VSS	VSS	—	—
AP7	6 (BL)	7	IO	PB6C	PB10C	VREF_6_07	L20T_D0
AN8	6 (BL)	7	IO	PB6D	PB10D	D19	L20C_D0
AL10	6 (BL)	8	IO	PB7A	PB11C	D20	L21T_D2
AP8	6 (BL)	8	IO	PB7B	PB11D	D21	L21C_D2
AL11	6 (BL)	8	IO	PB7C	PB12C	VREF_6_08	L22T_D0
AM10	6 (BL)	8	IO	PB7D	PB12D	D22	L22C_D0

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
AL19	5 (BC)	2	IO	PB17D	PB25D	—	L7C_A0
AP20	5 (BC)	3	IO	PB18A	PB26C	—	L8T_D3
AK19	5 (BC)	3	IO	PB18B	PB26D	VREF_5_03	L8C_D3
AM15	5 (BC)	—	VDDIO5	VDDIO5	VDDIO5	—	—
AN20	5 (BC)	3	IO	PB18C	PB27A	—	—
Y21	—	—	VSS	VSS	VSS	—	—
AP21	5 (BC)	3	IO	PB19A	PB27C	—	L9T_D2
AL20	5 (BC)	3	IO	PB19B	PB27D	—	L9C_D2
Y22	—	—	VSS	VSS	VSS	—	—
AK20	5 (BC)	3	IO	PB19C	PB28A	—	—
AN21	5 (BC)	3	IO	PB20A	PB28C	PBCK1T	L10T_A0
AM21	5 (BC)	3	IO	PB20B	PB28D	PBCK1C	L10C_A0
AM20	5 (BC)	—	VDDIO5	VDDIO5	VDDIO5	—	—
AK21	5 (BC)	3	IO	PB20C	PB29A	—	—
AP22	5 (BC)	4	IO	PB21A	PB29C	—	L11T_D2
AL21	5 (BC)	4	IO	PB21B	PB29D	—	L11C_D2
AA15	—	—	VSS	VSS	VSS	—	—
AN22	5 (BC)	4	IO	PB21C	PB30A	—	—
AP23	5 (BC)	4	IO	PB22A	PB30C	—	L12T_A0
AN23	5 (BC)	4	IO	PB22B	PB30D	VREF_5_04	L12C_A0
AA13	—	—	VSS	VSS	VSS	—	—
AK22	5 (BC)	4	IO	PB22C	PB31C	—	L13T_A0
AL22	5 (BC)	4	IO	PB22D	PB31D	—	L13C_A0
AN24	5 (BC)	5	IO	PB23C	PB32C	—	L14T_D2
AK23	5 (BC)	5	IO	PB23D	PB32D	VREF_5_05	L14C_D2
AA14	—	—	VSS	VSS	VSS	—	—
AL23	5 (BC)	5	IO	PB24C	PB33C	—	L15T_D0
AM24	5 (BC)	5	IO	PB24D	PB33D	—	L15C_D0
AP25	5 (BC)	5	IO	PB25A	PB34C	—	L16T_A0
AN25	5 (BC)	5	IO	PB25B	PB34D	—	L16T_A0
AP26	5 (BC)	6	IO	PB25C	PB35A	—	—
AK25	5 (BC)	6	IO	PB26A	PB35C	—	L17T_A0
AN26	5 (BC)	6	IO	PB26B	PB35D	VREF_5_06	L17C_A0
AP27	5 (BC)	6	IO	PB26C	PB36A	—	—
AM25	5 (BC)	6	IO	PB27A	PB36C	—	L18T_D3
AK26	5 (BC)	6	IO	PB27B	PB36D	—	L18C_D3
N32	—	—	VSS	VSS	VSS	—	—
AL24	—	—	O	TXDAA_P_N	TXDAA_P_N	—	L1N_A0
AK24	—	—	O	TXDAA_P_P	TXDAA_P_P	—	L1P_A0
A32	—	—	VDD33	VDD33	VDD33	—	—
AN27	—	—	O	TXDAB_P_N	TXDAB_P_N	—	L2N_D0
AP28	—	—	O	TXDAB_P_P	TXDAB_P_P	—	L2P_D0

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
A29	—	—	O	Reserved	Reserved	—	L56P_D0
D27	—	—	O	Reserved	Reserved	—	L57N_D0
E26	—	—	O	Reserved	Reserved	—	L57P_D0
C27	—	—	O	Reserved	Reserved	—	L58N_D0
D26	—	—	O	Reserved	Reserved	—	L58P_D0
A28	—	—	O	Reserved	Reserved	—	L59N_D0
B27	—	—	O	Reserved	Reserved	—	L59P_D0
C26	—	—	O	Reserved	Reserved	—	L60N_D0
D25	—	—	O	Reserved	Reserved	—	L60P_D0
A27	—	—	O	Reserved	Reserved	—	L61N_D0
B26	—	—	O	Reserved	Reserved	—	L61P_D0
D24	—	—	O	Reserved	Reserved	—	L62N_D0
C25	—	—	O	Reserved	Reserved	—	L62P_D0
C22	—	—	VSS	VSS	VSS	—	—
A26	1 (TC)	1	IO	PT26D	PT35D	—	L1C_D3
E25	1 (TC)	1	IO	PT26C	PT35C	—	L1T_D3
A25	1 (TC)	1	IO	PT26B	PT35B	—	L2C_A0
B25	1 (TC)	1	IO	PT26A	PT35A	—	L2T_A0
C24	1 (TC)	1	IO	PT25D	PT34D	VREF_1_01	L3C_D0
D23	1 (TC)	1	IO	PT25C	PT34C	—	L3T_D0
C32	—	—	VSS	VSS	VSS	—	—
B24	1 (TC)	1	IO	PT25B	PT33D	—	L4C_A2
E24	1 (TC)	1	IO	PT25A	PT33C	—	L4T_A2
D22	1 (TC)	2	IO	PT24D	PT32D	—	L5C_D1
B23	1 (TC)	2	IO	PT24C	PT32C	VREF_1_02	L5T_D1
E23	1 (TC)	2	IO	PT24B	PT31D	—	L6C_A3
A23	1 (TC)	2	IO	PT24A	PT31C	—	L6T_A3
D21	1 (TC)	2	IO	PT23D	PT30D	—	L7C_D1
B22	1 (TC)	2	IO	PT23C	PT30C	—	L7T_D1
D4	—	—	VSS	VSS	VSS	—	—
A22	1 (TC)	3	IO	PT22D	PT29D	—	L8C_D1
C21	1 (TC)	3	IO	PT22C	PT29C	VREF_1_03	L8T_D1
E22	1 (TC)	3	IO	PT22A	PT29A	—	—
D20	1 (TC)	3	IO	PT21D	PT28D	—	L9C_D1
B21	1 (TC)	3	IO	PT21C	PT28C	—	L9T_D1
D31	—	—	VSS	VSS	VSS	—	—
E21	1 (TC)	3	IO	PT21A	PT28A	—	—
A21	1 (TC)	3	IO	PT20D	PT27D	—	L10C_D0
B20	1 (TC)	3	IO	PT20C	PT27C	—	L10T_D0
A11	1 (TC)	—	VDDIO1	VDDIO1	VDDIO1	—	—
A20	1 (TC)	3	IO	PT20A	PT27A	—	—
E20	1 (TC)	4	IO	PT19D	PT26D	—	L11C_D0

Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
D19	1 (TC)	4	IO	PT19C	PT26C	—	L11T_D0
C19	1 (TC)	4	IO	PT19B	PT25D	—	L12C_A0
B19	1 (TC)	4	IO	PT19A	PT25C	—	L12T_A0
N3	—	—	VSS	VSS	VSS	—	—
E19	1 (TC)	4	IO	PT18D	PT24D	—	L13C_D0
D18	1 (TC)	4	IO	PT18C	PT24C	VREF_1_04	L13T_D0
A17	1 (TC)	—	VDDIO1	VDDIO1	VDDIO1	—	—
B18	1 (TC)	4	IO	PT18B	PT24B	—	L14C_A0
C18	1 (TC)	4	IO	PT18A	PT24A	—	L14T_A0
B17	1 (TC)	5	IO	PT17D	PT23D	PTCK1C	L15C_A0
C17	1 (TC)	5	IO	PT17C	PT23C	PTCK1T	L15T_A0
N13	—	—	VSS	VSS	VSS	—	—
A16	1 (TC)	5	IO	PT17B	PT23B	—	L16C_D2
D17	1 (TC)	5	IO	PT17A	PT23A	—	L16T_D2
B16	1 (TC)	5	IO	PT16D	PT22D	PTCK0C	L17C_A0
C16	1 (TC)	5	IO	PT16C	PT22C	PTCK0T	L17T_A0
D16	1 (TC)	5	IO	PT16A	PT22A	—	—
E18	1 (TC)	5	IO	PT15D	PT21D	VREF_1_05	L18C_D3
A15	1 (TC)	5	IO	PT15C	PT21C	—	L18T_D3
A19	1 (TC)	—	VDDIO1	VDDIO1	VDDIO1	—	—
B15	1 (TC)	5	IO	PT15A	PT21A	—	—
D15	1 (TC)	6	IO	PT14D	PT20D	—	L19C_D2
A14	1 (TC)	6	IO	PT14C	PT20C	—	L19T_D2
N14	—	—	VSS	VSS	VSS	—	—
B14	1 (TC)	6	IO	PT14A	PT20A	—	—
E17	1 (TC)	6	IO	PT13D	PT19D	—	L20C_D2
C14	1 (TC)	6	IO	PT13C	PT19C	VREF_1_06	L20T_D2
D14	1 (TC)	6	IO	PT13A	PT19A	—	—
N15	—	—	VSS	VSS	VSS	—	—
E16	0 (TL)	1	IO	PT11D	PT18D	MPI_RTRY_N	L1C_D3
A13	0 (TL)	1	IO	PT11C	PT18C	MPI_ACK_N	L1T_D3
B13	0 (TL)	1	IO	PT11B	PT17D	—	L2C_D0
A12	0 (TL)	1	IO	PT11A	PT17C	VREF_0_01	L2T_D0
B12	0 (TL)	1	IO	PT10D	PT16D	M0	L3C_D1
D13	0 (TL)	1	IO	PT10C	PT16C	M1	L3T_D1
A34	—	—	VSS	VSS	VSS	—	—
E15	0 (TL)	2	IO	PT10B	PT15D	MPI_CLK	L4C_D3
B11	0 (TL)	2	IO	PT10A	PT15C	A21/MPI_BURST_N	L4T_D3
A10	0 (TL)	2	IO	PT9D	PT14D	M2	L5C_D3
E14	0 (TL)	2	IO	PT9C	PT14C	M3	L5T_D3
A3	0 (TL)	—	VDDIO0	VDDIO0	VDDIO0	—	—
D12	0 (TL)	2	IO	PT9B	PT13D	VREF_0_02	L6C_D0

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 39 lists eight parasitics associated with the *ORCA* packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

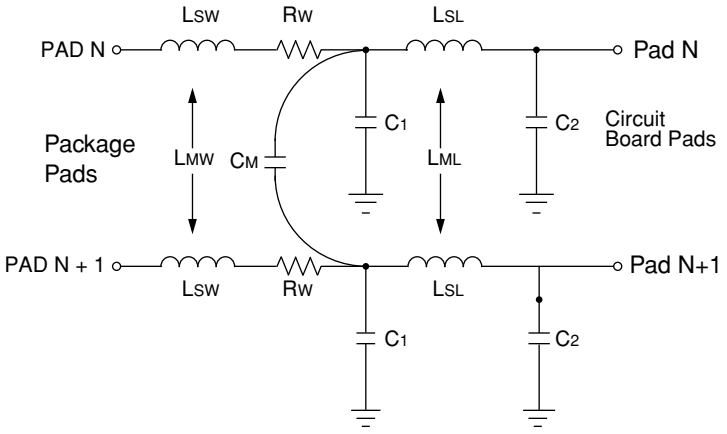
Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 39 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.

Table 39. ORCA ORT8850 Package Parasitics

Package Type	L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
680-Pin PBGAM	3.8	1.3	250	1.0	1.0	0.3	2.8 - 5.0	0.5 - 1.0

Figure 39. Package Parasitics



Package Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP): When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.

Table 44. Lead-Free Packaging – Commercial Ordering Information[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT8850L	ORT8850L-3BMN680C	3	Lead-Free PBGAM (fpBGA)	680	C
	ORT8850L-2BMN680C	2	Lead-Free PBGAM (fpBGA)	680	C
	ORT8850L-1BMN680C	1	Lead-Free PBGAM (fpBGA)	680	C
ORT8850H	ORT8850H-2BMN680C	2	Lead-Free PBGAM (fpBGA)	680	C
	ORT8850H-1BMN680C	1	Lead-Free PBGAM (fpBGA)	680	C

Table 45. Lead-Free Packaging – Industrial Ordering Information[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORT8850L	ORT8850L-2BMN680I	2	Lead-Free PBGAM (fpBGA)	680	I
	ORT8850L-1BMN680I	1	Lead-Free PBGAM (fpBGA)	680	I
ORT8850H	ORT8850H-1BMN680I	1	Lead-Free PBGAM (fpBGA)	680	I

1.For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.

Revision History

Date	Version	Change Summary
–	8	Previous Lattice releases.
January 2004	8.1	Added lead-free package designator.
August 2004	9	Added lead-free package ordering part numbers (OPNs).
October 2005	10	Added clarification to the STM Pointer Mover bypass. Added clarification to the signal description for LINE_FP.
April 2006	11	Added clarification to the B1, section bit interleavered parity (BIP-8) byte. Added clarification to B1 processing.
February 2008	11.1	Corrected name of Register 30009, Bits 5 & 6 in Memory Map Description table.