# E·XFLattice Semiconductor Corporation - <u>ORT8850L-3BM680C Datasheet</u>



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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	·
Number of Logic Elements/Cells	4992
Total RAM Bits	75776
Number of I/O	278
Number of Gates	397000
Voltage - Supply	1.425V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	680-BBGA
Supplier Device Package	680-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ort8850l-3bm680c

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# **FPGA Logic Overview**

The ORCA Series 4 architecture is a new generation of SRAM-based programmable devices from Lattice. It includes enhancements and innovations geared toward today's high-speed systems on a single chip. Designed with networking applications in mind, the Series 4 family incorporates system-level features that can further reduce logic requirements and increase system speed. ORCA Series 4 devices contain many new patented enhancements and are offered in a variety of packages and speed grades.

The hierarchical architecture of the logic, clocks, routing, RAM, and system-level blocks create a seamless merge of FPGA and ASIC designs. Modular hardware and software technologies enable System-on-a-Chip integration with true plug-and-play design implementation.

The architecture consists of four basic elements: Programmable Logic Cells (PLCs), Programmable I/O cells (PIOs), Embedded Block RAMs (EBRs) and system-level features. These elements are interconnected with a rich routing fabric of both global and local wires. An array of PLCs are surrounded by common interface blocks which provide an abundant interface to the adjacent PLCs or system blocks. Routing congestion around these critical blocks is eliminated by the use of the same routing fabric implemented within the programmable logic core. Each PLC contains a PFU, SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PIOs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, uplink and downlink functions, and other functions on two output signals. Large blocks of 512 x 18 quad-port RAM complement the existing distributed PFU memory. The RAM blocks can be used to implement RAM, ROM, FIFO, multiplier, and CAM. Some of the other system-level functions include the MicroProcessor Interface (MPI), Phase-Locked Loops (PLLs), and the Embedded System Bus (ESB).

#### PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/flip-flops, and one additional Flip-Flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion; two sets of four LUTs and flip-flops that can be controlled independently. Each PFU has two independent programmable clocks, clock enables, local SET/RESET, and data selects. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth flip-flop for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The flip-flops (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The flip-flops also have programmable clock polarity, clock enables, and local SET/RESET.

The SLIC is connected from PLC routing resources and from the outputs of the PFU. It contains eight 3-state, bidirectional buffers, and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections from the PFU outputs make fast, true, 3-state buses possible within the FPGA, reducing required routing and allowing for realworld system performance.

## Programmable I/O

The Series 4 PIO addresses the demand for the flexibility to select I/Os that meet system interface requirements. I/Os can be programmed in the same manner as in previous *ORCA* devices, with the additional new features which allow the user the flexibility to select new I/O types that support High-Speed Interfaces.

Each PIO contains four Programmable I/O pads and is interfaced through a common interface block to the FPGA array. The PIO is split into two pairs of I/O pads with each pair having independent clock enables, local SET/RESET, and global SET/RESET. On the input side, each PIO contains a programmable latch/Flip-Flop which enables very fast latching of data from any pad. The combination provides very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer with a PFU. On the output side of each PIO, an output from the PLC array can be routed to each output flip-flop, and logic can be associated

# **ORT8850 Overview**

The ORT8850 FPSCs provide high-speed backplane transceivers combined with FPGA logic. There are two devices in the ORT8850 family. The ORT8850L device is based on 1.5 V OR4E02 ORCA FPGA and has a 26 x 24 array of Programmable Logic Cells (PLCs). The ORT8850H device is based on 1.5V OR4E06 ORCA FPGA and has a 46 x 44 array. The embedded core which contains the backplane transceivers is attached to the right side of the device and is integrated directly into the FPGA array. A top level diagram of the basic chip configuration is shown in Figure 1.





# **Embedded Core Overview**

The ORT8850 embedded core contains a pseudo-SONET block for backplane or intra-board, chip-to-chip communication. The SONET block includes a High-Speed Interface (HSI) macrocell and a Synchronous Transport Module (STM) macrocell. It supports eight full-duplex channels and performs data transfer, scrambling/descrambling and SONET framing at the maximum rate of 850 Mbits/s. Figure 2 shows a top level diagram of the ORT8850 and the basic data flows through the device. this feature the alignment FIFO cannot be used with this clock architecture. The recovered clock is used for all receive timing in the embedded core and supplied to the FPGA logic which must provide the clock domain transfer functionality.





# SONET Bypass Mode

It is possible to utilize only the serializer and deserializer (SERDES) blocks in the ORT8850 and to bypass all of the SONET framing and scrambling/descrambling. In this mode the parallel data from the FPGA is serialized and sent out the LVDS pins. The serial data in the receive direction will be run through the SERDES and then received as parallel data with a recovered clock into the FPGA.

In the SONET Bypass mode there exists half and quarter rate selection options. Half rate allows the SERDES to operate at 4x the reference clock. When using half rate mode only the bits 7:4 of the parallel FPGA bus are utilized. Quarter rate allows the SERDES to operate at 2x the reference clock. When using quarter rate mode only bits 7:6 of the parallel FPGA bus are utilized. Half rate and quarter rate are selectable per channel and can be mixed per channel so that some channels can run in full rate mode while others operate in half rate mode and still others operate in quarter rate mode.

As shown in Table 3, 63.00 MHz is the slowest reference clock and 106.25 MHz is the fastest reference clock frequency supported. For all three modes, all bandwidths within the reference clock limits are supported. Note that there are gaps between the bandwidths supported in the three modes.

 Table 3. SONET Bypass Mode Bandwidth Options

Reference Clock	Full Mode	Half Mode Bits [7:4] Used	Quarter Mode Bits [7:6] Used
63	504.00 Mbits/s	252.00 Mbits/s	126.00 Mbits/s
77.76	622.08Mbits/s	311.04Mbits/s	155.52Mbits/s
106.25	850.00 Mbits/s	425.00 Mbits/s	212.50 Mbits/s

In the SONET Bypass mode a 1's density function similar to SONET scrambling must be implemented in the FPGA logic to assure reliable clock recovery at the receiver.

# STM Macrocells - Overview

The Synchronous Transport Module (STM) portion of the embedded core consists of two quads, STM A and B. The STM macrocells provide transmitter and receiver logic blocks on a per SERDES basis channel and are located in the data path between the FPGA interface and the HSI macrocell. The STM macrocells' main functions are framing and aligning data into standard STS-N frames as well as providing a 1's density through scrambling/descrambling.

# Figure 7. STM Macrocell Partitioning



## **Transmit STM Macrocell Logic - Overview**

In the transmit direction (FPGA interface to the backplane), each STM macrocell will receive frame aligned streams of STS-12 data (maximum of four streams) from the FPGA logic. The transmitter receive data interface is in a parallel 8-bit format. A common frame pulse for all 8 channels is provided as an input from the FPGA logic to the transmit SONET block.

On each frame pulse the A1/A2 frame alignment bytes are inserted into the data stream and will overwrite any data in this location of the frame. TOH data can be optionally inserted into the transmitted SONET frame. The SONET frame is then optionally scrambled and sent to the HSI macrocell.

TOH data can be inserted into the transmit data stream in two ways; transparently or by inserting serial TOH data from a TOH serial interface signal in the FPGA logic. In the transparent mode, the SPE and TOH data received on parallel input bus is transferred, unaltered, to the serial LVDS output. However, B1 byte of STS-1 is always replaced with a new calculated value (the 11 bytes following B1 are replaced with all zeros). Likewise, in serial and transport mode A1 and A2 bytes of all STS-1s are always regenerated. In the TOH serial insertion mode the SPE bytes are transferred unaltered from the input parallel bus to the serial LVDS output. TOH bytes, however, are received from the FPGA logic through the serial input port and are inserted in the STS- 12 frame before being sent to the LVDS

data. When valid SPE data is carried in this H3 slot, SPE is high in this particular TOH time slot also. In the SPE region, if there is no valid data during any SPE column, the SPE signal will be set to low.

After the pointer interpreter comes the pointer mover block. There is a separate pointer mover for each of the two SONET quads, A and B, each of which handles up to one STS-48 (four channels) The K1/K2 bytes and H1-SS bits are also passed through to the pointer generator so that the FPGA can receive them. The pointer mover handles both concatenations inside the STS-12, and to other STS-12s inside the core. The pointer mover block can correctly process any length of concatenation of STS frames (multiple of three) as long as it begins on an STS-3 boundary (i.e., STS-1 number one, four, seven, ten, etc.) and is contained within the smaller of STS-3, 12, or 48.

The pointer generator block then maps the corresponding bytes into their appropriate location in the outgoing byte stream. The generator also creates offset pointers based on the location of the J1 byte as indicated by the pointer interpreter.

# HSI Macrocell - Overview

The HSI macrocell consists of three functionally independent blocks: receiver, transmitter, and PLL synthesizer. The HSI logic is used for Clock/Data Recovery (CDR) and to serialize and deserialize between the 106.25 MHz byte-wide internal data buses and the 850 Mbits/s serial LVDS links. For a 622 Mbits/s SONET stream, the HSI will perform Clock and Data Recovery (CDR) and MUX/DEMUX between 77.76 MHz byte-wide internal data buses and 622 Mbits/s serial LVDS links. The transmitter block receives parallel data at its input. The MUX (serializer) module performs a parallel-to-serial conversion using a clock provided by the PLL/synthesizer block. The resulting serial data stream is then transmitted through the LVDS driver.

The receiver block receives a LVDS serial data without clock at its input. Based on data transitions, the receiver selects an appropriate clock phase for each channel to retime the data. The retimed data and clock are then passed to the DEMUX (deserializer) module. The DEMUX module performs serial-to-parallel conversion and provides parallel data and clock to the SONET framer block.

# Supervisory and Test Support Features - Overview

The supervisory and test support functions provided by the ORT8850 include data integrity monitoring, error insertion capabilities and loopback support. These functions are described in the following sections.

#### Integrity Monitoring

FPGA Parallel Bus Integrity: Parity error checking is implemented on each of the four parallel input buses on each STM quad (A & B). "Even" or "Odd" parity can be selected by setting a control register bit. Upon detection of an error, an alarm bit is set. This feature is on a per channel basis. Note that, on parallel output ports, parity is calculated over the 8-bit data bus and not on the SPE and C1J1 lines.

TOH Serial Port Integrity: There is "even" parity generation on each of the four TOH serial output ports. There is "even" parity error checking on each of the four TOH serial input ports. There is one parity bit embedded in the TOH frame. It occupies the Most Significant Bit location of A1 byte of STS#1. Upon detection of an error, an alarm bit is set. This feature is on a per channel basis.LVDS Link Integrity: There is B1 parity generation on each of the four LVDS output channels. There is also performance monitoring on each of the four LVDS input channels, implemented as B1 parity error checking. Upon detection of an error, a counter is incremented (one count per errored bit) and an alarm bit is set. The counter is 7-bits wide plus 1 overflow indicator bit. This feature is on a per channel basis.

Framer Monitor: The framer in the receive direction will report Loss of Frame by setting an alarm bit, as well as a LOF count and errored frame count. The LOF alarm bit is not clearable as long as the channel is in the LOF state. In addition, the errored frame count represents errored frames, and will not increment more than once per frame even if there are multiple errors.

Receiver Internal Path Integrity: There is "even" parity generation in the Receiver section (after descrambler). There is also "even" parity error checking in the Receiver section (before output). Upon detection of an error, an alarm bit is set. This feature is on a per channel basis.

STS-12 A>	12	9	6	3	11	8	5	2	10	7	4	1
STS-12 B>	24	21	18	15	23	20	17	14	22	19	16	13
STS-12 C>	36	33	30	27	35	32	29	26	34	31	28	25
STS-12 D>	48	45	42	39	47	44	41	38	46	43	40	37

All internal framing is based on the system frame pulse (SYS\_FP) which is a one-cycle pulse at an 8kHz rate. There is one system frame pulse for all 8 channels or both quads. When the framer receives the system frame pulse the individual overhead bytes are identified.

#### **HSI Macrocell**

The ORT8850 High-Speed Interface (HSI) provides a physical medium for high-speed asynchronous serial data transfer between ASIC devices. The devices can be mounted on the same PC board or mounted on different boards and connected through the shelf back-plane. The ORT8850 CDR macro is an eight-channel Clock-Phase Select (CPS) and data retime function with serial-to-parallel demultiplexing for the incoming data stream and parallel-to-serial multiplexing for outgoing data. The ORT8850 uses an eight-channel HSI macro cell. The HSI macro consists of three functionally independent blocks: receiver, transmitter, and PLL synthesizer.

The PLL synthesizer block generates the necessary 850 MHz clock for operation from a 106.25 MHz, reference. The PLL synthesizer block is a common asset shared by all eight receive and transmit channels. The PLL reference clock must match the interface frequency.

The HSI\_RX block receives differential 850 Mbits/s serial data without clock at its LVDS receiver input. Based on data transitions, the receiver selects an appropriate 850 MHz clock phase for each channel to retime the data. The retimed data and clock are then passed to the deMUX (deserializer) module. DeMUX module performs serial-to-parallel conversion and provides the 106 Mbits/s data and clock.

The HSI\_TX block receives 106 Mbits/s parallel data at its input. MUX (serializer) module performs a parallel-toserial conversion using an 850 MHz clock provided by the PLL/synthesizer block. The resulting 850 Mbits/s serial data stream is then transmitted through the LVDS driver.

The loopback feature built into the HSI macro provides looping of the transmitter data output into the receiver input when desired.

All rate examples described here are the maximum rates possible. The actual HSI internal clock rate is determined by the provided reference clock rate. For example, if a 77.76 MHz reference clock is provided, the HSI macro will operate at 622 Mbits/s.

#### Transmit Path Logic

In the transmit direction each STM quad will receive frame aligned streams of STS-12 data (maximum of four streams per quad) from the FPGA logic. The transmitter receives data interface in a parallel 8-bit format. A common frame pulse for all 8 channels is provided as an input from the FPGA logic to the transmit SONET block.

The system frame pulse is a single pulse at the reference clock rate every 9720 clock cycles. For a 77.76 MHz reference clock this creates an 8KHz pulse rate. The system frame pulse (SYS\_FP) is used to generate the A1/A2 in the transmit direction. It is also used by the Pointer Mover Block to perform the line side loopback, which otherwise uses the LINE\_FP frame pulse also provided by the user from the FPGA to the Embeddded ASIC Block. The Function of the LINE\_FP is mentioned in the Pointer Mover bypass description.

The system frame pulse is common to all channels in the transmit direction. Once it is received from the FPGA logic, the data to be transmitted goes through the following processing steps:

- A parity check is performed on the data
- The Transport Overhead (TOH) data is modified (optional)



#### Figure 16. Basic Logic Blocks, Receive Path, Single Channel

## HSI Functions (Clock Recovery and Deserializer)

The HSI receive path functions include Clock and Data Recovery (CDR) and deserialization of the incoming data from the selected work or protect input stream to the byte-wide internal data bus format. The serial data received from the LVDS buffer does not have an accompanying clock. Based on data transitions, the receiver selects an appropriate internal clock phase for each channel to retime the data. The retimed data and clock are then passed to the DEMUX (deserializer) module. The DEMUX module performs serial-to-parallel conversion and provides parallel data and clock to the SONET framer block. For a 622 Mbits/s SONET stream, the HSI will perform Clock and Data Recovery (CDR) and MUX/DEMUX between 77.76 MHz byte-wide internal data buses and 622 Mbits/s serial LVDS links.

## Sampler

This block operates on the byte-wide data directly from the HSI macro. The HSI external interface always runs at 622 Mbits/s (STS-12), or 850 Mbits/s, but it can be connected directly to a 155 Mbits/s STS-3 stream. If connected to a 155 Mbits/s stream, each incoming bit is received four times. This block is used to return the byte stream to the expected STS-12 format. The mode of operation is controlled by a register and can either be STS-12 (pass-through) or STS-3. The output from this block is not bit aligned (i.e., an 8-bit sample does not necessarily contain an entire SONET byte), but it is in standard SONET STS-12 format (i.e., four STS-3s) and is suitable for framing.

#### SONET Framer Block

The framer block takes byte-wide data from the HSI, and outputs a byte-aligned, byte-wide data stream and 8 kHz sync pulse. The framer algorithm determines the out-of-frame/in-frame status of the incoming data and will set alarm register bits on both an errored frame and an Out-Of-Frame (OOF) state.

The framer block takes byte wide data from the HSI, and outputs a byte aligned byte wide stream and 8 kHz sync pulse asserted coincident the first A1 byte which will be used by following blocks. (Note however that if the pointer

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Figure 29 shows the timing for sending data from the FPGA logic to the Core. In the input case, the constraints on the data are specified in terms of setup and hold times on the data at the interface relative to the clock at the interface. For correct operation these constraints must be met. In the case shown, launch and capture occur on the same (rising) clock edge. Data is captured before the next data is launched, so there will be no hold margin problem. Launched data also has nearly a full clock period to become stable at the capture latch, so setup margin should not be a problem.

# Figure 29. Full Cycle, Align and Bypass Mode Input Configuration and Timing (-1 Speed Grade)



#### a.) Configuration

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The next two examples show timing for serial TOH data input and output. For these cases, the clock is generated in the FPGA logic and the discussion accounts for the skew between the clock signal at the FPGA latch and at the FPGA/Core interface. The clock is routed over a secondary clock path and the skew can vary by  $\pm$  3 ns. A value of + 2 ns was assumed in the discussions.

Figure 30 shows the timing for sending serial TOH data from the Core to the FPGA logic with data being launched and latched on the same (rising) clock edge. As in the previous examples, setup and hold time constraints for the data versus the reference clock at the capturing latch must be met. Data is not captured before the next data is launched, so there might be a hold time margin problem. Launched data has nearly a full clock period to become stable at the capture latch and the maximum propagation delay is only 0.2 ns so setup margin should not be a problem for the timing relationships assumed. Actual timing analysis should be performed for each application because of the wide range of possible skew values.

#### Figure 30. Full Cycle, TOH Output Configuration and Timing (-1 Speed Grade)



a. Configuration

# Powerdown Mode

Powerdown mode will be entered when the corresponding channel is disabled. Channels can be independently enabled or disabled under software control.

Parallel data bus output enable and TOH serial data output enable signals are made available to the FPGA logic. The HSI macrocell's corresponding channel is also powered down. The device will power up with all eight channels in powerdown mode.

# **Protection Switching**

There is built-in protection switching between the SERDES channels, in the receive direction of the ORT8850. Protection switching allows pairs of SERDES channels to act as main and protect data links, and to switch between the main and protect links via a control register or FPGA interface port. There are two types of protection switches: parallel and LVDS.

Parallel protection switching takes place just before the FPGA interface ports, and after the alignment FIFO. The alignment FIFO must be used for this type of protection switching. It is possible to bypass the pointer interpreter/mover and still use the parallel protection switching. In this mode, SERDES channels AA and AB are used as main and protect. When selected for main, channel AA is used to provide data on interface ports AA. When selected for protect, channel AB is used to provide data on FPGA interface ports AA. The same scheme is used for channel groupings AC/AD, BA/BB, and BC/BD

There are two ways to control the parallel protection switching, interface signal and software control. On the FPGA interface, there are 4 input signals to the ORT8850 core that will select between a main and a protect channel. When using the interface signal to control protection switching, only the parallel data is switched; the serial TOH data outputs are not switched.

Software control will switch both the parallel data and the serial TOH data outputs to the FPGA. The software control register is found at 0x30009 in the memory map (Table 19).

FPGA Interface Signal	When '0'	When '1'
PROT_SWITCH_AA	Channel AB data on DOUTAA	Channel AA data on DOUTAA
PROT_SWITCH_AC	Channel AD data on DOUTAC	Channel AC data on DOUTAC
PROT_SWITCH_BA	Channel BB data on DOUTBA	Channel BA data on DOUTBA
PROT_SWITCH_BC	Channel BD data on DOUTBC	Channel BC data on DOUTBC

#### Table 17. Register Settings, Parallel Protection Switching

LVDS protection switching takes place at the LVDS buffer before the serial data is sent into the Data Recovery (CDR). The selection is between the main LVDS buffer and the protect LVDS buffer. The work LVDS buffers are TXDxx\_W\_[P:N], while the protect LVDS buffers are TXDxx\_P\_[P:N]. When operating using the LVDS buffers (default), no status information is available on the protect LVDS buffers since the serial stream must reach the SONET framer before status information is available on the data stream. The same is also true for the work LVDS buffers.

There are two ways to control the LVDS protection switching, interface and software control. On the FPGA interface, there are eight input signals to the ORT8850 core that will select between the work and protect LVDS buffers.

FPGA Interface Signal	When '0'	When '1'
LVDS_PROT_AA	Channel AA gets TXD_AA_W_[P:N]	Channel AA gets TXD_AA_P_[P:N]
LVDS_PROT_AB	Channel AB gets TXD_AB_W_[P:N]	Channel AB gets TXD_AB_P_[P:N]
LVDS_PROT_AC	Channel AC gets TXD_AC_W_[P:N]	Channel AC gets TXD_AC_P_[P:N]
LVDS_PROT_AD	Channel AD gets TXD_AD_W_[P:N]	Channel AD gets TXD_AD_P_[P:N]

#### Table 18. LVDS Protection Switching

FPGA Interface Signal	When '0'	When '1'
LVDS_PROT_BA	Channel BA gets TXD_BA_W_[P:N]	Channel BA gets TXD_BA_P_[P:N]
LVDS_PROT_BB	Channel BB gets TXD_BB_W_[P:N]	Channel BB gets TXD_BB_P_[P:N]
LVDS_PROT_BC	Channel BC gets TXD_BC_W_[P:N]	Channel BC gets TXD_BC_P_[P:N]
LVDS_PROT_BD	Channel BD gets TXD_BD_W_[P:N]	Channel BD gets TXD_BD_P_[P:N]

Table 18. LVDS Protection Switching (Continued)

For software control of the LVDS protection switching there is an enable bit to enable software control, and a bit per channel which selects main or protect. The enable register is at 0x30008 in the memory map (Table 19).

# **Memory Map**

The memory map for the ORT8850 core is only part of the full memory map of the ORT8850 device. The ORT8850 is an ORCA Series4 based device and thus uses the system bus as a communication bridge. The ORT8850 core register map contained in this data sheet only covers the embedded ASIC core of the device, not the entire device. The system bus itself, and the generic FPGA memory map, are fully documented in the MPI/System Bus Application Note. As part of the system bus, the embedded ASIC core of an FPSC is located at address offset 0x30000. The ORT8850 embedded core is an eight-bit slave interface on the Series 4 system bus.

Each ORCA device contains a device ID. This device ID is unique to each ORCA device and can be used for device identification and assist in system debugging. The device ID is located at absolute address 0x00000 - 0x00003. The ORT8850H's device ID is 0xDC0123C0 and the ORT8850L's device ID is 0xDC0121C0. More information on the device ID and other Series 4 generic registers can be found in the MPI/System Bus Application Note.

The ORT8850 core registers are clocked by the reference clock SYS\_CLK\_P/N. If a clock is not provided to the reference clock, the registers will fail to operate.

The ORT8850 core registers do not check for parity on a write operation. On a read operation, no parity is generated, and a "0" is passed back to the initiating bus master interface on the parity signal line.

# **Registers Access and General Description**

The memory map comprises three address blocks:

- Generic register block: ID, revision, scratch pad, lock and reset register.
- Device register block: control and status bits, common to the eight channels in each of the two quad interfaces.
- Channel register blocks: each of the four channels in both quads have an address block. The four address blocks in both quads have the same structure, with a constant address offset between channel register blocks.

All registers are write-protected by the lock register, except for the scratch pad register. The lock register is a 16-bit read/write register. Write access is given to registers only when the key value 0x0580 is present in the lock register. An error flag will be set upon detecting a write access when write permission is denied. The default value is 0x0000.

After power-up reset or soft reset, unused register bits will be read as zeros. Unused address locations are also read as zeros. Bit in write-only registers will always be read as zeros.

This table is constructed to show the correct values when read and written via the system bus MPI interface. When using this table while interfacing with the system bus user logic master interface, the data values will need to be byte flipped. This is due to the opposite orientation of the MPI and master interface bus ordering. More information on this can be found in the MPI/System Bus Application Note (TN1017).

Table 19.	Memory Map	Descriptions	(Continued)
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(0x) Absolute Address	Bit	Туре	Name	Reset Value (0x)	Description
	[0:3]	R/W	number of consec- utive A1 A2 errors to generate [0:3]	00	If a particular channel's "A1 A2 error insert command" control bit is set to the value 1 then the "A1 and A2 error insert values" will be inserted into that channels respective A1 and A2 bytes. The number of consecutive frames to be corrupted is deter- mined by the "number of consecutive A1 A2 errors to generate [0:3]" control bits. MSB is bit 3
3000C	[4]	R/W	backplane side loopback control	0	0 = No loopback. 1 = RX to TX loopback on backplane side. Serial input is run through SERDES and SONET block, then looped back in paral- lel to SERDES and out serial.
	[5]	R/W	DINxx/DOUTxx parallel bus parity control	1	0 = Odd parity 1 = Even parity
	[6]	R/W	scram- bler/descrambler	1	0 = no RX direction, descramble / TX direction scramble 1 = In RX direction, descramble channel after the SONET frame recovery. In TX direction, scramble data just before parallel-to- serial conversion
	[7]	-	Not Used	0	
3000D	[0:7]	R/W	A1 error insert value [0:7]	00	Value of the A1 byte for error insert
3000E	[0:7]	R/W	A2 error insert value [0:7]	00	Value of the A2 byte for error insert
3000F	[0:7]	R/W	transmit B1 error insert mask [0:7]	00	0 = No error insertion. 1 = Invert corresponding bit in B1 byte.
[0] R		AA alarm	0	Consolidation alarm for channel AA 1 = alarm 0 = no alarm.	
	[1]	R	AB alarm	0	Consolidation alarm for channel AB 1 = alarm 0 = no alarm.
30010	[2]	R	AC alarm	0	Consolidation alarm for channel AC 1 = alarm 0 = no alarm.
[3] F		R	AD alarm	0	Consolidation alarm for channel AD 1 = alarm 0 = no alarm.
	[4-7]	-	Not Used	0	
	[0]	R/W	AA/BA alarm enable/mask regis- ter	0	AA and BA enable 1 = enabled 0 = not enabled
	[1]	R/W	AB/BB alarm enable/mask regis- ter	0	AB and BB enable 1 = enabled 0 = not enabled
30011	[2]	R/W	AC/BC alarm enable/mask regis- ter	0	AC and BC enable 1 = enabled 0 = not enabled
	[3]	R/W	AD/BD alarm enable/mask regis- ter	0	AD and BD enable 1 = enabled 0 = not enabled
	[4-7]	-	Not Used	0	

# **HSI Electrical and Timing Characteristics**

# Table 22. Maximum Power Dissipation

Parameter	Conditions	Min.	Тур.	Max.	Units
Power Dissipation	SERDES, scrambler/descrambler, framer, FIFO alignment, pointer mover, and I/O (per channel), 622 Mbtis/s			125	mW

1. With all channels operating, 1.575 V and 3.6 V supplies,  $85^{\circ}$ C.

#### Table 23. Recommended Operating Conditions

Parameter	Conditions	Min.	Тур.	Max.	Units
VDD15 Supply Voltage		1.425	—	1.575	V
Junction Temperature	TJ	-40	_	125	°C

#### Table 24. Receiver Specifications

Parameter	Conditions	Тур.	Max.	Units	
Input Data					
Stream of Nontransitions <sup>1</sup>	_	—	_	72	bits
Phase Change, Input Signal	Over a 200 ns time interval <sup>2</sup>	—	_	100	ps
Eye Opening <sup>3</sup>	—	0.4			Ulp-p
Jitter Tolerance @ 622 Mbits/s, Worst Case	300 MV diff eye <sup>4</sup>	—		0.6	Ulp-p
Jitter Tolerance @ 155 Mbits/s, Worst Case	250 MV diff eye⁵	—		0.85	Ulp-p

1. This sequence should not occur more than once per minute.

2. Translates to a frequency change of 500 ppm.

3. A unit interval for 622.08 Mbits/s data is 1.6075 ns.

4. With STS-12 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., TA=0°C to 85°C, 1.425 V to 1.575 V supply. Jitter measured with a Wavecrest SIA-3000.

5. With STS-3 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., TA=0°C to 85°C, 1.425 V to 1.575 V supply. Jitter measured with a Wavecrest SIA-3000.

#### Table 25. Channel Output Jitter (622 Mbits/s)

Parameter	Conditions	Min.	Typ. <sup>1</sup>	Max. <sup>1</sup>	Units
Deterministic		—	0.09	0.10	Ulp-p
Random		—	0.11	0.14	Ulp-p
Total <sup>2,3</sup>		_	0.20	0.24	Ulp-p

1. With PRBS 2^7 data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0°C to 85°C, 1.425 V to 1.575 V supply.

2. Wavecrest SIA-3000 instrument used to measure one-sigma (rms) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10<sup>-12</sup>.

Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10<sup>-12</sup>. See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

#### Table 26. Channel Output Jitter (155 Mbits/s)

Parameter	Conditions	Min.	Typ. <sup>1</sup>	Max. <sup>1</sup>	Units
Deterministic		-	0.027	0.035	Ulp-p
Random		—	0.053	0.065	Ulp-p
Total <sup>2,3</sup>			0.08	0.10	Ulp-p

1. With PRBS 2<sup>7</sup> data pattern, all channels operating, FPGA logic active, REFCLK jitter of 30 ps., 0°C to 85°C, 1.425 V to 1.575 V supply.

2. Wavecrest SIA-3000 instrument used to measure one-sigma (rms) random jitter component value. This value is multiplied by 14 to provide the peak-to-peak value that corresponds to a BER of 10<sup>-12</sup>.

Total jitter measurement performed with Wavecrest SIA-3000 at a BER of 10<sup>-12</sup>. See instrument documentation and other Wavecrest publications for a detailed discussion of jitter types included in this measurement.

#### Table 27. Synthesizer Specifications

Parameter	Conditions	Min	Typical	Max	Unit
PLL <sup>1</sup>				1	
Loop Bandwidth		—	_	6	MHz
Jitter Peaking		—		2	dB
power-up Reset Time	_	10	_	—	μS
Lock Acquisition Time		—		1	ms
Input Reference Clock					
Frequency	—	62.5	_	106.25	MHz
Frequency Deviation <sup>2</sup>	_	-350	_	350	ppm
Phase Change	Over a 200 ns time interval <sup>3</sup>	—	—	100	ps

1. External 10 k $\Omega$  resistor to analog ground required.

2. The frequency deviation allowed between the transmitter reference clock and receiver reference clock on a given link.

3. Translates to a frequency change of 500 ppm.

# **Pin Information**

This section describes the pins and signals that perform FPGA-related functions. During configuration, the userprogrammable I/Os are 3-stated and pulled up with an internal resistor. If any FPGA function pin is not used (or not bonded to package pin), it is also 3-stated and pulled up after configuration.

Table 32. FPGA Common-Function Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD33	_	3.3 V positive power supply. This power supply is used for 3.3 V configuration RAMs and internal PLLs. When using PLLs, this power supply should be well isolated from all other power supplies on the board for proper operation.
VDD15	—	1.5 V positive power supply for internal logic.
VDDIO	—	Positive power supply used by I/O banks.
Vss	-	Ground.
PTEMP	I	Temperature sensing diode pin. Dedicated input.
RESET	I	During configuration, RESET forces the restart of configuration and a pull-up is enabled. After con- figuration, RESET can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously SET/RESET.
CCLK	0	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in.
	I	In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.*
	0	As an active-high, open-drain output, a high level on this signal indicates that configuration is com- plete. DONE has an optional pull-up resistor.
PRGM	I	PRGM is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
RD_CFG	I	This pin must be held high during device initialization until the INIT pin goes high. This pin always has an active pull-up. During configuration, RD_CFG is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, RD_CFG can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on RD_CFG will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	0	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
CFG_IRQ/MPI_IRQ	0	During JTAG, slave, master, and asynchronous peripheral configuration assertion on this CFG_IRQ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output, when the MPI is used.

1. The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Symbol	I/O	Description				
Special-Purpose Pir	าร					
M[3:0]	I	During power-up and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of INIT. During configuration, a pull-up is enabled.				
	I/O	After configuration, these pins are user-programmable I/O.*				
PLL_CK[0:7][TC]	I	Semi-dedicated PLL clock pins. During configuration they are 3-stated with a pull up.				
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.				
P[TBLR]CLK[1:0][T	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.				
[C]	I/O	After configuration these pins are user-programmable I/O, if not used for clock inputs.				
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.				
	I/O	After configuration, these pins are user-programmable I/O in boundary scan is not used.*				
RDY/BUSY/RCLK	0	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.				
	I/O	After configuration this pin is a user-programmable I/O pin.*				
HDC	0	High during configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.				
	I/O	ter configuration, this pin is a user-programmable I/O pin.*				
LDC	0	Low during configuration is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.				
	I/O	After configuration, this pin is a user-programmable I/O pin.*				
INIT	I/O	<b>INIT</b> is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, INIT is held low during power stabilization and internal clearing of memory. As an active-low input, INIT holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.*				
<u>CS0</u> , CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.				
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.*				
RD/MPI_STRB	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. WR and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.				
WR/MPI_RW	I	$\overline{\text{WR}}$ is used in asynchronous peripheral mode. A low on $\overline{\text{WR}}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write trans- fer to the FPGA.				
	I/O	After configuration, if the MPI is not used, $\overline{\text{WR}}/\text{MPI}_{\text{RW}}$ is a user-programmable I/O pin.*				
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the <i>PowerPC</i> bus master utilizing the least-significant bits of the <i>PowerPC</i> 32-bit address.				
MPI_BURST	I	MPI_BURST is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indi- cates that the current transfer is not a burst.				

#### Table 32. FPGA Common-Function Pin Descriptions (Continued)

The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

### Table 32. FPGA Common-Function Pin Descriptions (Continued)

Symbol	I/O	Description
MPI_BDIP	I	MPI_BDIP is driven by the <i>PowerPC</i> processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	0	During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_ACK	0	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_CLK	I	This is the <i>PowerPC</i> synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the embedded system bus. If MPI is used this will be the <i>AMBA</i> bus clock.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_TEA	0	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the inter- nal system bus for the current transaction.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_RTRY	0	This pin requests the MPC860 to relinquish the bus and retry the cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
D[0:31]	I/O	Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write trans- action and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	0	D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.*
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.*
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data syn- chronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
DOUT	0	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.*
TESTCFG	I	During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user programmable I/O pin.*
LVDS_R	—	Reference resistor connection for controlled impedance termination of Series 4 FPGA LVDS inputs.

1. The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

 

 Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
AB1	7 (CL)	6	IO	PL17A	PL29C	A7/PPC A21	L20T D3
AA5	7 (CL)	6	IO	PL18D	PL30D	A6/PPC A20	L21C A1
AA3	7 (CL)	6	IO	PL18C	PL30C		 L21T_A1
U1	7 (CL)	_	VDDIO7	VDDIO7	VDDIO7		
AB2	7 (CL)	7	IO	PL18B	PL31D	_	
AA4	7 (CL)	7	IO	PL19D	PL32D	WR_N/MPI_RW	L22C_D2
AC1	7 (CL)	7	IO	PL19C	PL32C	VREF_7_07	L22T_D2
AB5	7 (CL)	7	IO	PL19B	PL33D	—	L23C_D2
AC2	7 (CL)	7	IO	PL19A	PL33C	—	L23T_D2
AB4	7 (CL)	8	IO	PL20D	PL34D	A4/PPC_A18	L23C_D0
AC5	7 (CL)	8	IO	PL20C	PL34C	VREF_7_08	L23T_D0
W1	7 (CL)	_	VDDIO7	VDDIO7	VDDIO7	—	
AD2	7 (CL)	8	IO	PL20B	PL35D	A3/PPC_A17	L23C_D0
AE1	7 (CL)	8	IO	PL20A	PL35C	A2/PPC_A16	L23T_D0
AD3	7 (CL)	8	IO	PL21D	PL36D	A1/PPC_A15	L24C_D0
AE2	7 (CL)	8	IO	PL21C	PL36C	A0/PPC_A14	L24T_D0
AF1	7 (CL)	8	IO	PL21B	PL37D	DP0	L25C_D2
AD4	7 (CL)	8	IO	PL21A	PL37C	DP1	L25T_D2
AE3	6 (BL)	1	IO	PL22D	PL38D	D8	L1C_D0
AF2	6 (BL)	1	IO	PL22C	PL38C	VREF_6_01	L1T_D0
AB13	—	-	Vss	Vss	Vss	—	—
AE4	6 (BL)	1	IO	PL22B	PL39D	D9	L2C_D0
AF3	6 (BL)	1	IO	PL22A	PL39C	D10	L2T_D0
AE5	6 (BL)	2	IO	PL23D	PL40D	—	L3C_D1
AG2	6 (BL)	2	IO	PL23C	PL40C	VREF_6_02	L3T_D1
AK5	6 (BL)	—	VDDIO6	VDDIO6	VDDIO6	—	—
AH1	6 (BL)	2	IO	PL23B	PL41D	—	L4C_D3
AF5	6 (BL)	2	IO	PL23A	PL41C	—	L4T_D3
AF4	6 (BL)	3	IO	PL24D	PL42D	D11	L5C_D0
AG3	6 (BL)	3	IO	PL24C	PL42C	D12	L5T_D0
AB14	—	—	Vss	Vss	Vss	—	
AH2	6 (BL)	3	IO	PL24B	PL43D	—	L6C_D0
AJ1	6 (BL)	3	IO	PL24A	PL43C	—	L6T_D0
AG4	6 (BL)	3	IO	PL25D	PL44D	VREF_6_03	L7C_A0
AG5	6 (BL)	3	IO	PL25C	PL44C	D13	L7T_A0
AL3	6 (BL)	_	VDDIO6	VDDIO6	VDDIO6	—	_
AH3	6 (BL)	4	10	PL25B	PL44B	—	
AK1	6 (BL)	4	10	PL25A	PL45A	—	
AJ2	6 (BL)	4	IO	PL26D	PL45D	—	L8C_D2
AH5	6 (BL)	4	IO	PL26C	PL45C	VREF_6_04	L8T_D2
AB15	—		Vss	Vss	Vss		
AH4	6 (BL)	4	IO	PL26B	PL46D	—	—

 

 Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
E7	_		IO	PCCLK	PCCLK	CCLK	_
D5			IO	PDONE	PDONE	DONE	
E6	_		VDD33	VDD33	VDD33	_	_
B34	_		Vss	Vss	Vss	_	_
A24	1 (TC)		VDDIO1	VDDIO1	VDDIO1	_	
AM23	5 (BC)	_	VDDIO5	VDDIO5	VDDIO5	_	
AP1		_	Vss	Vss	Vss	_	
K4	0 (TL)	10	IO	UNUSED	PL11A	_	
M5	0 (TL)	10	IO	UNUSED	PL13A	_	
R5	7 (CL)	3	IO	UNUSED	PL20A	_	
T5	7 (CL)	3	IO	UNUSED	PL21A	_	
W4	7 (CL)	5	IO	UNUSED	PL27A	—	
AA2	7 (CL)	6	IO	UNUSED	PL28A	—	—
Y4	7 (CL)	6	IO	UNUSED	PL29A	—	—
AC4	7 (CL)	8	IO	UNUSED	PL35A	—	—
AD5	7 (CL)	8	IO	UNUSED	PL37A	—	
AG1	6 (BL)	1	IO	UNUSED	PL38A	—	
AK10	6 (BL)	7	IO	UNUSED	PB9A	—	—
AK11	6 (BL)	7	IO	UNUSED	PB10A	—	_
AM9	6 (BL)	8	IO	UNUSED	PB11A	—	—
AN9	6 (BL)	8	IO	UNUSED	PB12A	—	—
AM14	6 (BL)	11	IO	UNUSED	PB19A	—	_
AN14	6 (BL)	11	IO	UNUSED	PB20A	—	—
D11	0 (TL)	3	IO	UNUSED	PT12A	—	_
E13	0 (TL)	3	IO	UNUSED	PT11A	—	_
AP4	6 (BL)	5	IO	UNUSED	PB3A	—	_
Y3	7 (CL)		VDDIO7	VDDIO7	VDDIO7	—	_
AC3	7 (CL)		VDDIO7	VDDIO7	VDDIO7	—	—
AD1	7 (CL)	_	VDDIO7	VDDIO7	VDDIO7	—	—
AP11	5 (BC)	_	VDDIO5	VDDIO5	VDDIO5	—	—
AP17	5 (BC)	—	VDDIO5	VDDIO5	VDDIO5	—	
AP19	5 (BC)	—	VDDIO5	VDDIO5	VDDIO5	—	—
AP24	5 (BC)	—	VDDIO5	VDDIO5	VDDIO5	—	—
C12	1 (TC)	—	VDDIO1	VDDIO1	VDDIO1	—	—
C15	1 (TC)	—	VDDIO1	VDDIO1	VDDIO1	—	—
C20	1 (TC)	—	VDDIO1	VDDIO1	VDDIO1	—	—
C23	1 (TC)		VDDIO1	VDDIO1	VDDIO1	—	
W22			VDD15	VDD15	VDD15	—	
Y16			VDD15	VDD15	VDD15		_
V22		_	VDD15	VDD15	VDD15	—	_
U22			VDD15	VDD15	VDD15		_
T22			VDD15	VDD15	VDD15		

 

 Table 36. ORT8850L and ORT8850H 680-Pin PBGAM Pinout (note: pins labeled "Reserved" should be left unconnected) (Continued)

BM680	VDDIO Bank	VREF Group	I/O	ORT8850L	ORT8850H	Additional Function	Pair
C3	—	_	Vss	Vss	Vss	—	_
C13	—	_	Vss	Vss	Vss	_	_
AP2	—	_	Vss	Vss	Vss	_	_
AP18	—	_	Vss	Vss	Vss	—	
AP33	—	_	Vss	Vss	Vss	_	_
AP34	—	_	Vss	Vss	Vss	_	_
AA20	—	_	Vss	Vss	Vss	—	
AA21	—	_	Vss	Vss	Vss	_	_
AA22	—	_	Vss	Vss	Vss	_	_
N21	—	_	Vss	Vss	Vss	—	
N22	—	_	Vss	Vss	Vss	_	_
AB3	—	_	Vss	Vss	Vss	—	
AB19	—	—	VDD15	VDD15	VDD15	—	_
N20	—	_	Vss	Vss	Vss	—	

Note: Pins labeled "reserved" should be left unconnected.