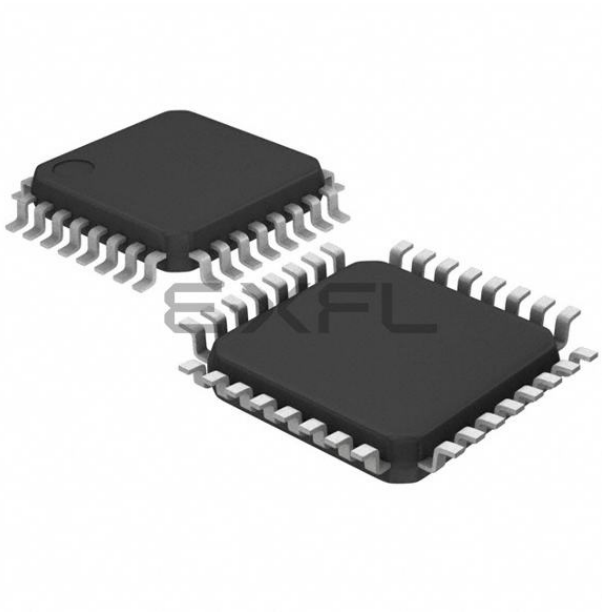

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f32g-a-qfp32

1. Feature List

The EFM8UB2 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 48 MHz maximum operating frequency
- Memory:
  - Up to 64 KB flash memory, in-system re-programmable from firmware.
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Internal 5-to-3.3 V LDO allows direct connection to USB supply net
  - Power-on reset circuit and brownout detectors
- I/O: Up to 40 total multifunction I/O pins:
  - Flexible peripheral crossbar for peripheral routing
  - 10 mA source, 25 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 48 MHz precision oscillator (±1.5% accuracy without USB clock recovery, ±0.25% accuracy with USB clock recovery)
  - Internal 80 kHz low-frequency oscillator
  - External crystal, RC, C, and CMOS clock options
- Timers/Counters and PWM:
  - 5-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes with watchdog timer function
  - 6 x 16-bit general-purpose timers
- Communications and Digital Peripherals:
  - Universal Serial Bus (USB) Function Controller with eight flexible endpoint pipes, integrated transceiver, and 1 KB FIFO RAM
  - 2 x UART
  - SPI™ Master / Slave
  - 2 x SMBus™/I2C™ Master / Slave
  - External Memory Interface (EMIF)
- Analog:
  - 10-Bit Analog-to-Digital Converter (ADC0)
  - 2 x Low-current analog comparators
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded USB bootloader
- Temperature range -40 to 85 ºC
- Single power supply 2.65 to 3.6 V
- QFP48, QFP32, and QFN32 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.65 to 3.6 V operation and is available in 32-pin QFN, 32-pin QFP, or 48-pin QFP packages. All package options are lead-free and RoHS compliant.

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN48	P3.7
QFP32	P3.0 / C2D
QFN32	P3.0 / C2D

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 11, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.7[2]	3.3	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}		2.7	—	5.25	V
System Clock Frequency	f_{SYSCLK}		0	—	48	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. All voltages with respect to GND
2. The USB specification requires 3.0 V minimum supply voltage.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 48 MHz[2]	—	12	14	mA
		F_{SYSCLK} = 24 MHz[2]	—	7	8	mA
		F_{SYSCLK} = 80 kHz[3]	—	280	—	µA
Idle Mode—Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 48 MHz[2]	—	6.5	8	mA
		F_{SYSCLK} = 24 MHz[2]	—	3.5	5	mA
		F_{SYSCLK} = 80 kHz[3]	—	220	—	µA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off. Regulators in low-power mode.	I_{DD}	LFO Running	—	105	—	µA
		LFO Stopped	—	100	—	µA
Stop Mode—Core halted and all clocks stopped, Regulators in low-power mode, Supply monitor off.	I_{DD}		—	100	—	µA
Shutdown Mode—Core halted and all clocks stopped,Regulators Off, Supply monitor off.	I_{DD}		—	0.25	—	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 48 MHz, T_A = 25 °C	—	900	—	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	5	—	µA
ADC0 Supply Current	I_{ADC}	Operating at 500 ksps V_{DD} = 3.0 V	—	750	1000	µA
On-chip Precision Reference	I_{VREFP}		—	75	—	µA
Temperature Sensor	I_{TSENSE}		—	35	—	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	1	—	µA
		CPMD = 10	—	4	—	µA
		CPMD = 01	—	10	—	µA
		CPMD = 00	—	20	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	50	µA
Regulator Bias Currents	I_{VREG}	Both Regulators in Normal Mode	—	200	—	µA
		Both Regulators in Low Power Mode	—	100	—	µA
		5 V Regulator Off, Internal LDO in Low Power Mode	—	150	—	µA
USB (USB0) Full-Speed	I_{USB}	Active	—	8	—	mA

4.1.8 ADC

Table 4.8. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}			10		Bits
Throughput Rate	f_S		—	—	500	ksps
Tracking Time	t_{TRK}		300	—	—	ns
SAR Clock Frequency	f_{SAR}		—	—	8.33	MHz
Conversion Time	t_{CNV}	10-Bit Conversion,	13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}		—	30	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Single-Ended (AIN+ - GND)	0	—	V_{REF}	V
		Differential (AIN+ - AIN-)	$-V_{REF}$	—	V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance, VREF = 2.4 V						
Integral Nonlinearity	INL		—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Offset Error	E_{OFF}		-2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.005	—	LSB/°C
Slope Error	E_M		—	-0.2	±0.5	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, VREF = 2.4 V						
Signal-to-Noise	SNR		55	58	—	dB
Signal-to-Noise Plus Distortion	SNDR		55	58	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD		—	-73	—	dB
Spurious-Free Dynamic Range	SFDR		—	78	—	dB

Note:
1. Absolute input pin voltage is limited by the VDD and GND supply pins.

4.1.9 Voltage Reference

Table 4.9. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
On-chip Precision Reference						
Output Voltage	V_{REFP}	T = 25 °C	2.38	2.42	2.46	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin	—	3	—	ms
		0.1 µF ceramic bypass on VREF pin	—	100	—	µs
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to GND	—	360	—	µV / µA
Short-circuit current	ISC_{VREFP}		—	—	8	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	140	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 500 ksps; VREF = 3.0 V	—	9	—	µA

4.1.10 Temperature Sensor

Table 4.10. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	764	—	mV
Offset Error[1]	E_{OFF}	T_A = 0 °C	—	15	—	mV
Slope	M		—	2.87	—	mV/°C
Slope Error[1]	E_M		—	120	—	µV/°C
Linearity			—	0.5	—	°C
Turn-on Time			—	1.8	—	µs

Note:
1. Represents one standard deviation from the mean.

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	250	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.05	—	µs
		-100 mV Differential	—	5.2	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

4.1.15 SMBus

Table 4.15. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		0	—	—	µs
Data Setup Time	$t_{SU:DAT}$		4.7	—	—	µs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[3]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	256[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	256[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		0	—	—	µs
Data Setup Time	$t_{SU:DAT}$		1.3	—	—	µs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[3]	µs

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

Table 4.16. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:
1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

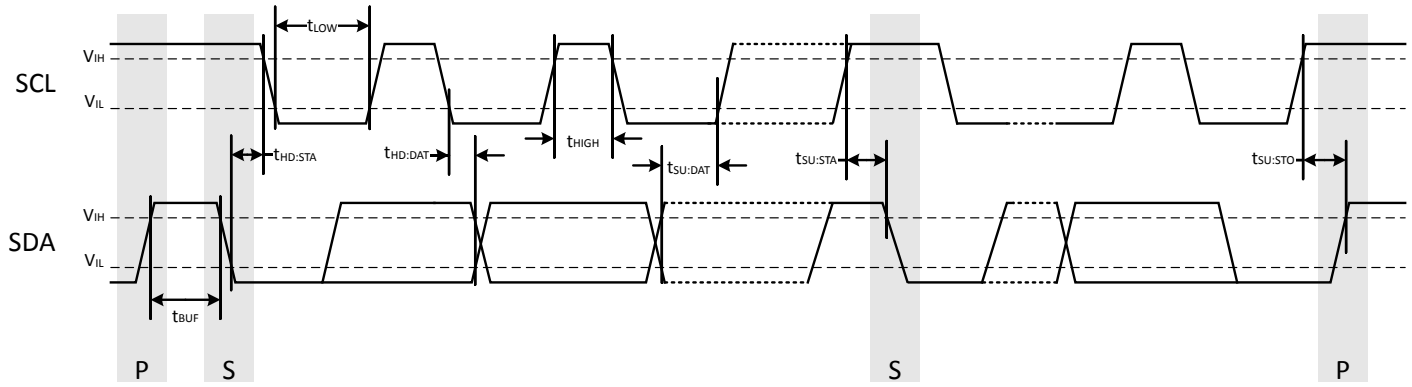


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.17. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFP48 Packages	—	60	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QFN32 Packages	—	28	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (bus-powered). The VBUS signal is used to detect when USB is connected to a host device.

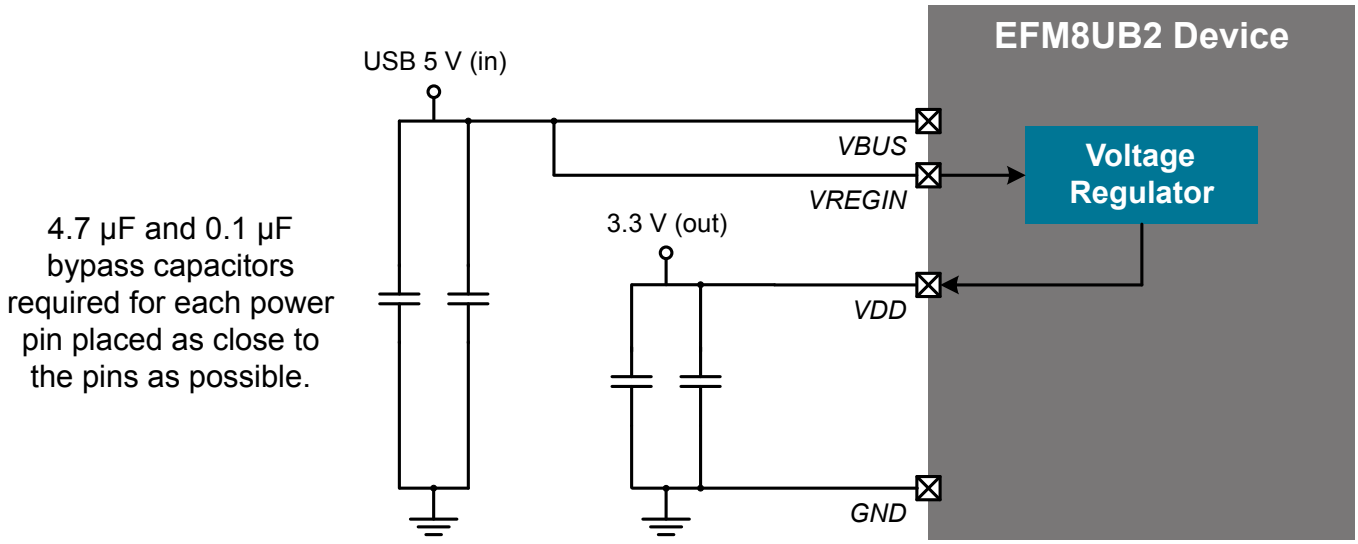


Figure 5.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (self-powered). The VBUS signal is used to detect when USB is connected to a host device and is shown with a resistor divider. This resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification for self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V.

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P4.4	Multifunction I/O		EMIF_D4 EMIF_AD4m	ADC0P.13 ADC0N.13 CMP0N.3
19	P4.3	Multifunction I/O		EMIF_D3 EMIF_AD3m	ADC0P.12 ADC0N.12 CMP0P.3
20	P4.2	Multifunction I/O		EMIF_D2 EMIF_AD2m	ADC0P.33 ADC0N.33
21	P4.1	Multifunction I/O		EMIF_D1 EMIF_AD1m	ADC0P.32 ADC0N.32
22	P4.0	Multifunction I/O		EMIF_D0 EMIF_AD0m	ADC0P.11 ADC0N.11 CMP1N.2
23	P3.7	Multifunction I/O	Yes	EMIF_A7 EMIF_A15m	ADC0P.10 ADC0N.10 CMP1P.2
24	P3.6	Multifunction I/O	Yes	EMIF_A6 EMIF_A14m	ADC0P.29 ADC0N.29
25	P3.5	Multifunction I/O	Yes	EMIF_A5 EMIF_A13m	ADC0P.9 ADC0N.9 CMP0N.2
26	P3.4	Multifunction I/O	Yes	EMIF_A4 EMIF_A12m	ADC0P.8 ADC0N.8 CMP0P.2
27	P3.3	Multifunction I/O	Yes	EMIF_A3 EMIF_A11m	ADC0P.28 ADC0N.28
28	P3.2	Multifunction I/O	Yes	EMIF_A2 EMIF_A10m	ADC0P.27 ADC0N.27
29	P3.1	Multifunction I/O	Yes	EMIF_A1 EMIF_A9m	ADC0P.7 ADC0N.7 CMP1N.1
30	P3.0	Multifunction I/O	Yes	EMIF_A0 EMIF_A8m	ADC0P.6 ADC0N.6 CMP1P.1
31	P2.7	Multifunction I/O	Yes	EMIF_A15	ADC0P.26 ADC0N.26

6.2 EFM8UB2x-QFP32 Pin Definitions

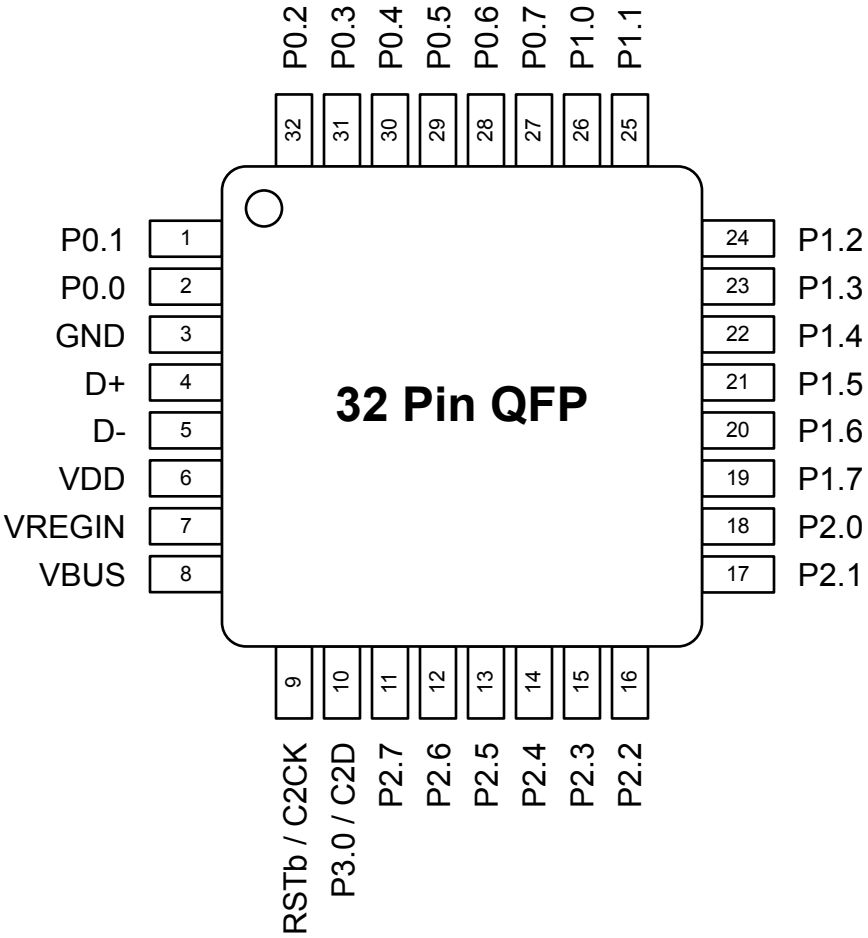


Figure 6.2. EFM8UB2x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8UB2x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	ADC0P.18 ADC0N.18 CMP0N.4
2	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	ADC0P.17 ADC0N.17 CMP0P.4
3	GND	Ground			
4	D+	USB Data Positive			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
32	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
Note: XTAL1 and XTAL2 are not available on this package. EXTCLK is still available on P0.3.					

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.4	Multifunction I/O	Yes	INT0.4 INT1.4 UART0_TX	ADC0P.19 ADC0N.19 CMP1P.4
31	P0.3	Multifunction I/O	Yes	EXTCLK INT0.3 INT1.3	
32	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
Center	GND	Ground			
Note: XTAL1 and XTAL2 are not available on this package. EXTCLK is still available on P0.3.					

7.2 QFP48 PCB Land Pattern

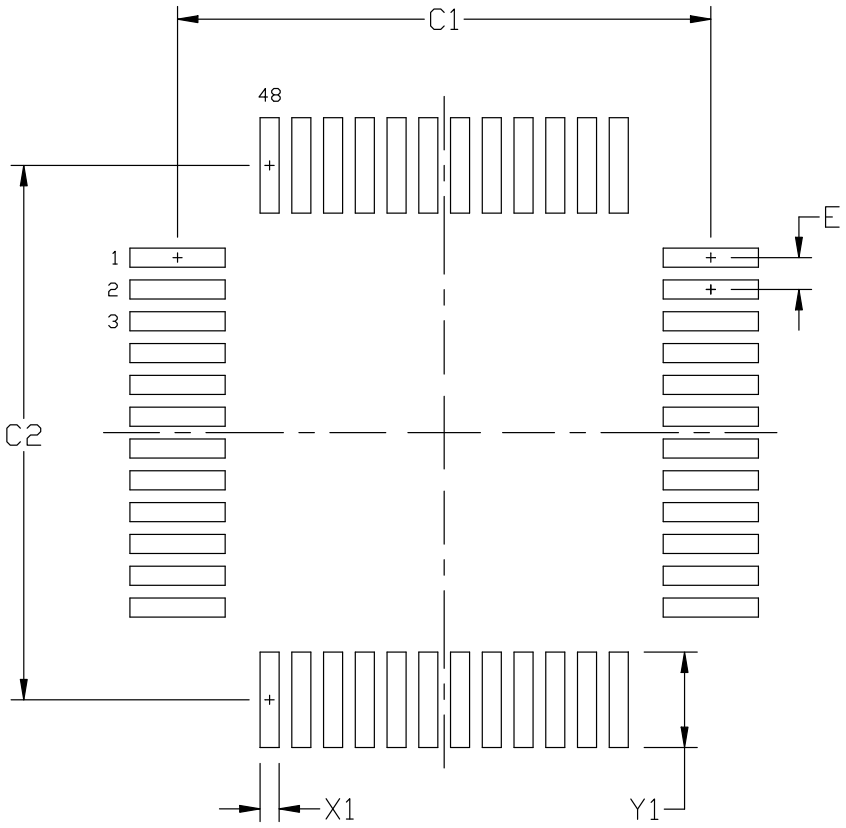


Figure 7.2. QFP48 PCB Land Pattern Drawing

Table 7.2. QFP48 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.30	8.40
C2	8.30	8.40
E	0.50 BSC	
X1	0.20	0.30
Y1	1.40	1.50

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

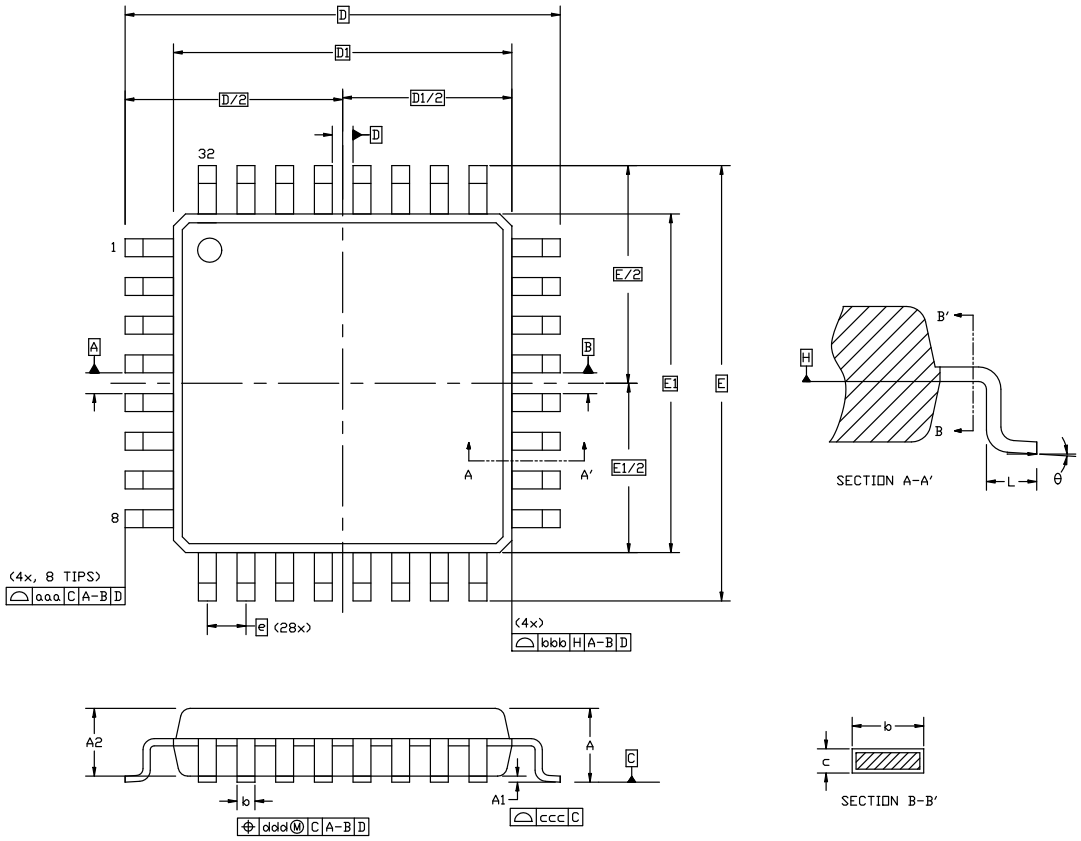


Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D		9.00 BSC	
D1		7.00 BSC	
e		0.80 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
aaa		0.20	

9.2 QFN32 PCB Land Pattern

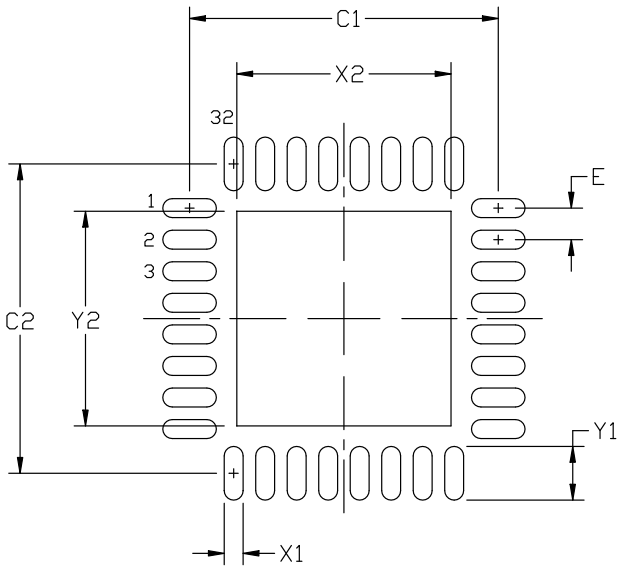


Figure 9.2. QFN32 PCB Land Pattern Drawing

Table 9.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.3 QFN32 Package Marking

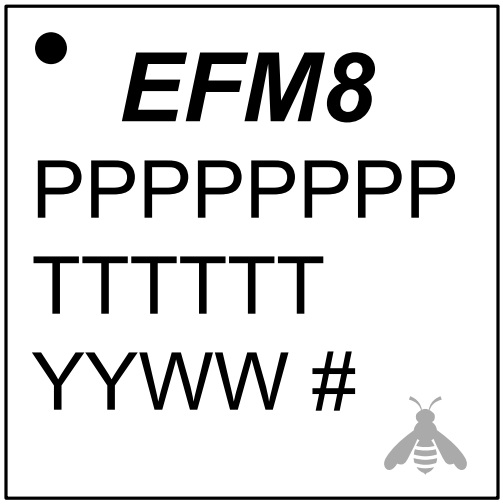
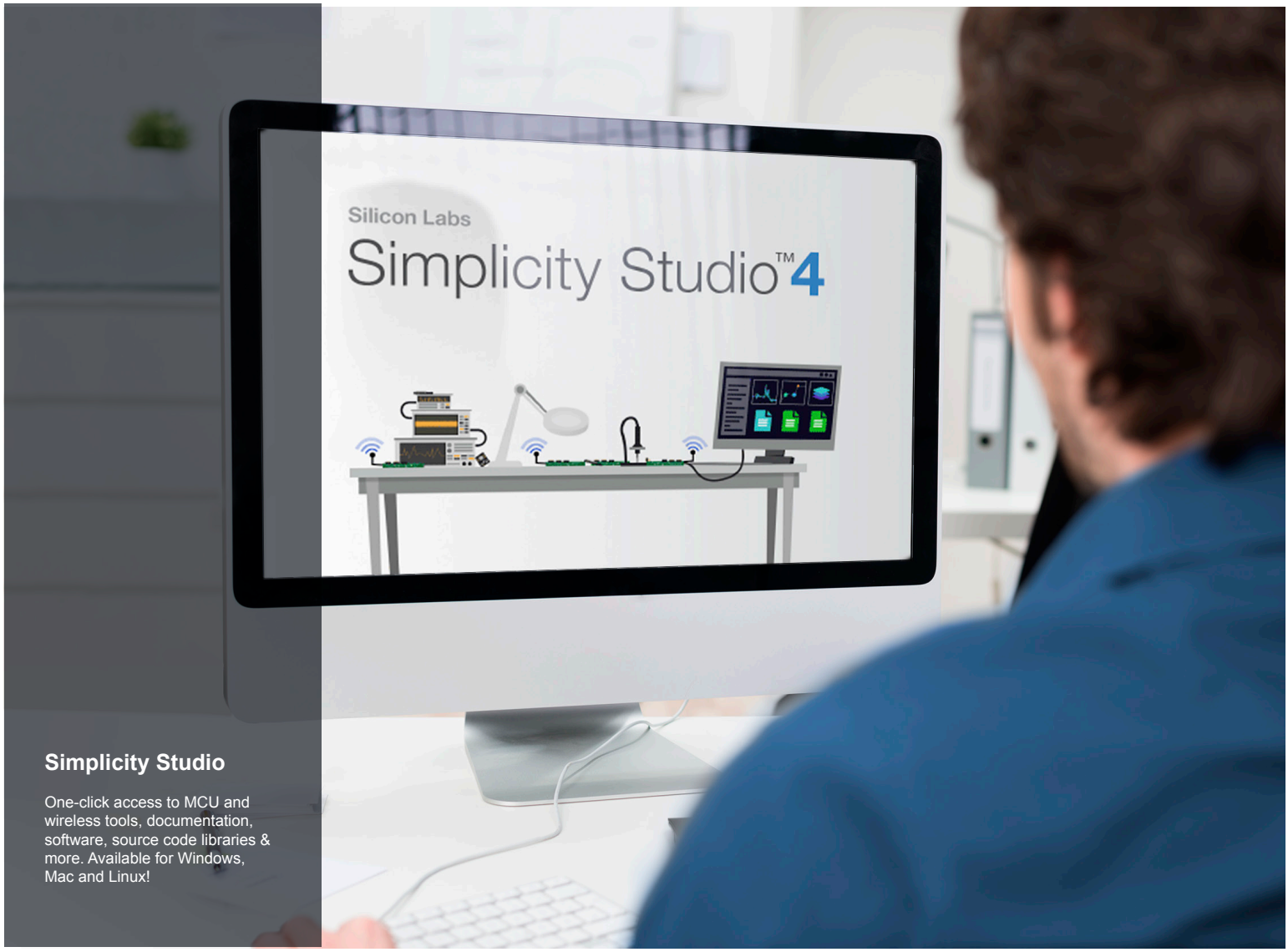


Figure 9.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).



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