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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	EBI/EMI, I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f32g-a-qfp48

3. System Overview

3.1 Introduction

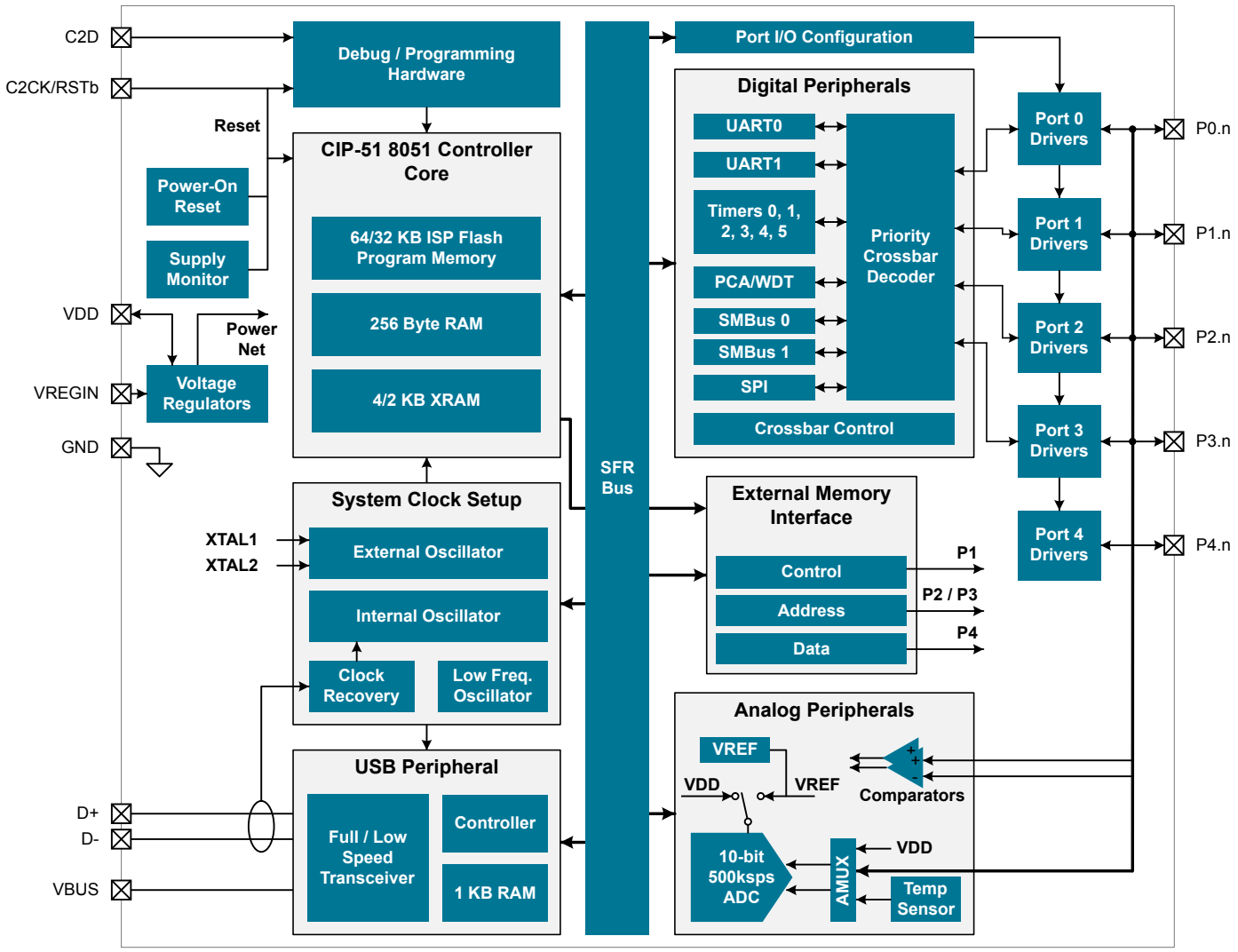

Figure 3.1. Detailed EFM8UB2 Block Diagram

This section describes the EFM8UB2 family at a high level. For more information on each module including register definitions, see the EFM8UB2 Reference Manual.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and peripheral clocks halted • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SUSPEND bit in HFO0CN	USB0 Bus Activity
Stop	• All internal power nets shut down • Pins retain state • Exit on any reset source	Set STOP bit in PCON0	Any reset source
Shutdown	• All internal power nets shut down • 5V regulator remains active (if enabled) • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG01CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P3.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P4.0-P4.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 on some packages.

- Up to 40 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1) available on P0 pins.

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 48 MHz oscillator divided by 4, then divided by 8 (1.5 MHz).

- Provides clock to core and peripherals.
- 48 MHz internal oscillator (HFOSC0), accurate to ±1.5% over supply and temperature corners: accurate to +/- 0.25% when using USB clock recovery.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK) for QFP48 packages.
- External CMOS clock option (EXTCLK) for QFP32 and QFN32 packages.
- Internal oscillator has clock divider with eight settings for flexible clock scaling: 1, 2, 4, or 8.

3.6 Communications and Other Digital Peripherals

Universal Serial Bus (USB0)

The USB0 module provides Full/Low Speed function for USB peripheral implementations. The USB function controller (USB0) consists of a Serial Interface Engine (SIE), USB transceiver (including matching resistors and configurable pull-up resistors), 1 KB FIFO block, and clock recovery mechanism for crystal-less operation. No external components are required. The USB0 module is Universal Serial Bus Specification 2.0 compliant.

The USB0 module includes the following features:

- Full and Low Speed functionality.
- Implements 4 bidirectional endpoints.
- USB 2.0 compliant USB peripheral support (no host capability).
- Direct module access to 1 KB of RAM for FIFO memory.
- Clock recovery to meet USB clocking requirements with no external components.

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Three byte FIFO on receive.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to SYSCLK / 2 in master mode and SYSCLK / 10 in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock clock rate generator.
- Support for multiple masters on the same data lines.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 48 MHz[2]	—	12	14	mA
		F_{SYSCLK} = 24 MHz[2]	—	7	8	mA
		F_{SYSCLK} = 80 kHz[3]	—	280	—	µA
Idle Mode—Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 48 MHz[2]	—	6.5	8	mA
		F_{SYSCLK} = 24 MHz[2]	—	3.5	5	mA
		F_{SYSCLK} = 80 kHz[3]	—	220	—	µA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off. Regulators in low-power mode.	I_{DD}	LFO Running	—	105	—	µA
		LFO Stopped	—	100	—	µA
Stop Mode—Core halted and all clocks stopped, Regulators in low-power mode, Supply monitor off.	I_{DD}		—	100	—	µA
Shutdown Mode—Core halted and all clocks stopped,Regulators Off, Supply monitor off.	I_{DD}		—	0.25	—	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 48 MHz, T_A = 25 °C	—	900	—	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	5	—	µA
ADC0 Supply Current	I_{ADC}	Operating at 500 ksps V_{DD} = 3.0 V	—	750	1000	µA
On-chip Precision Reference	I_{VREFP}		—	75	—	µA
Temperature Sensor	I_{TSENSE}		—	35	—	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	1	—	µA
		CPMD = 10	—	4	—	µA
		CPMD = 01	—	10	—	µA
		CPMD = 00	—	20	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	50	µA
Regulator Bias Currents	I_{VREG}	Both Regulators in Normal Mode	—	200	—	µA
		Both Regulators in Low Power Mode	—	100	—	µA
		5 V Regulator Off, Internal LDO in Low Power Mode	—	150	—	µA
USB (USB0) Full-Speed	I_{USB}	Active	—	8	—	mA

4.1.8 ADC

Table 4.8. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}			10		Bits
Throughput Rate	f_S		—	—	500	ksps
Tracking Time	t_{TRK}		300	—	—	ns
SAR Clock Frequency	f_{SAR}		—	—	8.33	MHz
Conversion Time	t_{CNV}	10-Bit Conversion,	13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}		—	30	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Single-Ended (AIN+ - GND)	0	—	V_{REF}	V
		Differential (AIN+ - AIN-)	$-V_{REF}$	—	V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance, VREF = 2.4 V						
Integral Nonlinearity	INL		—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Offset Error	E_{OFF}		-2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.005	—	LSB/°C
Slope Error	E_M		—	-0.2	±0.5	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, VREF = 2.4 V						
Signal-to-Noise	SNR		55	58	—	dB
Signal-to-Noise Plus Distortion	SNDR		55	58	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD		—	-73	—	dB
Spurious-Free Dynamic Range	SFDR		—	78	—	dB

Note:
1. Absolute input pin voltage is limited by the VDD and GND supply pins.

4.1.11 5 V Voltage Regulator

Table 4.11. 5V Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range[1]	V_{REGIN}		2.7	—	5.25	V
Output Voltage on VDD[2]	V_{REGOUT}	Output Current = 1 to 100 mA	3.0	3.3	3.6	V
Output Current[2]	I_{REGOUT}		—	—	100	mA

Note:
1. Input range specified for regulation. When an external regulator is used, VREGIN should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	250	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.05	—	µs
		-100 mV Differential	—	5.2	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (bus-powered). The VBUS signal is used to detect when USB is connected to a host device.

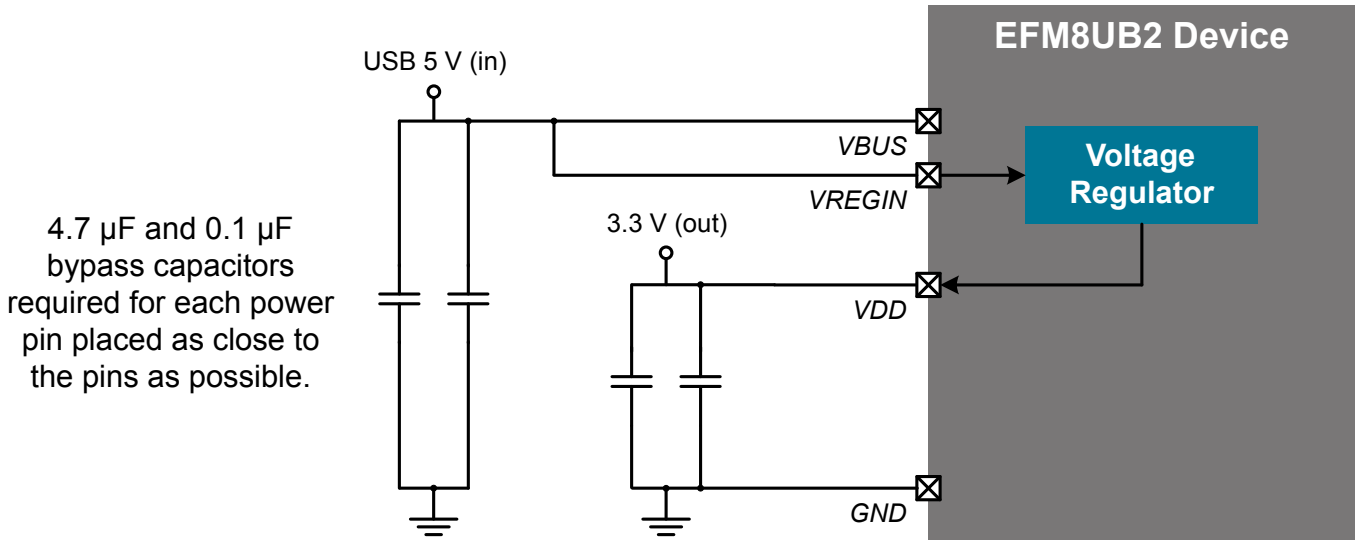

Figure 5.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (self-powered). The VBUS signal is used to detect when USB is connected to a host device and is shown with a resistor divider. This resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification for self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V.

Table 6.1. Pin Definitions for EFM8UB2x-QFP48

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.5	Multifunction I/O	Yes	UART0_RX INT0.5 INT1.5	
2	P0.4	Multifunction I/O	Yes	UART0_TX INT0.4 INT1.4	ADC0P.18 ADC0N.18 CMP0N.4
3	P0.3	Multifunction I/O	Yes	INT0.3 INT1.3	ADC0P.17 ADC0N.17 CMP0P.4
4	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
5	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	
6	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	
7	GND	Ground			
8	D+	USB Data Positive			
9	D-	USB Data Negative			
10	VDD	Supply Power Input / 5V Regulator Output			
11	VREGIN	5V Regulator Input			
12	VBUS	USB VBUS Sense Input		VBUS	
13	RST / C2CK	Active-low Reset / C2 Debug Clock			
14	C2D	C2 Debug Data			
15	P4.7	Multifunction I/O		EMIF_D7 EMIF_AD7m	ADC0P.34 ADC0N.34
16	P4.6	Multifunction I/O		EMIF_D6 EMIF_AD6m	ADC0P.15 ADC0N.15 CMP1N.3
17	P4.5	Multifunction I/O		EMIF_D5 EMIF_AD5m	ADC0P.14 ADC0N.14 CMP1P.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P4.4	Multifunction I/O		EMIF_D4 EMIF_AD4m	ADC0P.13 ADC0N.13 CMP0N.3
19	P4.3	Multifunction I/O		EMIF_D3 EMIF_AD3m	ADC0P.12 ADC0N.12 CMP0P.3
20	P4.2	Multifunction I/O		EMIF_D2 EMIF_AD2m	ADC0P.33 ADC0N.33
21	P4.1	Multifunction I/O		EMIF_D1 EMIF_AD1m	ADC0P.32 ADC0N.32
22	P4.0	Multifunction I/O		EMIF_D0 EMIF_AD0m	ADC0P.11 ADC0N.11 CMP1N.2
23	P3.7	Multifunction I/O	Yes	EMIF_A7 EMIF_A15m	ADC0P.10 ADC0N.10 CMP1P.2
24	P3.6	Multifunction I/O	Yes	EMIF_A6 EMIF_A14m	ADC0P.29 ADC0N.29
25	P3.5	Multifunction I/O	Yes	EMIF_A5 EMIF_A13m	ADC0P.9 ADC0N.9 CMP0N.2
26	P3.4	Multifunction I/O	Yes	EMIF_A4 EMIF_A12m	ADC0P.8 ADC0N.8 CMP0P.2
27	P3.3	Multifunction I/O	Yes	EMIF_A3 EMIF_A11m	ADC0P.28 ADC0N.28
28	P3.2	Multifunction I/O	Yes	EMIF_A2 EMIF_A10m	ADC0P.27 ADC0N.27
29	P3.1	Multifunction I/O	Yes	EMIF_A1 EMIF_A9m	ADC0P.7 ADC0N.7 CMP1N.1
30	P3.0	Multifunction I/O	Yes	EMIF_A0 EMIF_A8m	ADC0P.6 ADC0N.6 CMP1P.1
31	P2.7	Multifunction I/O	Yes	EMIF_A15	ADC0P.26 ADC0N.26

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
32	P2.6	Multifunction I/O	Yes	EMIF_A14	ADC0P.5 ADC0N.5 CMP0N.1
33	P2.5	Multifunction I/O	Yes	EMIF_A13	ADC0P.4 ADC0N.4 CMP0P.1
34	P2.4	Multifunction I/O	Yes	EMIF_A12	ADC0P.25 ADC0N.25
35	P2.3	Multifunction I/O	Yes	EMIF_A11	ADC0P.3 ADC0N.3 CMP1N.0
36	P2.2	Multifunction I/O	Yes	EMIF_A10	ADC0P.2 ADC0N.2 CMP1P.0
37	P2.1	Multifunction I/O	Yes	EMIF_A9	ADC0P.1 ADC0N.1 CMP0N.0
38	P2.0	Multifunction I/O	Yes	EMIF_A8	ADC0P.0 ADC0N.0 CMP0P.0
39	P1.7	Multifunction I/O	Yes	EMIF_WRb	ADC0P.24 ADC0N.24
40	P1.6	Multifunction I/O	Yes	EMIF_RDb	ADC0P.23 ADC0N.23
41	P1.5	Multifunction I/O	Yes		VREF
42	P1.4	Multifunction I/O	Yes	CNVSTR	
43	P1.3	Multifunction I/O	Yes	EMIF_ALEm	ADC0P.22 ADC0N.22
44	P1.2	Multifunction I/O	Yes		ADC0P.20 ADC0N.20 CMP1N.4
45	P1.1	Multifunction I/O	Yes		ADC0P.19 ADC0N.19 CMP1P.4
46	P1.0	Multifunction I/O	Yes		ADC0P.21 ADC0N.21

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
47	P0.7	Multifunction I/O	Yes	XTAL2 EXTCLK INT0.7 INT1.7	
48	P0.6	Multifunction I/O	Yes	XTAL1 INT0.6 INT1.6	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
5	D-	USB Data Negative			
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	VBUS	USB VBUS Sense Input		VBUS	
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		ADC0P.16 ADC0N.16
11	P2.7	Multifunction I/O	Yes		ADC0P.15 ADC0N.15
12	P2.6	Multifunction I/O	Yes		ADC0P.14 ADC0N.14
13	P2.5	Multifunction I/O	Yes		ADC0P.13 ADC0N.13 CMP0N.3
14	P2.4	Multifunction I/O	Yes		ADC0P.12 ADC0N.12 CMP0P.3
15	P2.3	Multifunction I/O	Yes		ADC0P.11 ADC0N.11 CMP1N.2
16	P2.2	Multifunction I/O	Yes		ADC0P.10 ADC0N.10 CMP1P.2
17	P2.1	Multifunction I/O	Yes		ADC0P.9 ADC0N.9 CMP0N.2
18	P2.0	Multifunction I/O	Yes		ADC0P.8 ADC0N.8 CMP0P.2
19	P1.7	Multifunction I/O	Yes		ADC0P.7 ADC0N.7 CMP1N.1

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
20	P1.6	Multifunction I/O	Yes		ADC0P.6 ADC0N.6 CMP1P.1
21	P1.5	Multifunction I/O	Yes		ADC0P.5 ADC0N.5 CMP0N.1
22	P1.4	Multifunction I/O	Yes		ADC0P.4 ADC0N.4 CMP0P.1
23	P1.3	Multifunction I/O	Yes		ADC0P.3 ADC0N.3 CMP1N.0
24	P1.2	Multifunction I/O	Yes		ADC0P.2 ADC0N.2 CMP1P.0
25	P1.1	Multifunction I/O	Yes		ADC0P.1 ADC0N.1 CMP0N.0
26	P1.0	Multifunction I/O	Yes		ADC0P.0 ADC0N.0 CMP0P.0
27	P0.7	Multifunction I/O	Yes	INT0.7 INT1.7	VREF
28	P0.6	Multifunction I/O	Yes	CNVSTR INT0.6 INT1.6	
29	P0.5	Multifunction I/O	Yes	INT0.5 INT1.5 UART0_RX	ADC0P.20 ADC0N.20 CMP1N.4
30	P0.4	Multifunction I/O	Yes	INT0.4 INT1.4 UART0_TX	ADC0P.19 ADC0N.19 CMP1P.4
31	P0.3	Multifunction I/O	Yes	EXTCLK INT0.3 INT1.3	

7. QFP48 Package Specifications

7.1 QFP48 Package Dimensions

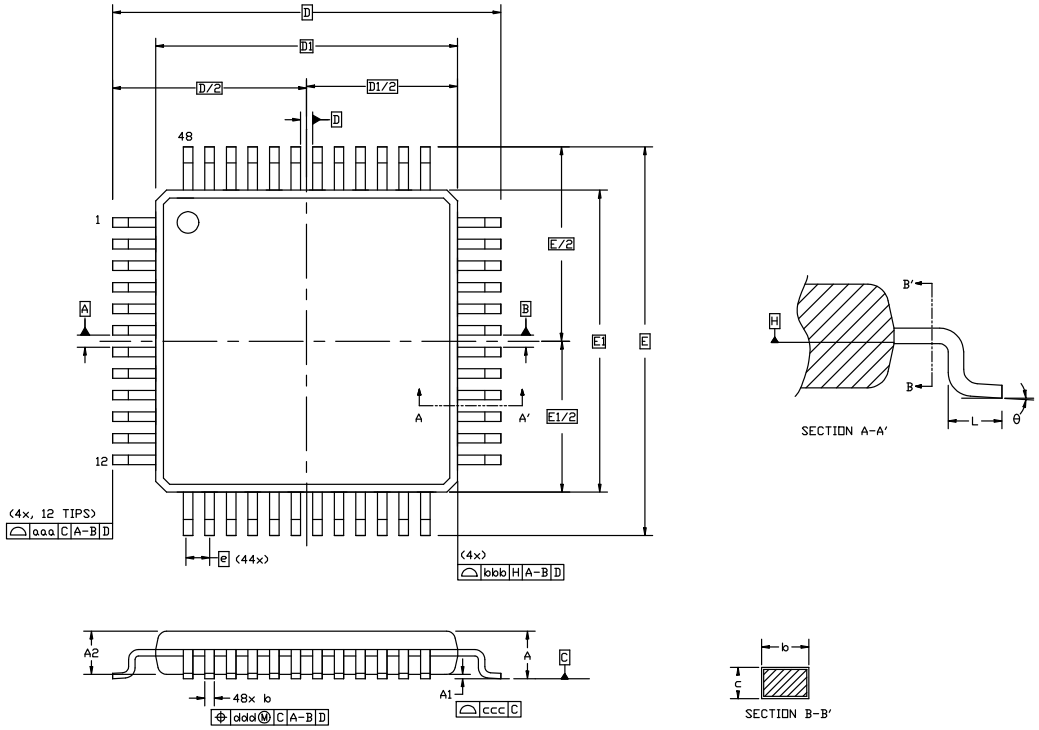

Figure 7.1. QFP48 Package Drawing

Table 7.1. QFP48 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D		9.00 BSC	
D1		7.00 BSC	
e		0.50 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
aaa		0.20	
bbb		0.20	

Dimension	Min	Typ	Max
bbb		0.20	
ccc		0.10	
ddd		0.20	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.2 QFP32 PCB Land Pattern

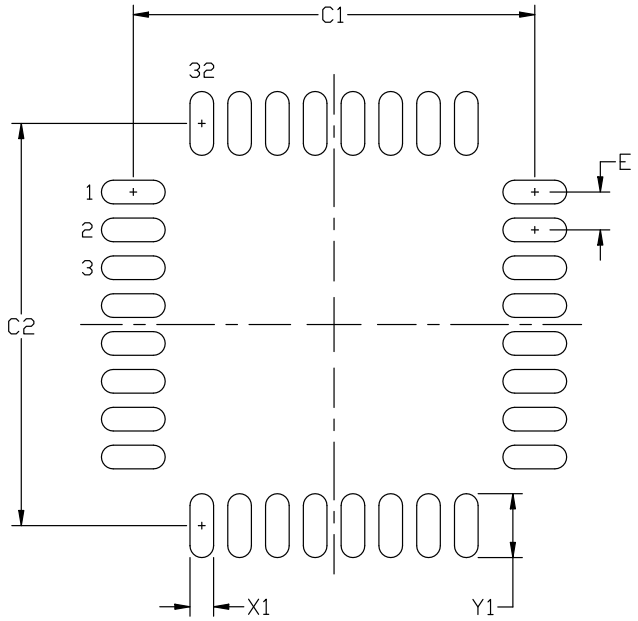

Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.3 QFP32 Package Marking

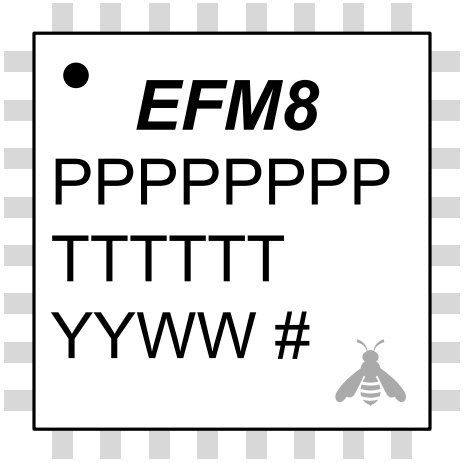

Figure 8.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9.3 QFN32 Package Marking

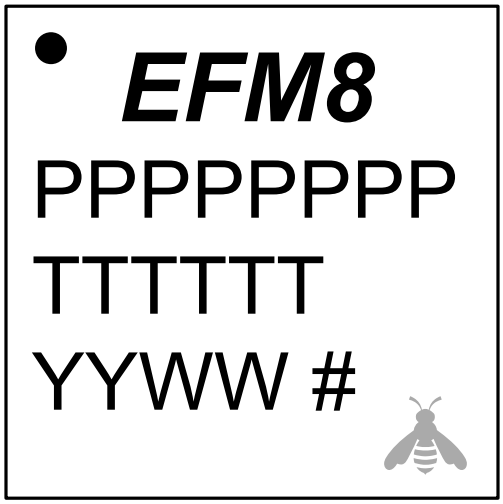

Figure 9.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. Revision History

10.1 Revision 1.3

Updated ordering part numbers to revision B.

Added Power-On Reset Threshold and Reset Delay from POR specifications to 4.1.3 Reset and Supply Monitor.

Added CRC Calculation Time specification to 4.1.4 Flash Memory.

Added VBUS Detection Input High Voltage and VBUS Detection Input Low Voltage specifications to Table 4.14 USB Transceiver on page 20.

Added specifications for 4.1.15 SMBus.

Added 5.4 Debug.

Added information about bootloader implementation and bootloader pinout to 3.10 Bootloader.

Added notes to Table 6.3 Pin Definitions for EFM8UB2x-QFN32 on page 37 and Table 6.2 Pin Definitions for EFM8UB2x-QFP32 on page 33 to clarify that XTAL1 and XTAL2 are not available on the 32-pin packages.

Updated Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 and Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 to recommend 4.7 µF capacitors instead of 1.0 µF capacitors.

Added text and Figure 5.3 Connection Diagram with Voltage Regulator Not Used on page 25 to demonstrate the proper connections when the regulator is not used.

Added reference to the Reference Manual in 3.1 Introduction.

10.2 Revision 1.2

Updated the VDD Ramp Time specification in Table 4.3 Reset and Supply Monitor on page 13 to a maximum of 1 ms.

10.3 Revision 1.1

Initial release.