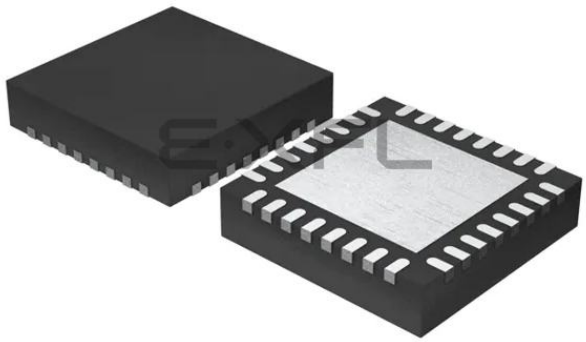

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f32g-b-qfn32

1. Feature List

The EFM8UB2 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 48 MHz maximum operating frequency
- Memory:
  - Up to 64 KB flash memory, in-system re-programmable from firmware.
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Internal 5-to-3.3 V LDO allows direct connection to USB supply net
  - Power-on reset circuit and brownout detectors
- I/O: Up to 40 total multifunction I/O pins:
  - Flexible peripheral crossbar for peripheral routing
  - 10 mA source, 25 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 48 MHz precision oscillator (±1.5% accuracy without USB clock recovery, ±0.25% accuracy with USB clock recovery)
  - Internal 80 kHz low-frequency oscillator
  - External crystal, RC, C, and CMOS clock options
- Timers/Counters and PWM:
  - 5-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes with watchdog timer function
  - 6 x 16-bit general-purpose timers
- Communications and Digital Peripherals:
  - Universal Serial Bus (USB) Function Controller with eight flexible endpoint pipes, integrated transceiver, and 1 KB FIFO RAM
  - 2 x UART
  - SPI™ Master / Slave
  - 2 x SMBus™/I2C™ Master / Slave
  - External Memory Interface (EMIF)
- Analog:
  - 10-Bit Analog-to-Digital Converter (ADC0)
  - 2 x Low-current analog comparators
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded USB bootloader
- Temperature range -40 to 85 ºC
- Single power supply 2.65 to 3.6 V
- QFP48, QFP32, and QFN32 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.65 to 3.6 V operation and is available in 32-pin QFN, 32-pin QFP, or 48-pin QFP packages. All package options are lead-free and RoHS compliant.

2. Ordering Information

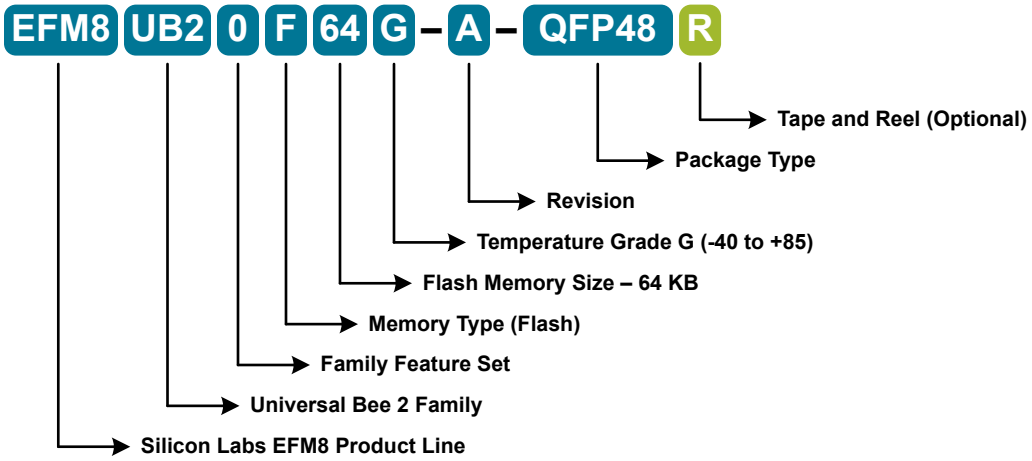


Figure 2.1. EFM8UB2 Part Numbering

All EFM8UB2 family members have the following features:

- CIP-51 Core running up to 48 MHz
- Two Internal Oscillators (48 MHz and 80 kHz)
- USB Full/Low speed Function Controller
- 5 V-In, 3.3 V-Out Regulator
- 2 SMBus/I2C Interfaces
- SPI
- 2 UARTs
- 5-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 6 16-bit Timers
- 2 Analog Comparators
- 10-bit Differential Analog-to-Digital Converter with integrated multiplexer and temperature sensor
- Pre-loaded USB bootloader

In addition to these features, each part number in the EFM8UB2 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Crystal Oscillator	External Memory Interface	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8UB20F64G-B-QFP48	64	4352	40	32	5	5	Yes	Yes	Yes	-40 to +85 °C	QFP48
EFM8UB20F64G-B-QFP32	64	4352	25	20	5	4	—	—	Yes	-40 to +85 °C	QFP32
EFM8UB20F64G-B-QFN32	64	4352	25	20	5	4	—	—	Yes	-40 to +85 °C	QFN32
EFM8UB20F32G-B-QFP48	32	2304	40	32	5	5	Yes	Yes	Yes	-40 to +85 °C	QFP48
EFM8UB20F32G-B-QFP32	32	2304	25	20	5	4	—	—	Yes	-40 to +85 °C	QFP32
EFM8UB20F32G-B-QFN32	32	2304	25	20	5	4	—	—	Yes	-40 to +85 °C	QFN32

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and peripheral clocks halted • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 2. Set SUSPEND bit in HFO0CN	USB0 Bus Activity
Stop	• All internal power nets shut down • Pins retain state • Exit on any reset source	Set STOP bit in PCON0	Any reset source
Shutdown	• All internal power nets shut down • 5V regulator remains active (if enabled) • Pins retain state • Exit on pin or power-on reset	1. Set STOPCF bit in REG01CN 2. Set STOP bit in PCON0	• RSTb pin reset • Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P3.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P4.0-P4.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 on some packages.

- Up to 40 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1) available on P0 pins.

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 48 MHz oscillator divided by 4, then divided by 8 (1.5 MHz).

- Provides clock to core and peripherals.
- 48 MHz internal oscillator (HFOSC0), accurate to ±1.5% over supply and temperature corners: accurate to +/- 0.25% when using USB clock recovery.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK) for QFP48 packages.
- External CMOS clock option (EXTCLK) for QFP32 and QFN32 packages.
- Internal oscillator has clock divider with eight settings for flexible clock scaling: 1, 2, 4, or 8.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Up to five independently-configurable channels
- 8- or 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- USB start-of-frame or falling edge of LFOSC0 capture (Timer 2 and Timer 3)

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

3.6 Communications and Other Digital Peripherals

Universal Serial Bus (USB0)

The USB0 module provides Full/Low Speed function for USB peripheral implementations. The USB function controller (USB0) consists of a Serial Interface Engine (SIE), USB transceiver (including matching resistors and configurable pull-up resistors), 1 KB FIFO block, and clock recovery mechanism for crystal-less operation. No external components are required. The USB0 module is Universal Serial Bus Specification 2.0 compliant.

The USB0 module includes the following features:

- Full and Low Speed functionality.
- Implements 4 bidirectional endpoints.
- USB 2.0 compliant USB peripheral support (no host capability).
- Direct module access to 1 KB of RAM for FIFO memory.
- Clock recovery to meet USB clocking requirements with no external components.

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Three byte FIFO on receive.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to SYSCLK / 2 in master mode and SYSCLK / 10 in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock clock rate generator.
- Support for multiple masters on the same data lines.

3.10 Bootloader

All devices come pre-programmed with a USB bootloader. This bootloader resides in the last three pages of code flash, which includes the code security page; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

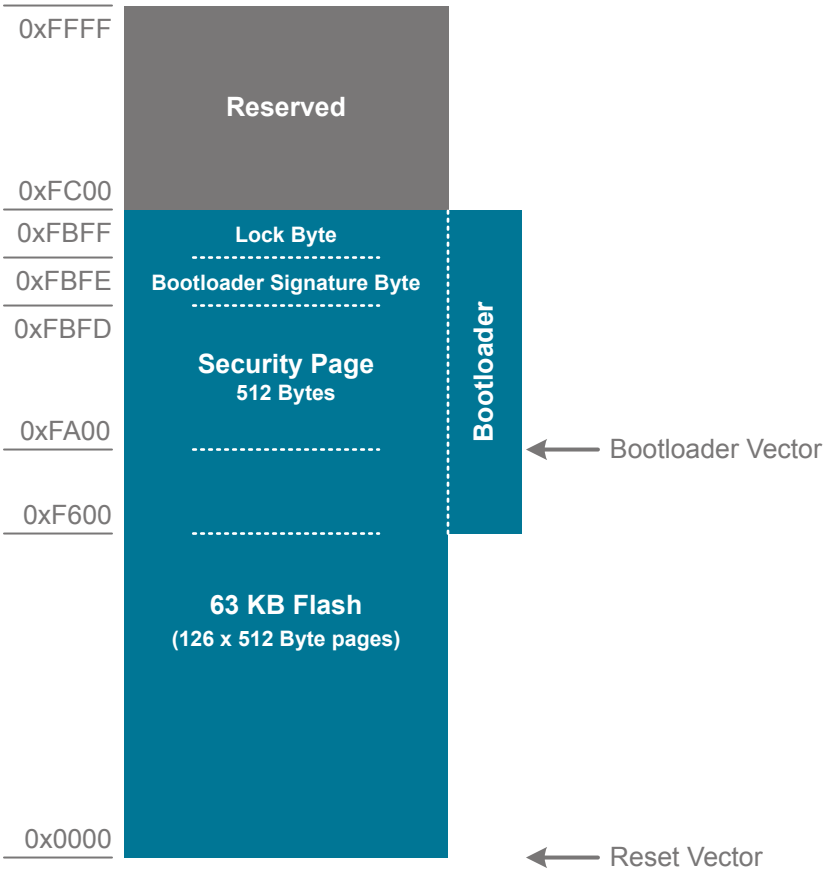


Figure 3.2. Flash Memory Map with Bootloader—64 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5
USB	VBUS
	D+
	D-

4.1.5 Internal Oscillators

Table 4.5. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (48 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	47.3	48	48.7	MHz
Power Supply Sensitivity	PSS_{HFOSC0}	T_A = 25 °C	—	110	—	ppm/V
Temperature Sensitivity	TS_{HFOSC0}	V_{DD} = 3.0 V	—	25	—	ppm/°C
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.0 V	—	65	—	ppm/°C

4.1.6 Crystal Oscillator

Table 4.6. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	—	30	MHz

4.1.7 External Clock Input

Table 4.7. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	48	MHz

4.1.8 ADC

Table 4.8. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}			10		Bits
Throughput Rate	f_S		—	—	500	ksps
Tracking Time	t_{TRK}		300	—	—	ns
SAR Clock Frequency	f_{SAR}		—	—	8.33	MHz
Conversion Time	t_{CNV}	10-Bit Conversion,	13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}		—	30	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Single-Ended (AIN+ - GND)	0	—	V_{REF}	V
		Differential (AIN+ - AIN-)	$-V_{REF}$	—	V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance, VREF = 2.4 V						
Integral Nonlinearity	INL		—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Offset Error	E_{OFF}		-2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.005	—	LSB/°C
Slope Error	E_M		—	-0.2	±0.5	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, VREF = 2.4 V						
Signal-to-Noise	SNR		55	58	—	dB
Signal-to-Noise Plus Distortion	SNDR		55	58	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD		—	-73	—	dB
Spurious-Free Dynamic Range	SFDR		—	78	—	dB

Note:
1. Absolute input pin voltage is limited by the VDD and GND supply pins.

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	250	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.05	—	µs
		-100 mV Differential	—	5.2	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

4.1.14 USB Transceiver

Table 4.14. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VBUS Detection Input Low Voltage	V_{BUS_L}		—	—	1.0	V
VBUS Detection Input High Voltage	V_{BUS_H}		3.0	—	—	V
Transmitter						
Output High Voltage	V_{OH}	V_{DD} ≥3.0V	2.8	—	—	V
Output Low Voltage	V_{OL}	V_{DD} ≥3.0V	—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High	—	38	—	Ω
		Driving Low	—	38	—	
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up)	1.425	1.5	1.575	kΩ
		Low Speed (D- Pull-up)				
Output Rise Time	T_R	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Output Fall Time	T_F	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Receiver						V
Differential Input Sensitivity	V_{DI}	| (D+) - (D-) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Refer to the USB Specification for timing diagrams and symbol definitions.						

4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.18 Absolute Maximum Ratings on page 23 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.18. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VREGIN	V_{REGIN}		GND-0.3	5.8	V
Voltage on I/O, RSTb, or VBUS pins	V_{IN}	V_{DD} > 2.2 V	GND-0.3	5.8	V
		V_{DD} < 2.2 V	GND-0.3	V_{DD}+3.6	V
Total Current Sunk into Supply Pin	I_{VDD}		—	500	mA
Total Current Sourced out of Ground Pin	I_{GND}		500	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I_{IO}		-100	100	mA

Note:
1. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.4 Typical Performance Curves

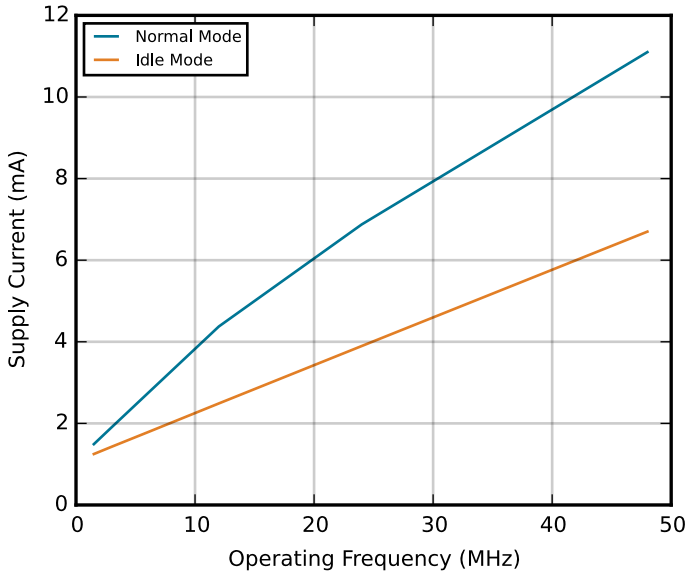


Figure 4.2. Typical Operating Supply Current using HFOSC0

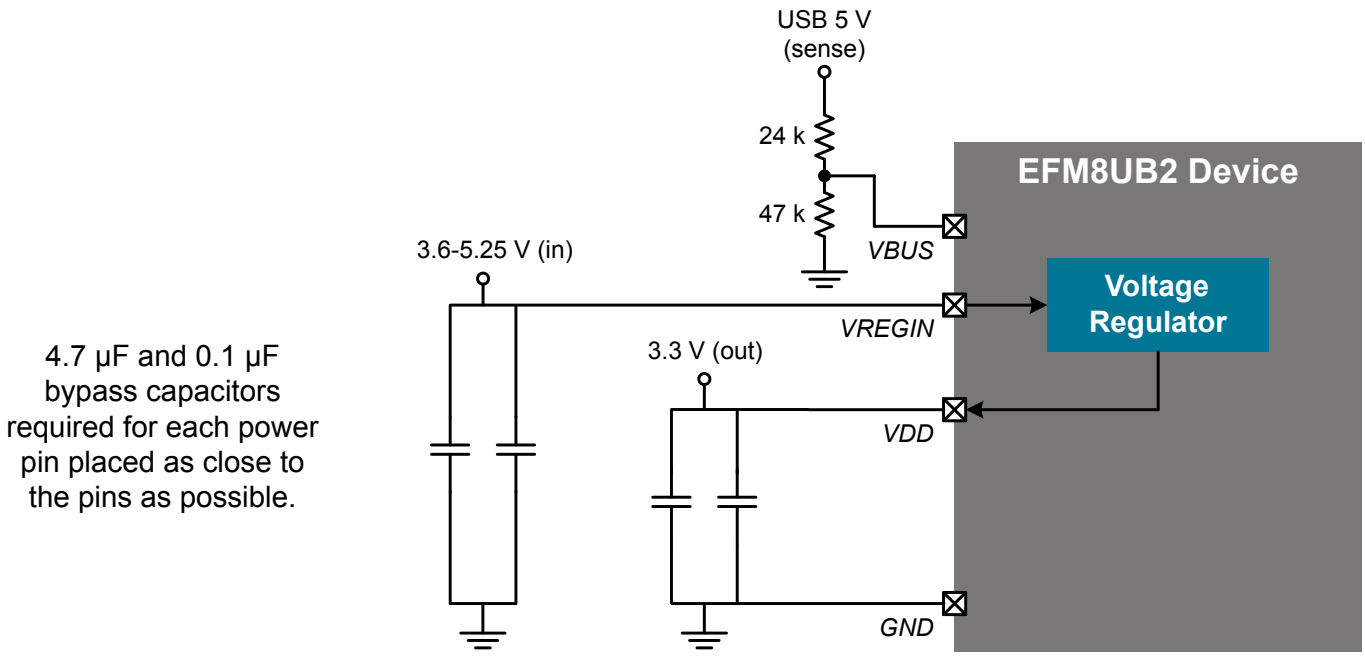


Figure 5.2. Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered)

The figure below shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal 5 V-to-3.3 V regulator is not used.

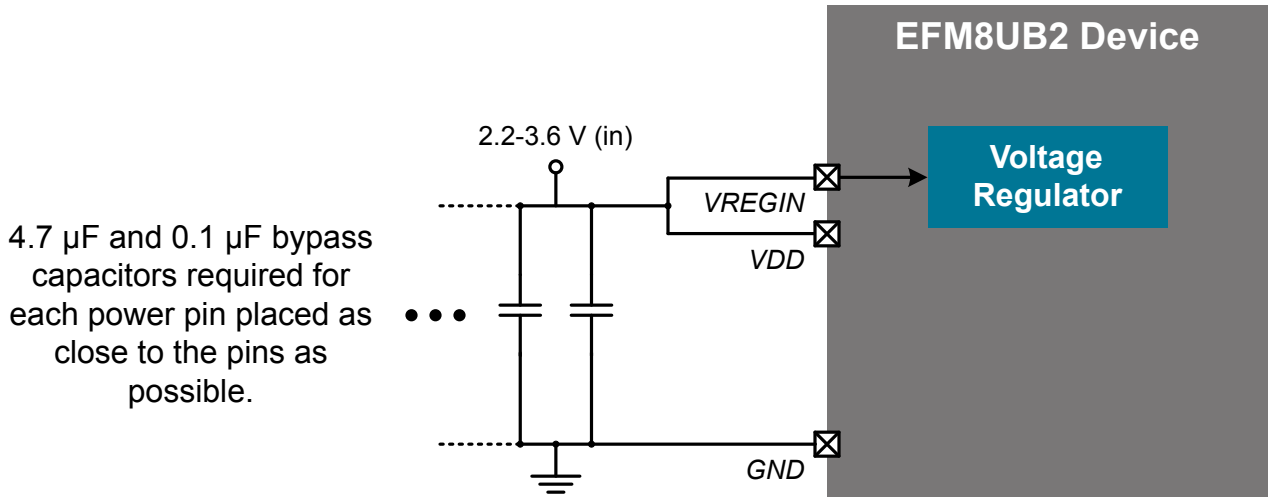


Figure 5.3. Connection Diagram with Voltage Regulator Not Used

Table 6.1. Pin Definitions for EFM8UB2x-QFP48

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.5	Multifunction I/O	Yes	UART0_RX INT0.5 INT1.5	
2	P0.4	Multifunction I/O	Yes	UART0_TX INT0.4 INT1.4	ADC0P.18 ADC0N.18 CMP0N.4
3	P0.3	Multifunction I/O	Yes	INT0.3 INT1.3	ADC0P.17 ADC0N.17 CMP0P.4
4	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
5	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	
6	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	
7	GND	Ground			
8	D+	USB Data Positive			
9	D-	USB Data Negative			
10	VDD	Supply Power Input / 5V Regulator Output			
11	VREGIN	5V Regulator Input			
12	VBUS	USB VBUS Sense Input		VBUS	
13	RST / C2CK	Active-low Reset / C2 Debug Clock			
14	C2D	C2 Debug Data			
15	P4.7	Multifunction I/O		EMIF_D7 EMIF_AD7m	ADC0P.34 ADC0N.34
16	P4.6	Multifunction I/O		EMIF_D6 EMIF_AD6m	ADC0P.15 ADC0N.15 CMP1N.3
17	P4.5	Multifunction I/O		EMIF_D5 EMIF_AD5m	ADC0P.14 ADC0N.14 CMP1P.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
32	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
Note: XTAL1 and XTAL2 are not available on this package. EXTCLK is still available on P0.3.					

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.4	Multifunction I/O	Yes	INT0.4 INT1.4 UART0_TX	ADC0P.19 ADC0N.19 CMP1P.4
31	P0.3	Multifunction I/O	Yes	EXTCLK INT0.3 INT1.3	
32	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
Center	GND	Ground			
Note: XTAL1 and XTAL2 are not available on this package. EXTCLK is still available on P0.3.					

Dimension	Min	Typ	Max
ccc		0.08	
ddd		0.08	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Typ	Max
bbb		0.20	
ccc		0.10	
ddd		0.20	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.3 QFN32 Package Marking

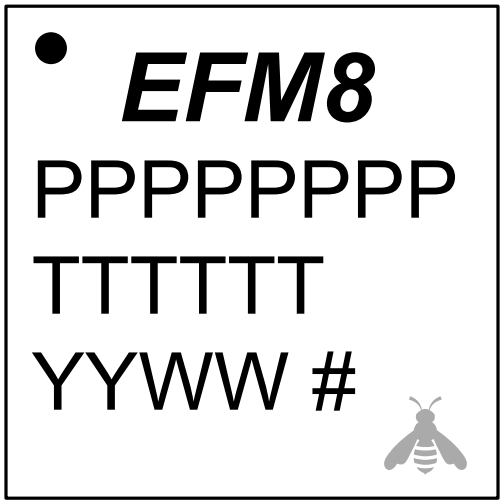


Figure 9.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. Revision History

10.1 Revision 1.3

Updated ordering part numbers to revision B.

Added Power-On Reset Threshold and Reset Delay from POR specifications to 4.1.3 Reset and Supply Monitor.

Added CRC Calculation Time specification to 4.1.4 Flash Memory.

Added VBUS Detection Input High Voltage and VBUS Detection Input Low Voltage specifications to Table 4.14 USB Transceiver on page 20.

Added specifications for 4.1.15 SMBus.

Added 5.4 Debug.

Added information about bootloader implementation and bootloader pinout to 3.10 Bootloader.

Added notes to Table 6.3 Pin Definitions for EFM8UB2x-QFN32 on page 37 and Table 6.2 Pin Definitions for EFM8UB2x-QFP32 on page 33 to clarify that XTAL1 and XTAL2 are not available on the 32-pin packages.

Updated Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 and Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 to recommend 4.7 µF capacitors instead of 1.0 µF capacitors.

Added text and Figure 5.3 Connection Diagram with Voltage Regulator Not Used on page 25 to demonstrate the proper connections when the regulator is not used.

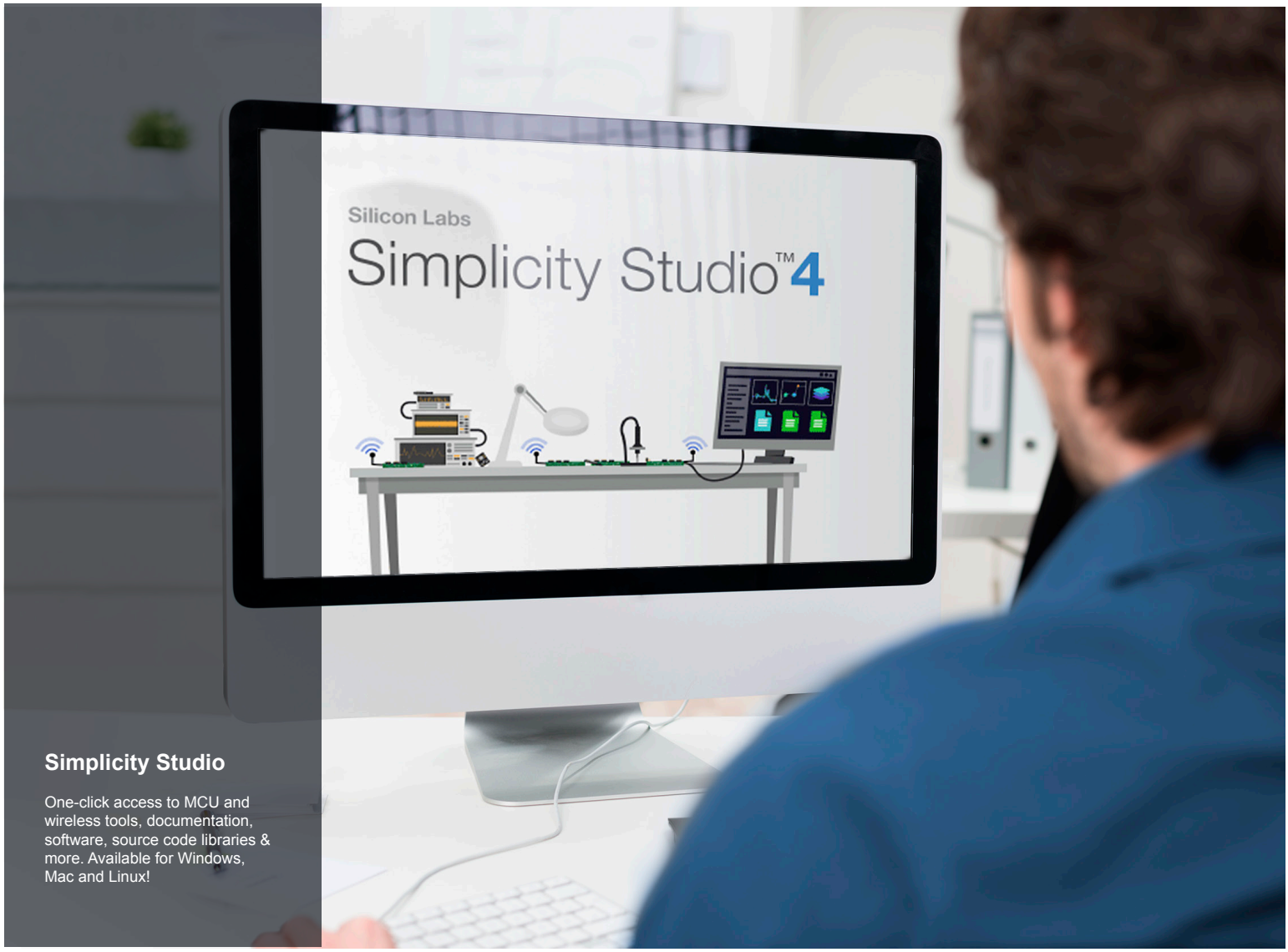
Added reference to the Reference Manual in 3.1 Introduction.

10.2 Revision 1.2

Updated the VDD Ramp Time specification in Table 4.3 Reset and Supply Monitor on page 13 to a maximum of 1 ms.

10.3 Revision 1.1

Initial release.



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