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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	I ² C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f32g-b-qfp32r

1. Feature List

The EFM8UB2 highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 48 MHz maximum operating frequency
- Memory:
 - Up to 64 KB flash memory, in-system re-programmable from firmware.
 - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
 - Internal LDO regulator for CPU core voltage
 - Internal 5-to-3.3 V LDO allows direct connection to USB supply net
 - Power-on reset circuit and brownout detectors
- I/O: Up to 40 total multifunction I/O pins:
 - Flexible peripheral crossbar for peripheral routing
 - 10 mA source, 25 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 48 MHz precision oscillator ($\pm 1.5\%$ accuracy without USB clock recovery, $\pm 0.25\%$ accuracy with USB clock recovery)
 - Internal 80 kHz low-frequency oscillator
 - External crystal, RC, C, and CMOS clock options
- Timers/Counters and PWM:
 - 5-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes with watchdog timer function
 - 6 x 16-bit general-purpose timers
- Communications and Digital Peripherals:
 - Universal Serial Bus (USB) Function Controller with eight flexible endpoint pipes, integrated transceiver, and 1 KB FIFO RAM
 - 2 x UART
 - SPI™ Master / Slave
 - 2 x SMBus™/I2C™ Master / Slave
 - External Memory Interface (EMIF)
- Analog:
 - 10-Bit Analog-to-Digital Converter (ADC0)
 - 2 x Low-current analog comparators
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-loaded USB bootloader
- Temperature range -40 to 85 °C
- Single power supply 2.65 to 3.6 V
- QFP48, QFP32, and QFN32 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.65 to 3.6 V operation and is available in 32-pin QFN, 32-pin QFP, or 48-pin QFP packages. All package options are lead-free and RoHS compliant.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	<ul style="list-style-type: none"> Core halted All peripherals clocked and fully operational Code resumes execution on wake event 	Set IDLE bit in PCON0	Any interrupt
Suspend	<ul style="list-style-type: none"> Core and peripheral clocks halted Code resumes execution on wake event 	<ol style="list-style-type: none"> Switch SYSCLK to HFOSC0 Set SUSPEND bit in HFO0CN 	USB0 Bus Activity
Stop	<ul style="list-style-type: none"> All internal power nets shut down Pins retain state Exit on any reset source 	Set STOP bit in PCON0	Any reset source
Shutdown	<ul style="list-style-type: none"> All internal power nets shut down 5V regulator remains active (if enabled) Pins retain state Exit on pin or power-on reset 	<ol style="list-style-type: none"> Set STOPCF bit in REG01CN Set STOP bit in PCON0 	<ul style="list-style-type: none"> RSTb pin reset Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P3.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P4.0-P4.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 on some packages.

- Up to 40 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1) available on P0 pins.

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 48 MHz oscillator divided by 4, then divided by 8 (1.5 MHz).

- Provides clock to core and peripherals.
- 48 MHz internal oscillator (HFOSC0), accurate to $\pm 1.5\%$ over supply and temperature corners: accurate to $\pm 0.25\%$ when using USB clock recovery.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK) for QFP48 packages.
- External CMOS clock option (EXTCLK) for QFP32 and QFN32 packages.
- Internal oscillator has clock divider with eight settings for flexible clock scaling: 1, 2, 4, or 8.

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN48	P3.7
QFP32	P3.0 / C2D
QFN32	P3.0 / C2D

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 11](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.7 ²	3.3	3.6	V
Operating Supply Voltage on VREGIN	V _{REGIN}		2.7	—	5.25	V
System Clock Frequency	f _{SYSCLK}		0	—	48	MHz
Operating Ambient Temperature	T _A		-40	—	85	°C

Note:

1. All voltages with respect to GND
2. The USB specification requires 3.0 V minimum supply voltage.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode—Full speed with code executing from flash	I _{DD}	F _{SYSCLK} = 48 MHz ²	—	12	14	mA
		F _{SYSCLK} = 24 MHz ²	—	7	8	mA
		F _{SYSCLK} = 80 kHz ³	—	280	—	μA
Idle Mode—Core halted with peripherals running	I _{DD}	F _{SYSCLK} = 48 MHz ²	—	6.5	8	mA
		F _{SYSCLK} = 24 MHz ²	—	3.5	5	mA
		F _{SYSCLK} = 80 kHz ³	—	220	—	μA
Suspend Mode—Core halted and high frequency clocks stopped, Supply monitor off. Regulators in low-power mode.	I _{DD}	LFO Running	—	105	—	μA
		LFO Stopped	—	100	—	μA
Stop Mode—Core halted and all clocks stopped, Regulators in low-power mode, Supply monitor off.	I _{DD}		—	100	—	μA
Shutdown Mode—Core halted and all clocks stopped, Regulators Off, Supply monitor off.	I _{DD}		—	0.25	—	μA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I _{HFOSC0}	Operating at 48 MHz, T _A = 25 °C	—	900	—	μA
Low-Frequency Oscillator	I _{LFOSC}	Operating at 80 kHz, T _A = 25 °C	—	5	—	μA
ADC0 Supply Current	I _{ADC}	Operating at 500 ksps V _{DD} = 3.0 V	—	750	1000	μA
On-chip Precision Reference	I _{VREFP}		—	75	—	μA
Temperature Sensor	I _{TSENSE}		—	35	—	μA
Comparator 0 (CMP0, CMP1)	I _{CMP}	CPMD = 11	—	1	—	μA
		CPMD = 10	—	4	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	20	—	μA
Voltage Supply Monitor (VMON0)	I _{VMON}		—	15	50	μA
Regulator Bias Currents	I _{VREG}	Both Regulators in Normal Mode	—	200	—	μA
		Both Regulators in Low Power Mode	—	100	—	μA
		5 V Regulator Off, Internal LDO in Low Power Mode	—	150	—	μA
USB (USB0) Full-Speed	I _{USB}	Active	—	8	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: <ol style="list-style-type: none"> 1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount. 2. Includes supply current from regulators, supply monitor, and High Frequency Oscillator. 3. Includes supply current from regulators, supply monitor, and Low Frequency Oscillator. 						

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		2.60	2.65	2.70	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to $V_{DD} > 2.7$ V	—	—	1	ms
Reset Delay from POR	t_{POR}	Relative to $V_{DD} > V_{POR}$	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	—	250	μ s
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	μ s
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{SYSCLK} > 1$ MHz	80	580	800	μ s
VDD Supply Monitor Turn-On Time	t_{MON}		—	—	100	μ s

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time ¹	t_{WRITE}	One Byte	10	15	20	μ s
Erase Time ¹	t_{ERASE}	One Page	10	15	22.5	ms
V_{DD} Voltage During Programming ²	V_{PROG}		2.7	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		10k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block SYSCLK = 48 MHz	—	5.5	—	μ s
Note: <ol style="list-style-type: none"> 1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles. 2. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}). 3. Data Retention Information is published in the Quarterly Quality and Reliability Report. 						

4.1.14 USB Transceiver

Table 4.14. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VBUS Detection Input Low Voltage	V _{BUS_L}		—	—	1.0	V
VBUS Detection Input High Voltage	V _{BUS_H}		3.0	—	—	V
Transmitter						
Output High Voltage	V _{OH}	V _{DD} ≥3.0V	2.8	—	—	V
Output Low Voltage	V _{OL}	V _{DD} ≥3.0V	—	—	0.8	V
Output Crossover Point	V _{CRS}		1.3	—	2.0	V
Output Impedance	Z _{DRV}	Driving High	—	38	—	Ω
		Driving Low	—	38	—	
Pull-up Resistance	R _{PU}	Full Speed (D+ Pull-up) Low Speed (D- Pull-up)	1.425	1.5	1.575	kΩ
Output Rise Time	T _R	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Output Fall Time	T _F	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Receiver						V
Differential Input Sensitivity	V _{DI}	(D+) - (D-)	0.2	—	—	V
Differential Input Common Mode Range	V _{CM}		0.8	—	2.5	V
Input Leakage Current	I _L	Pullups Disabled	—	<1.0	—	μA
Refer to the USB Specification for timing diagrams and symbol definitions.						

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P4.4	Multifunction I/O		EMIF_D4 EMIF_AD4m	ADC0P.13 ADC0N.13 CMP0N.3
19	P4.3	Multifunction I/O		EMIF_D3 EMIF_AD3m	ADC0P.12 ADC0N.12 CMP0P.3
20	P4.2	Multifunction I/O		EMIF_D2 EMIF_AD2m	ADC0P.33 ADC0N.33
21	P4.1	Multifunction I/O		EMIF_D1 EMIF_AD1m	ADC0P.32 ADC0N.32
22	P4.0	Multifunction I/O		EMIF_D0 EMIF_AD0m	ADC0P.11 ADC0N.11 CMP1N.2
23	P3.7	Multifunction I/O	Yes	EMIF_A7 EMIF_A15m	ADC0P.10 ADC0N.10 CMP1P.2
24	P3.6	Multifunction I/O	Yes	EMIF_A6 EMIF_A14m	ADC0P.29 ADC0N.29
25	P3.5	Multifunction I/O	Yes	EMIF_A5 EMIF_A13m	ADC0P.9 ADC0N.9 CMP0N.2
26	P3.4	Multifunction I/O	Yes	EMIF_A4 EMIF_A12m	ADC0P.8 ADC0N.8 CMP0P.2
27	P3.3	Multifunction I/O	Yes	EMIF_A3 EMIF_A11m	ADC0P.28 ADC0N.28
28	P3.2	Multifunction I/O	Yes	EMIF_A2 EMIF_A10m	ADC0P.27 ADC0N.27
29	P3.1	Multifunction I/O	Yes	EMIF_A1 EMIF_A9m	ADC0P.7 ADC0N.7 CMP1N.1
30	P3.0	Multifunction I/O	Yes	EMIF_A0 EMIF_A8m	ADC0P.6 ADC0N.6 CMP1P.1
31	P2.7	Multifunction I/O	Yes	EMIF_A15	ADC0P.26 ADC0N.26

6.2 EFM8UB2x-QFP32 Pin Definitions

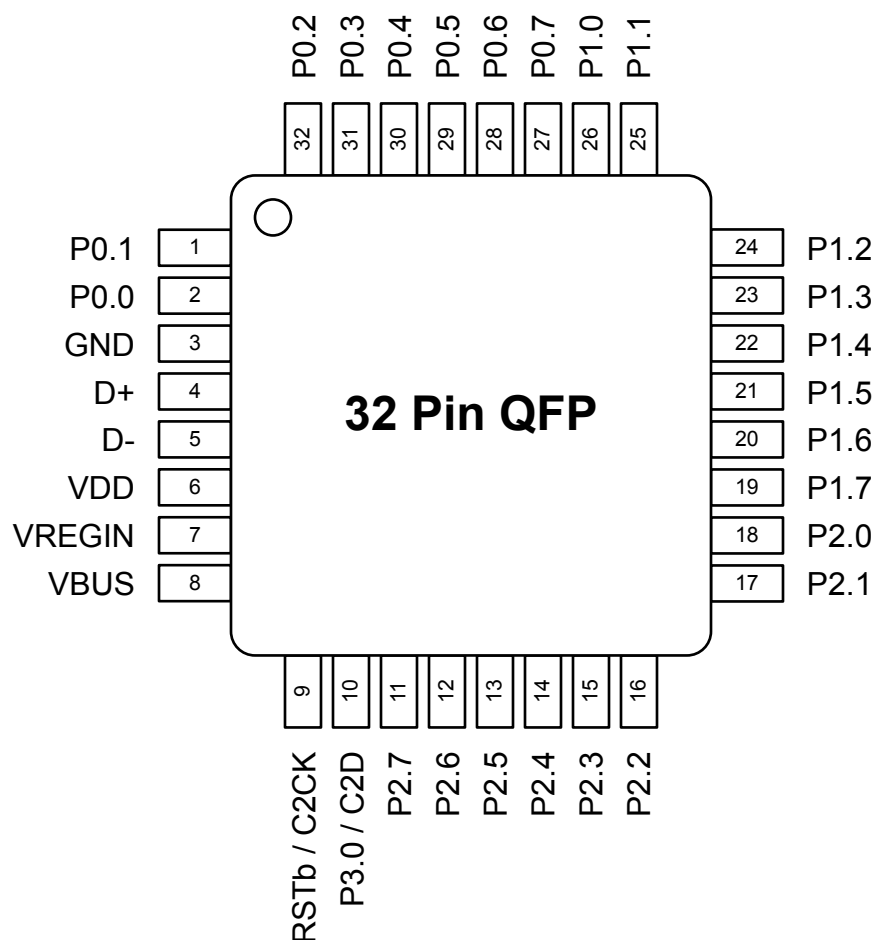


Figure 6.2. EFM8UB2x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8UB2x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	ADC0P.18 ADC0N.18 CMP0N.4
2	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	ADC0P.17 ADC0N.17 CMP0P.4
3	GND	Ground			
4	D+	USB Data Positive			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
5	D-	USB Data Negative			
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	VBUS	USB VBUS Sense Input		VBUS	
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		ADC0P.16 ADC0N.16
11	P2.7	Multifunction I/O	Yes		ADC0P.15 ADC0N.15
12	P2.6	Multifunction I/O	Yes		ADC0P.14 ADC0N.14
13	P2.5	Multifunction I/O	Yes		ADC0P.13 ADC0N.13 CMP0N.3
14	P2.4	Multifunction I/O	Yes		ADC0P.12 ADC0N.12 CMP0P.3
15	P2.3	Multifunction I/O	Yes		ADC0P.11 ADC0N.11 CMP1N.2
16	P2.2	Multifunction I/O	Yes		ADC0P.10 ADC0N.10 CMP1P.2
17	P2.1	Multifunction I/O	Yes		ADC0P.9 ADC0N.9 CMP0N.2
18	P2.0	Multifunction I/O	Yes		ADC0P.8 ADC0N.8 CMP0P.2
19	P1.7	Multifunction I/O	Yes		ADC0P.7 ADC0N.7 CMP1N.1

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
32	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
Note: XTAL1 and XTAL2 are not available on this package. EXTCLK is still available on P0.3.					

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
30	P0.4	Multifunction I/O	Yes	INT0.4 INT1.4 UART0_TX	ADC0P.19 ADC0N.19 CMP1P.4
31	P0.3	Multifunction I/O	Yes	EXTCLK INT0.3 INT1.3	
32	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
Center	GND	Ground			

Note: XTAL1 and XTAL2 are not available on this package. EXTCLK is still available on P0.3.

Dimension	Min	Typ	Max
ccc	0.08		
ddd	0.08		
theta	0°	3.5°	7°
Note: <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to JEDEC outline MS-026, variation ABC. 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components. 			

Dimension	Min	Max
Note: <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 5. The stencil thickness should be 0.125 mm (5 mils). 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 7. A No-Clean, Type-3 solder paste is recommended. 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components. 		

7.3 QFP48 Package Marking

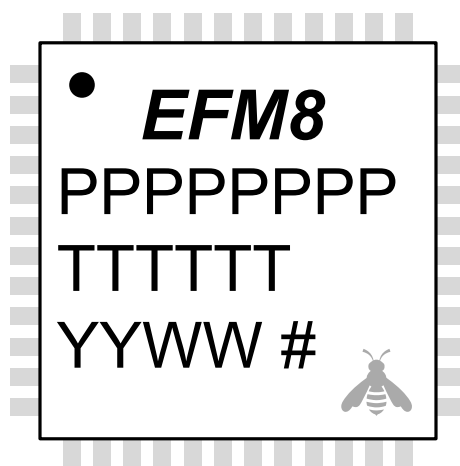


Figure 7.3. QFP48 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

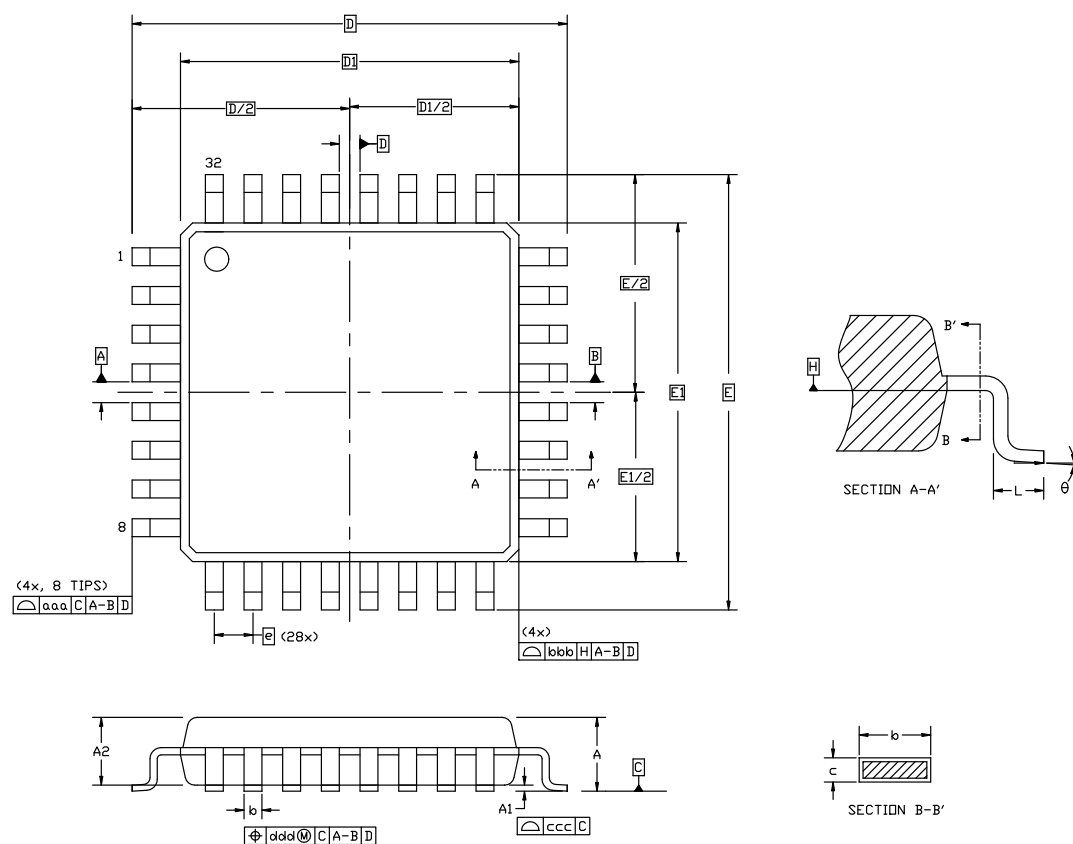


Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
aaa	0.20		

8.2 QFP32 PCB Land Pattern

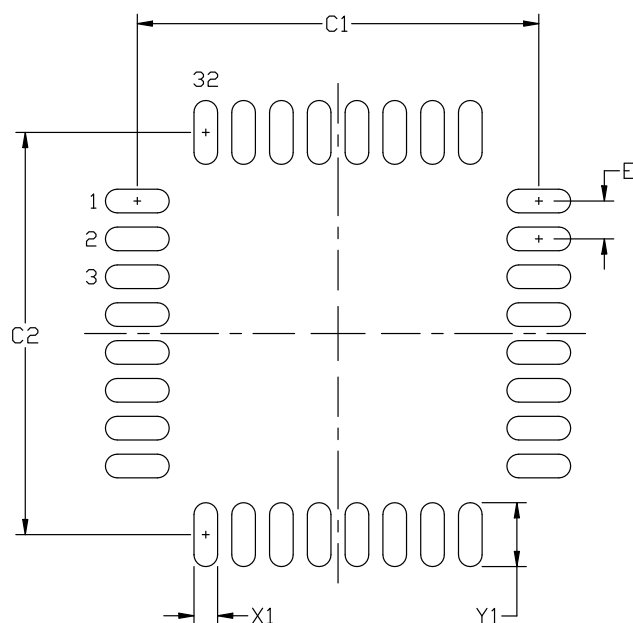


Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Typ	Max
ddd	—	—	0.05
eee	—	—	0.08

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.2 QFN32 PCB Land Pattern

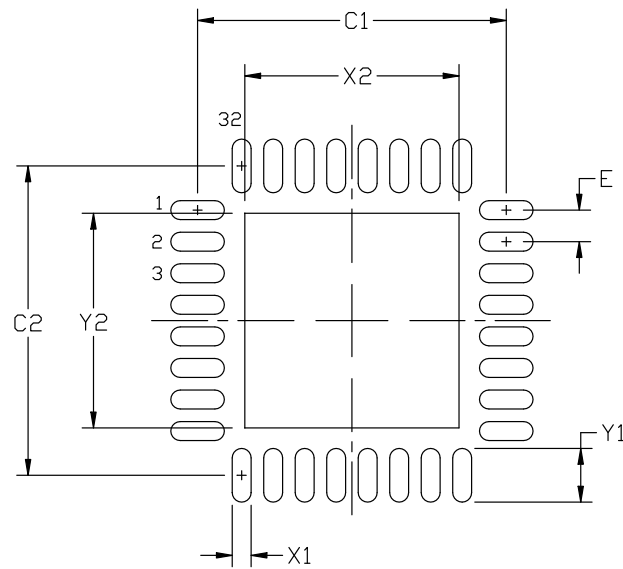


Figure 9.2. QFN32 PCB Land Pattern Drawing

Table 9.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.3 QFN32 Package Marking



Figure 9.3. QFN32 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. Revision History

10.1 Revision 1.3

Updated ordering part numbers to revision B.

Added Power-On Reset Threshold and Reset Delay from POR specifications to [4.1.3 Reset and Supply Monitor](#).

Added CRC Calculation Time specification to [4.1.4 Flash Memory](#).

Added VBUS Detection Input High Voltage and VBUS Detection Input Low Voltage specifications to [Table 4.14 USB Transceiver on page 20](#).

Added specifications for [4.1.15 SMBus](#).

Added [5.4 Debug](#).

Added information about bootloader implementation and bootloader pinout to [3.10 Bootloader](#).

Added notes to [Table 6.3 Pin Definitions for EFM8UB2x-QFN32 on page 37](#) and [Table 6.2 Pin Definitions for EFM8UB2x-QFP32 on page 33](#) to clarify that XTAL1 and XTAL2 are not available on the 32-pin packages.

Updated [Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected \(Bus-Powered\) on page 24](#) and [Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected \(Self-Powered\) on page 25](#) to recommend 4.7 μ F capacitors instead of 1.0 μ F capacitors.

Added text and [Figure 5.3 Connection Diagram with Voltage Regulator Not Used on page 25](#) to demonstrate the proper connections when the regulator is not used.

Added reference to the Reference Manual in [3.1 Introduction](#).

10.2 Revision 1.2

Updated the VDD Ramp Time specification in [Table 4.3 Reset and Supply Monitor on page 13](#) to a maximum of 1 ms.

10.3 Revision 1.1

Initial release.