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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	EBI/EMI, I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f32g-b-qfp48

3.10 Bootloader

All devices come pre-programmed with a USB bootloader. This bootloader resides in the last three pages of code flash, which includes the code security page; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

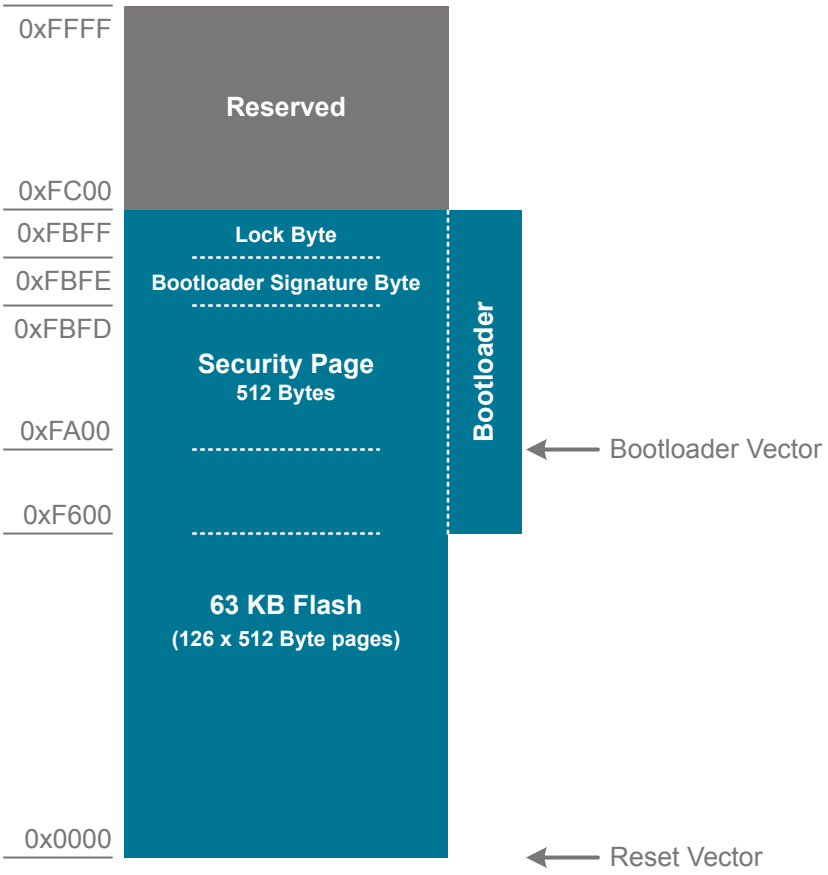

Figure 3.2. Flash Memory Map with Bootloader—64 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5
USB	VBUS
	D+
	D-

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 11, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.7[2]	3.3	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}		2.7	—	5.25	V
System Clock Frequency	f_{SYSCLK}		0	—	48	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. All voltages with respect to GND
2. The USB specification requires 3.0 V minimum supply voltage.

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	250	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.05	—	µs
		-100 mV Differential	—	5.2	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

Table 4.16. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:
1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

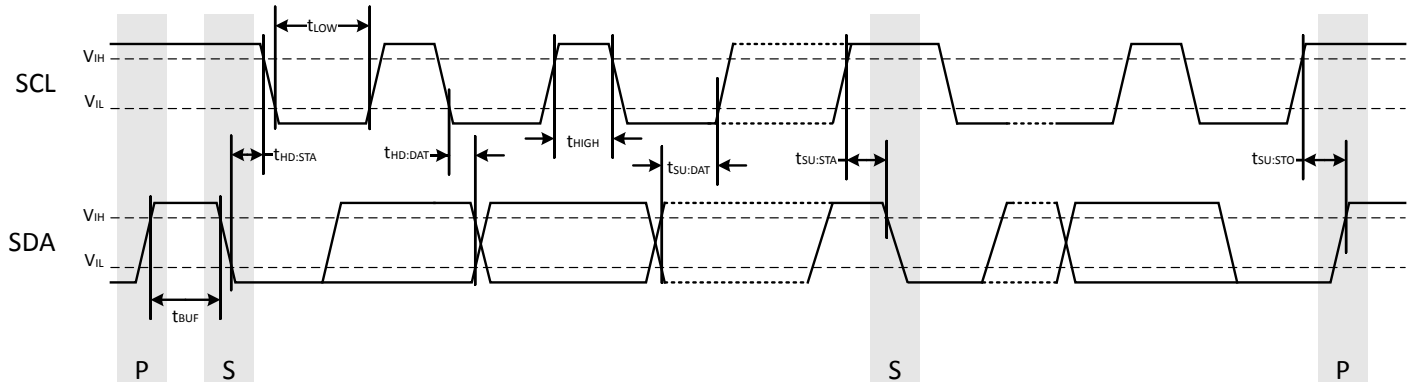

Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.17. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFP48 Packages	—	60	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QFN32 Packages	—	28	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (bus-powered). The VBUS signal is used to detect when USB is connected to a host device.

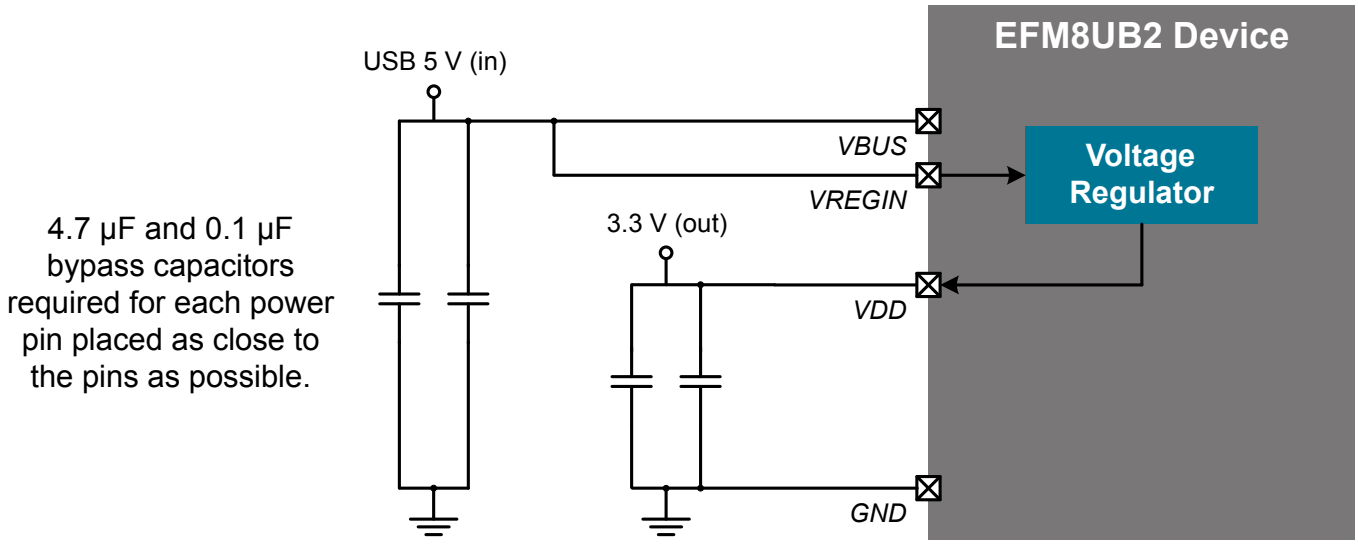

Figure 5.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (self-powered). The VBUS signal is used to detect when USB is connected to a host device and is shown with a resistor divider. This resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification for self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V.

5.2 USB

Figure 5.4 Connection Diagram for USB Pins on page 26 shows a typical connection diagram for the USB pins of the EFM8UB2 devices including ESD protection diodes on the USB pins.

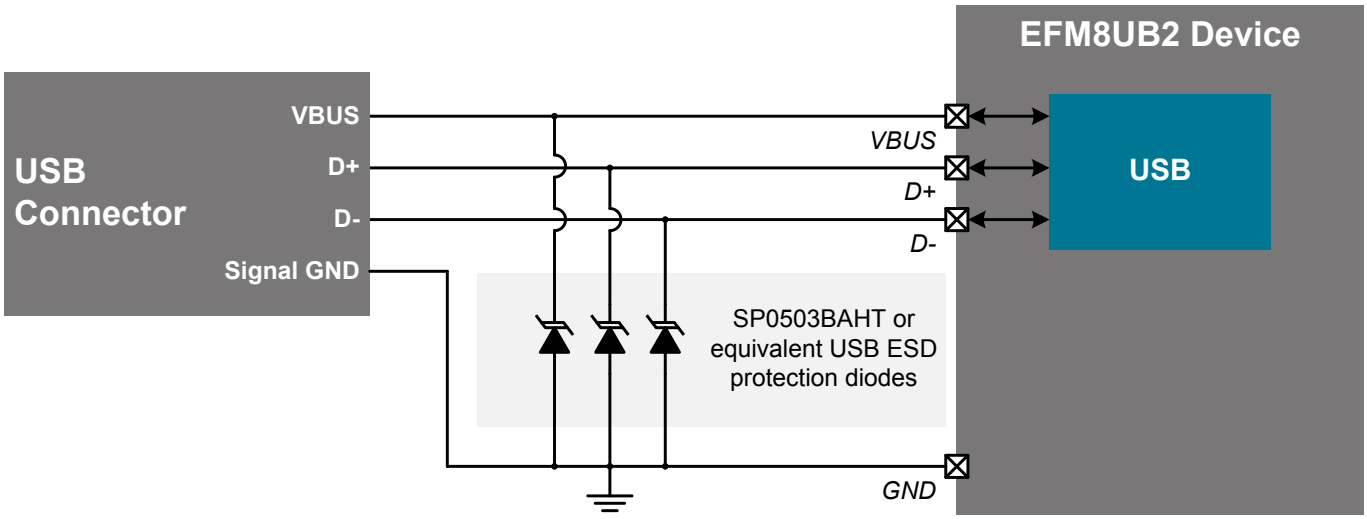

Figure 5.4. Connection Diagram for USB Pins

5.3 Voltage Reference (VREF)

Figure 5.5 Connection Diagram for Internal Voltage Reference on page 26 shows a typical connection diagram for the voltage reference (VREF) pin of the EFM8UB2 devices when using the internal voltage reference. When using an external voltage reference, consult the external reference data sheet for connection recommendations.

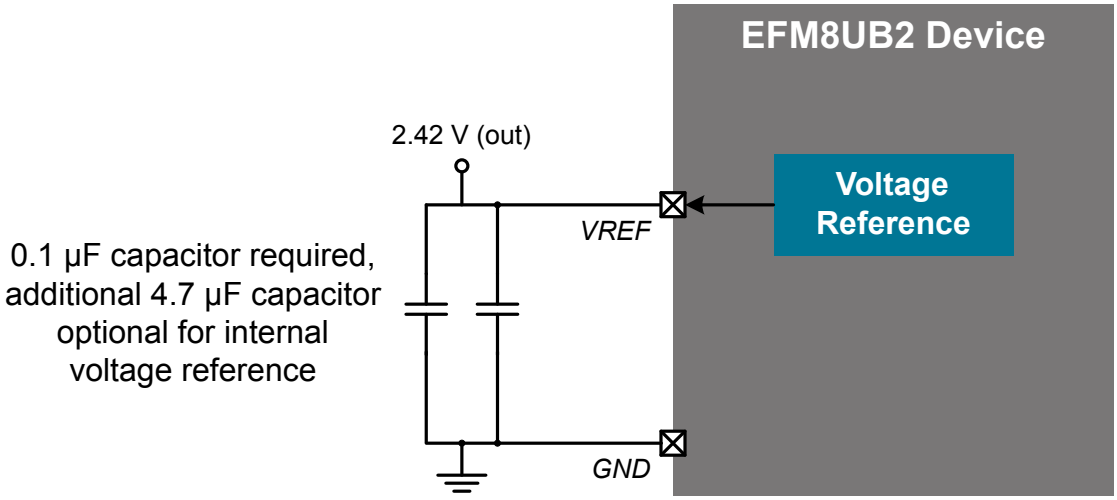

Figure 5.5. Connection Diagram for Internal Voltage Reference

6. Pin Definitions

6.1 EFM8UB2x-QFP48 Pin Definitions

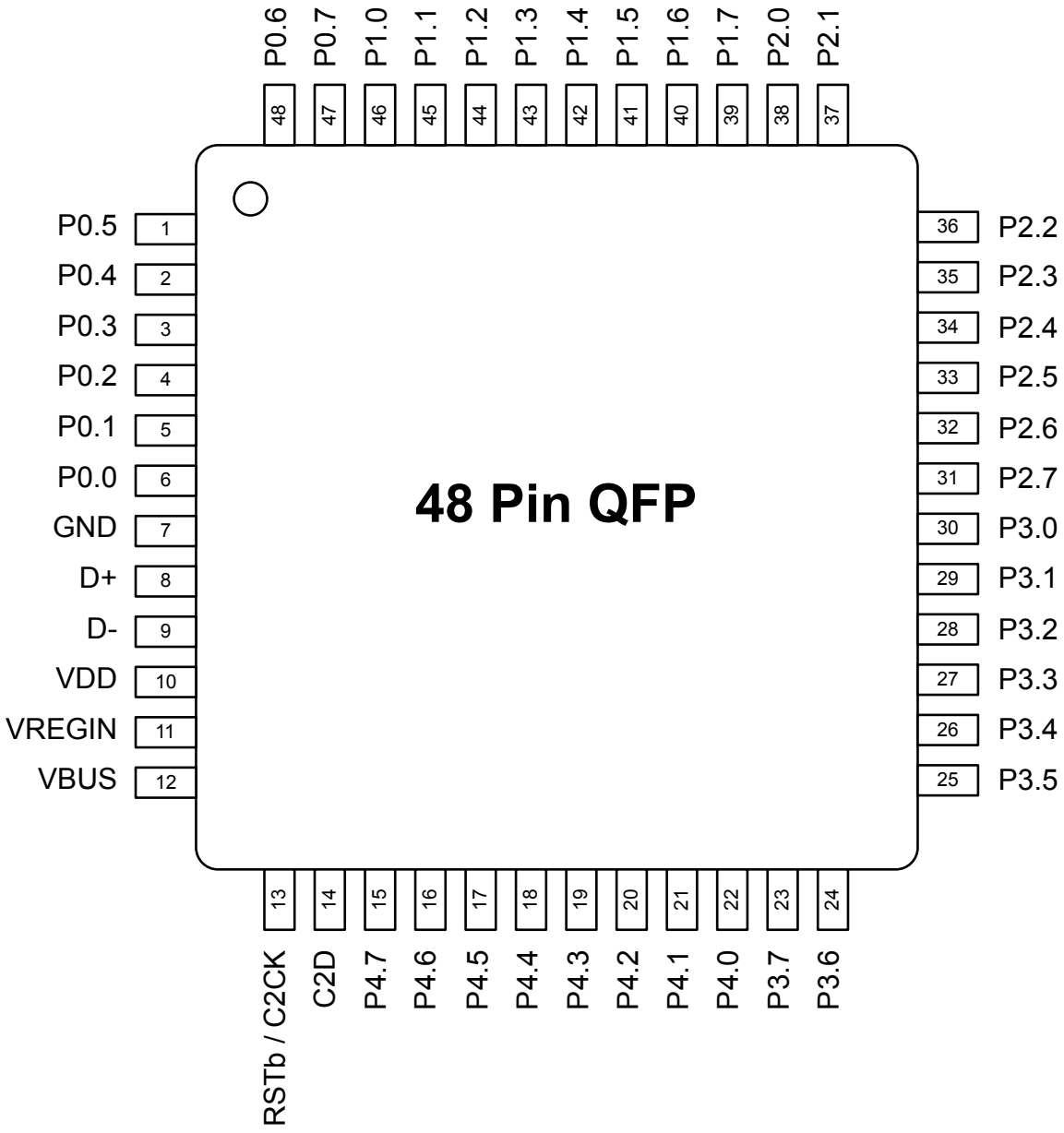

Figure 6.1. EFM8UB2x-QFP48 Pinout

6.2 EFM8UB2x-QFP32 Pin Definitions

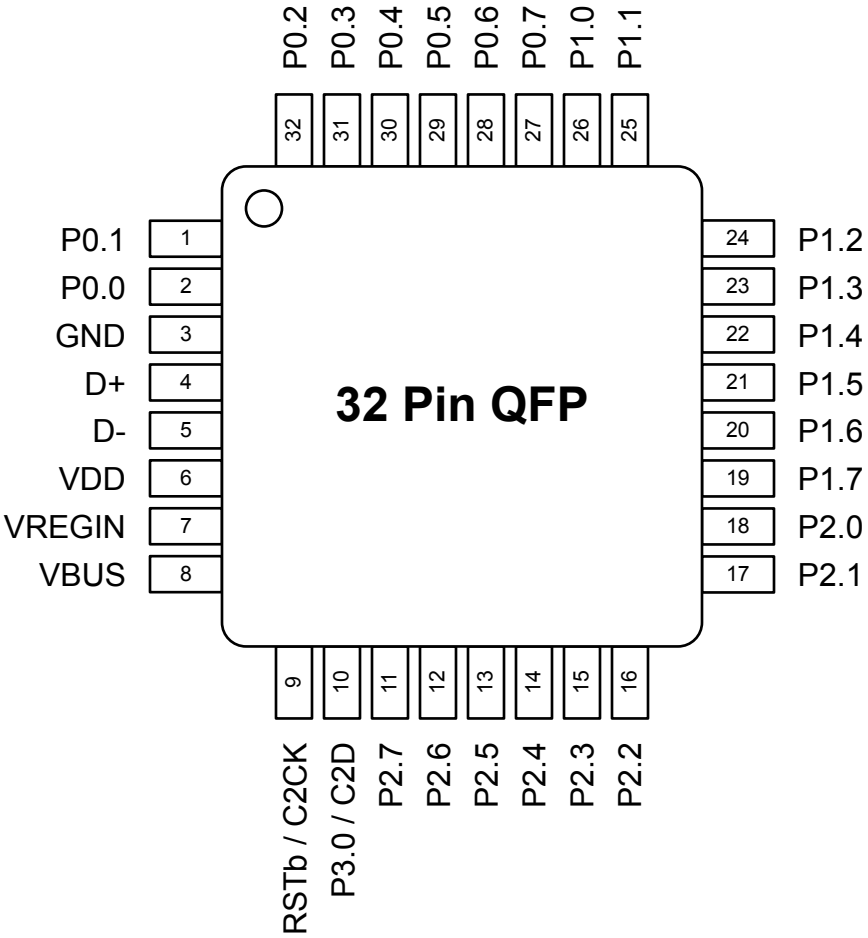

Figure 6.2. EFM8UB2x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8UB2x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	ADC0P.18 ADC0N.18 CMP0N.4
2	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	ADC0P.17 ADC0N.17 CMP0P.4
3	GND	Ground			
4	D+	USB Data Positive			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
20	P1.6	Multifunction I/O	Yes		ADC0P.6 ADC0N.6 CMP1P.1
21	P1.5	Multifunction I/O	Yes		ADC0P.5 ADC0N.5 CMP0N.1
22	P1.4	Multifunction I/O	Yes		ADC0P.4 ADC0N.4 CMP0P.1
23	P1.3	Multifunction I/O	Yes		ADC0P.3 ADC0N.3 CMP1N.0
24	P1.2	Multifunction I/O	Yes		ADC0P.2 ADC0N.2 CMP1P.0
25	P1.1	Multifunction I/O	Yes		ADC0P.1 ADC0N.1 CMP0N.0
26	P1.0	Multifunction I/O	Yes		ADC0P.0 ADC0N.0 CMP0P.0
27	P0.7	Multifunction I/O	Yes	INT0.7 INT1.7	VREF
28	P0.6	Multifunction I/O	Yes	CNVSTR INT0.6 INT1.6	
29	P0.5	Multifunction I/O	Yes	INT0.5 INT1.5 UART0_RX	ADC0P.20 ADC0N.20 CMP1N.4
30	P0.4	Multifunction I/O	Yes	INT0.4 INT1.4 UART0_TX	ADC0P.19 ADC0N.19 CMP1P.4
31	P0.3	Multifunction I/O	Yes	EXTCLK INT0.3 INT1.3	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
32	P0.2	Multifunction I/O	Yes	INT0.2 INT1.2	
Note: XTAL1 and XTAL2 are not available on this package. EXTCLK is still available on P0.3.					

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	ADC0P.17 ADC0N.17 CMP0P.4
3	GND	Ground			
4	D+	USB Data Positive			
5	D-	USB Data Negative			
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	VBUS	USB VBUS Sense Input		VBUS	
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		ADC0P.16 ADC0N.16
11	P2.7	Multifunction I/O	Yes		ADC0P.15 ADC0N.15
12	P2.6	Multifunction I/O	Yes		ADC0P.14 ADC0N.14
13	P2.5	Multifunction I/O	Yes		ADC0P.13 ADC0N.13 CMP0N.3
14	P2.4	Multifunction I/O	Yes		ADC0P.12 ADC0N.12 CMP0P.3
15	P2.3	Multifunction I/O	Yes		ADC0P.11 ADC0N.11 CMP1N.2
16	P2.2	Multifunction I/O	Yes		ADC0P.10 ADC0N.10 CMP1P.2
17	P2.1	Multifunction I/O	Yes		ADC0P.9 ADC0N.9 CMP0N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P2.0	Multifunction I/O	Yes		ADC0P.8 ADC0N.8 CMP0P.2
19	P1.7	Multifunction I/O	Yes		ADC0P.7 ADC0N.7 CMP1N.1
20	P1.6	Multifunction I/O	Yes		ADC0P.6 ADC0N.6 CMP1P.1
21	P1.5	Multifunction I/O	Yes		ADC0P.5 ADC0N.5 CMP0N.1
22	P1.4	Multifunction I/O	Yes		ADC0P.4 ADC0N.4 CMP0P.1
23	P1.3	Multifunction I/O	Yes		ADC0P.3 ADC0N.3 CMP1N.0
24	P1.2	Multifunction I/O	Yes		ADC0P.2 ADC0N.2 CMP1P.0
25	P1.1	Multifunction I/O	Yes		ADC0P.1 ADC0N.1 CMP0N.0
26	P1.0	Multifunction I/O	Yes		ADC0P.0 ADC0N.0 CMP0P.0
27	P0.7	Multifunction I/O	Yes	INT0.7 INT1.7	VREF
28	P0.6	Multifunction I/O	Yes	CNVSTR INT0.6 INT1.6	
29	P0.5	Multifunction I/O	Yes	INT0.5 INT1.5 UART0_RX	ADC0P.20 ADC0N.20 CMP1N.4

Dimension	Min	Typ	Max
ccc		0.08	
ddd		0.08	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2 QFP48 PCB Land Pattern

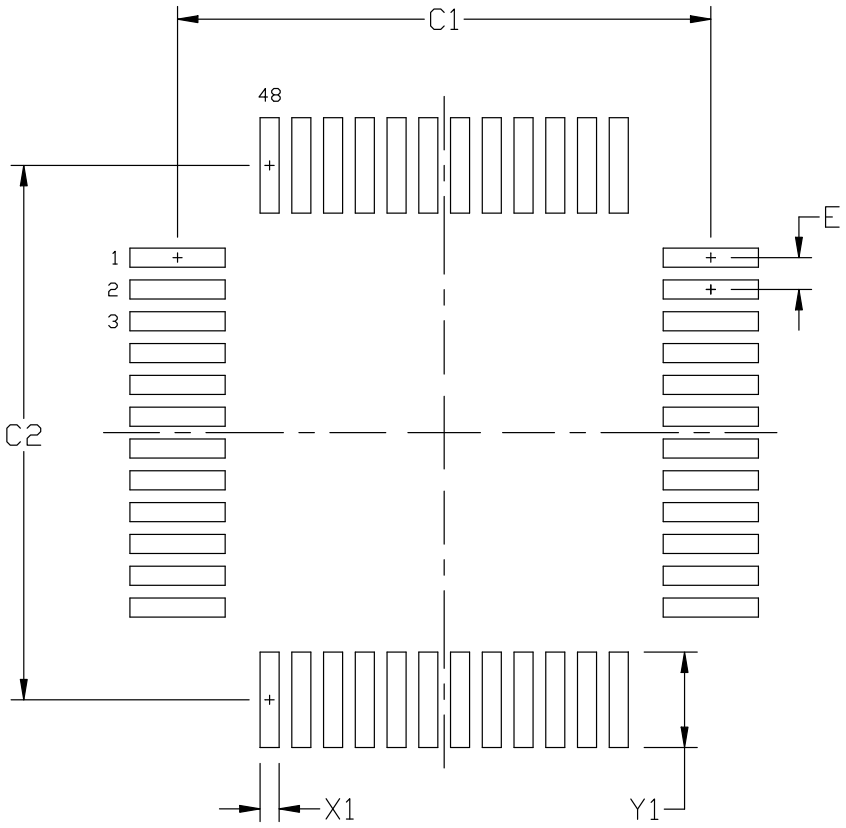

Figure 7.2. QFP48 PCB Land Pattern Drawing

Table 7.2. QFP48 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.30	8.40
C2	8.30	8.40
E	0.50 BSC	
X1	0.20	0.30
Y1	1.40	1.50

Dimension	Min	Typ	Max
bbb		0.20	
ccc		0.10	
ddd		0.20	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. QFN32 Package Specifications

9.1 QFN32 Package Dimensions

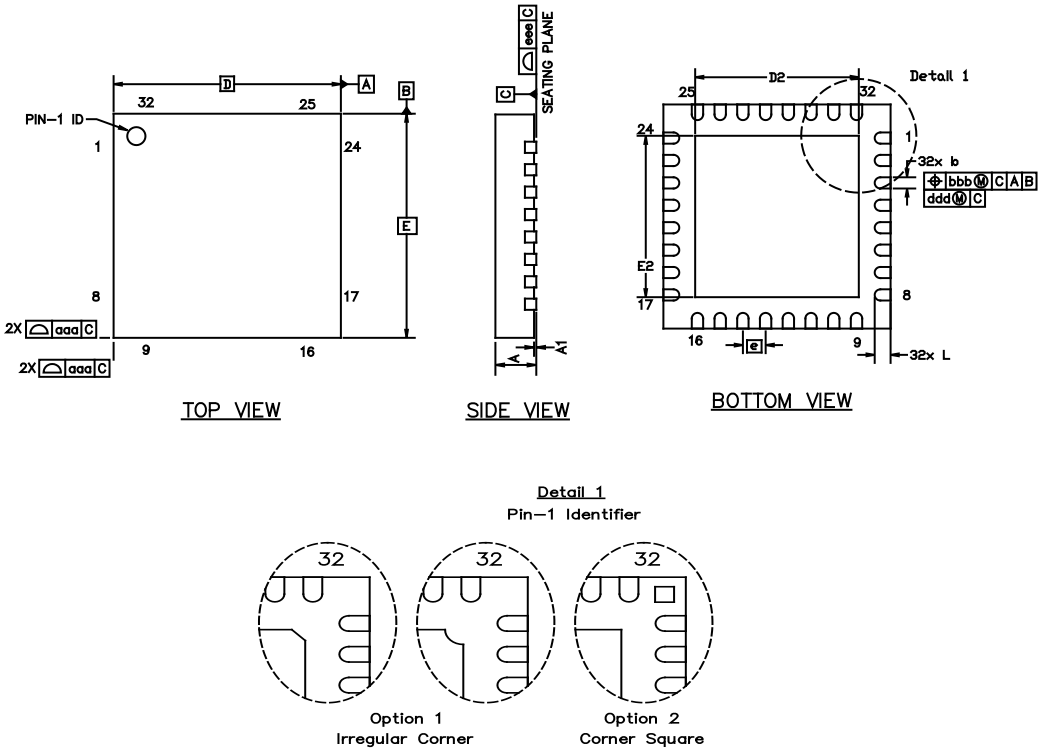

Figure 9.1. QFN32 Package Drawing

Table 9.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC	
D2	3.20	3.30	3.40
e		0.50 BSC	
E		5.00 BSC	
E2	3.20	3.30	3.40
L	0.35	0.40	0.45
aaa	—	—	0.10
bbb	—	—	0.10

Dimension	Min	Typ	Max
ddd	—	—	0.05
eee	—	—	0.08

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.2 QFN32 PCB Land Pattern

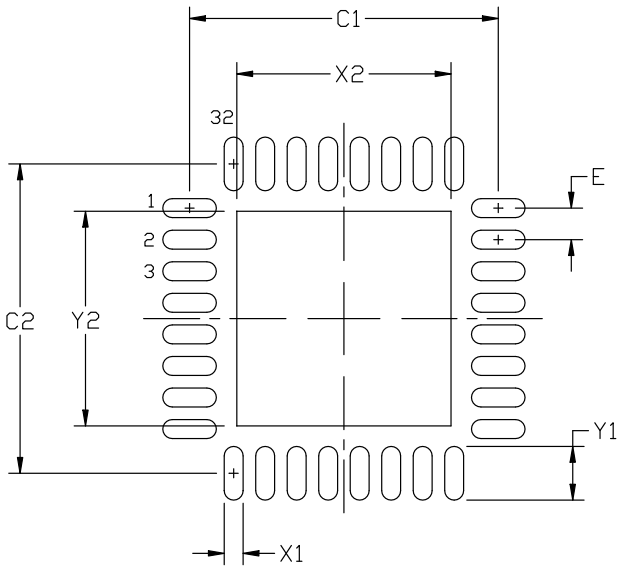

Figure 9.2. QFN32 PCB Land Pattern Drawing

Table 9.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. Revision History

10.1 Revision 1.3

Updated ordering part numbers to revision B.

Added Power-On Reset Threshold and Reset Delay from POR specifications to 4.1.3 Reset and Supply Monitor.

Added CRC Calculation Time specification to 4.1.4 Flash Memory.

Added VBUS Detection Input High Voltage and VBUS Detection Input Low Voltage specifications to Table 4.14 USB Transceiver on page 20.

Added specifications for 4.1.15 SMBus.

Added 5.4 Debug.

Added information about bootloader implementation and bootloader pinout to 3.10 Bootloader.

Added notes to Table 6.3 Pin Definitions for EFM8UB2x-QFN32 on page 37 and Table 6.2 Pin Definitions for EFM8UB2x-QFP32 on page 33 to clarify that XTAL1 and XTAL2 are not available on the 32-pin packages.

Updated Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 and Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 to recommend 4.7 µF capacitors instead of 1.0 µF capacitors.

Added text and Figure 5.3 Connection Diagram with Voltage Regulator Not Used on page 25 to demonstrate the proper connections when the regulator is not used.

Added reference to the Reference Manual in 3.1 Introduction.

10.2 Revision 1.2

Updated the VDD Ramp Time specification in Table 4.3 Reset and Supply Monitor on page 13 to a maximum of 1 ms.

10.3 Revision 1.1

Initial release.

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