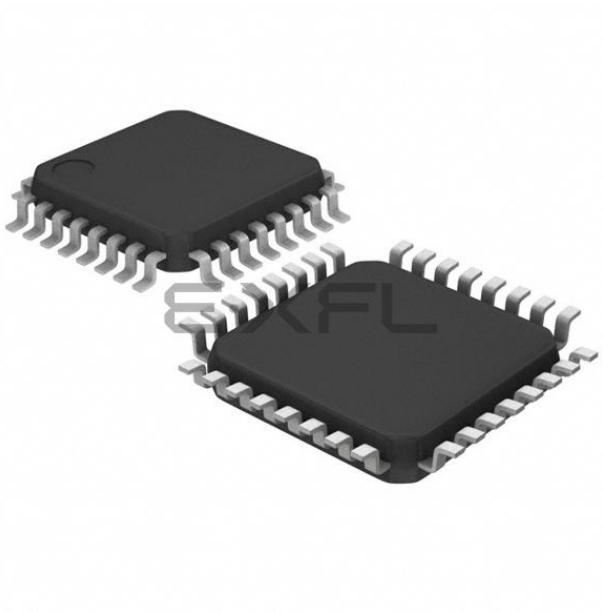

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f64g-a-qfp32

System Management Bus / I2C (SMB0 and SMB1)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus modules include the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

External Memory Interface (EMIF0)

The External Memory Interface (EMIF) enables access of off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either 8-bit or 16-bit formats.

- Supports multiplexed and non-multiplexed memory access.
- Four external memory modes:
  - Internal only.
  - Split mode without bank select.
  - Split mode with bank select.
  - External only
- Configurable ALE (address latch enable) timing.
- Configurable address setup and hold times.
- Configurable write and read pulse widths.

3.7 Analog

10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 10-bit mode, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

The ADC module is a Successive Approximation Register (SAR) Analog to Digital Converter (ADC). The key features of this ADC module are:

- Up to 32 external inputs.
- Differential or Single-ended 10-bit operation.
- Supports an output update rate of 500 ksps samples per second.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Two tracking mode options with programmable tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Voltage reference selectable from external reference pin, on-chip precision reference (driven externally on reference pin), or VDD supply.
- Integrated temperature sensor.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from regulators, supply monitor, and High Frequency Oscillator.
3. Includes supply current from regulators, supply monitor, and Low Frequency Oscillator.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		2.60	2.65	2.70	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.7 V	—	—	1	ms
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	—	250	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} >1 MHz	80	580	800	µs
VDD Supply Monitor Turn-On Time	t_{MON}		—	—	100	µs

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1]	t_{WRITE}	One Byte	10	15	20	µs
Erase Time[1]	t_{ERASE}	One Page	10	15	22.5	ms
V_{DD} Voltage During Programming[2]	V_{PROG}		2.7	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		10k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block SYSCLK = 48 MHz	—	5.5	—	µs

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
3. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.18 Absolute Maximum Ratings on page 23 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.18. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		-55	125	°C
Storage Temperature	T_{STG}		-65	150	°C
Voltage on VDD	V_{DD}		GND-0.3	4.2	V
Voltage on VREGIN	V_{REGIN}		GND-0.3	5.8	V
Voltage on I/O, RSTb, or VBUS pins	V_{IN}	V_{DD} > 2.2 V	GND-0.3	5.8	V
		V_{DD} < 2.2 V	GND-0.3	V_{DD}+3.6	V
Total Current Sunk into Supply Pin	I_{VDD}		—	500	mA
Total Current Sourced out of Ground Pin	I_{GND}		500	—	mA
Current Sourced or Sunk by any I/O Pin or RSTb	I_{IO}		-100	100	mA

Note:
1. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.4 Typical Performance Curves

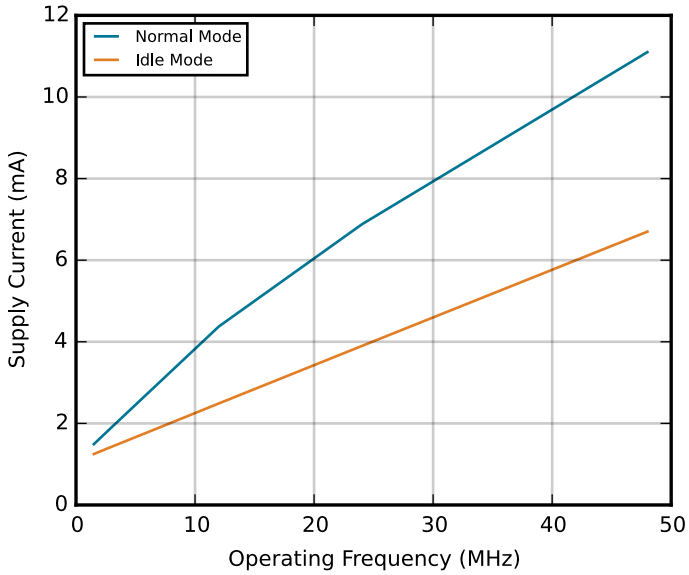

Figure 4.2. Typical Operating Supply Current using HFOSC0

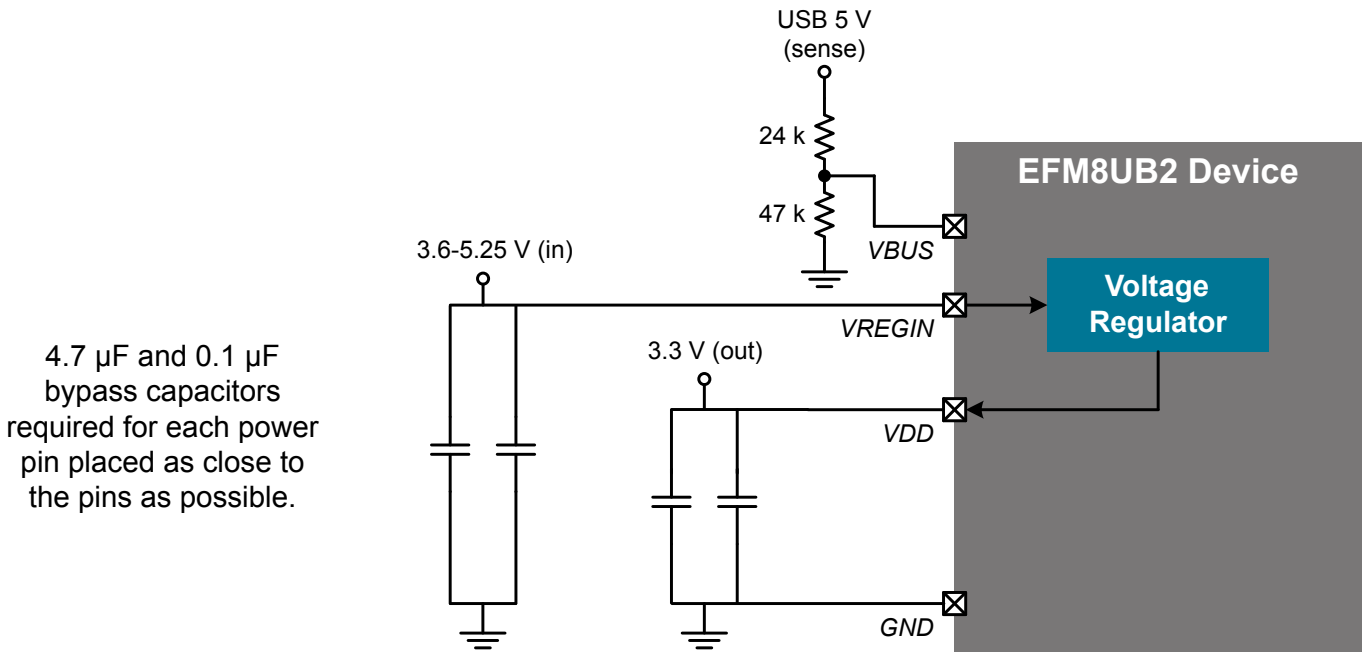

Figure 5.2. Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered)

The figure below shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal 5 V-to-3.3 V regulator is not used.

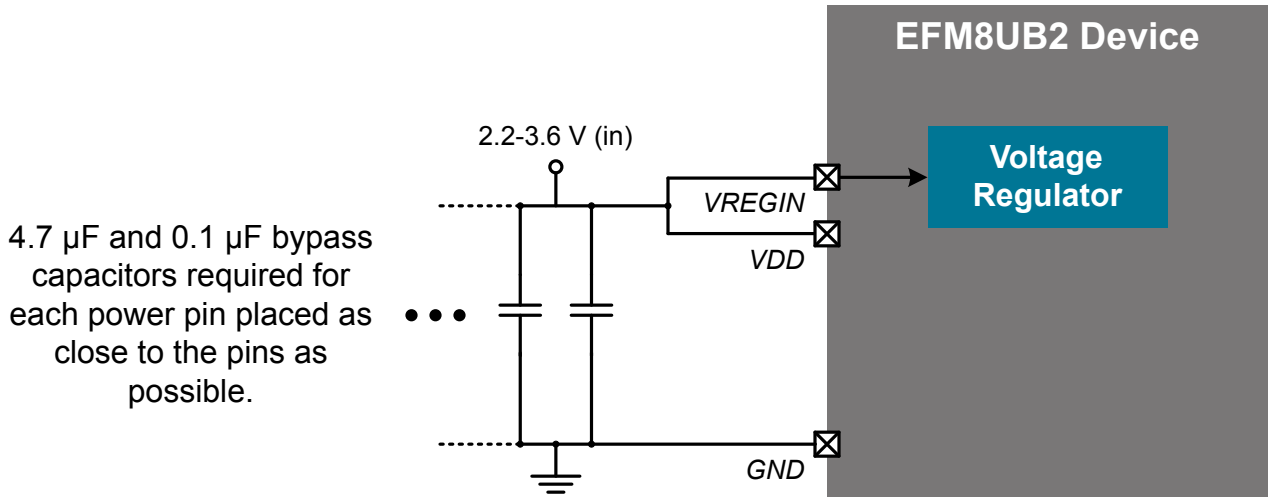

Figure 5.3. Connection Diagram with Voltage Regulator Not Used

5.2 USB

Figure 5.4 Connection Diagram for USB Pins on page 26 shows a typical connection diagram for the USB pins of the EFM8UB2 devices including ESD protection diodes on the USB pins.

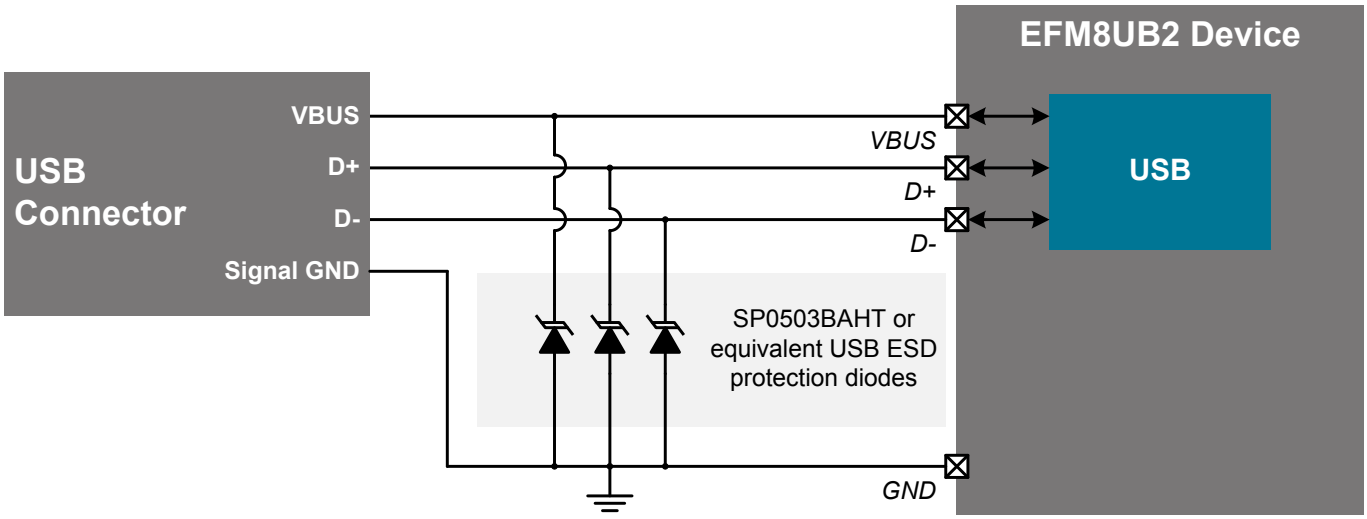

Figure 5.4. Connection Diagram for USB Pins

5.3 Voltage Reference (VREF)

Figure 5.5 Connection Diagram for Internal Voltage Reference on page 26 shows a typical connection diagram for the voltage reference (VREF) pin of the EFM8UB2 devices when using the internal voltage reference. When using an external voltage reference, consult the external reference data sheet for connection recommendations.

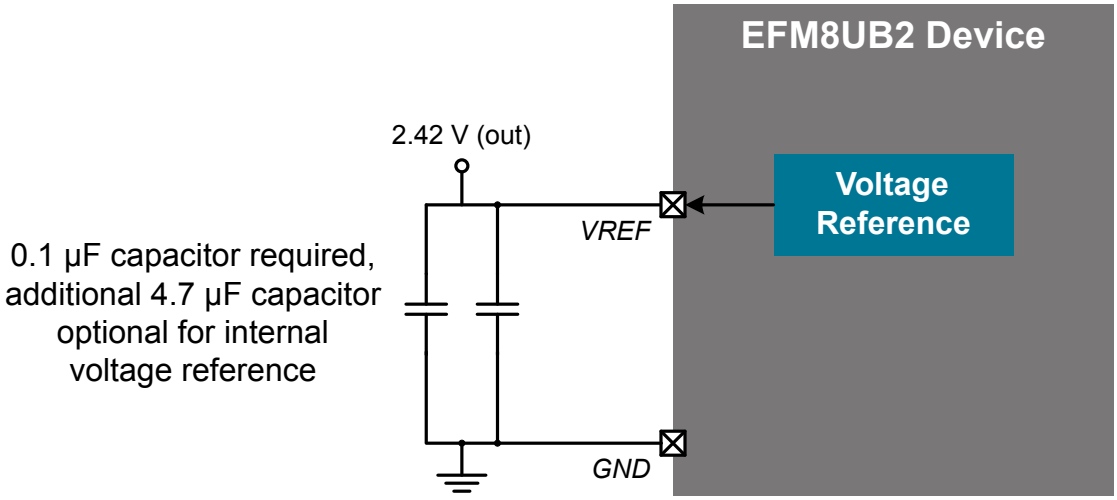

Figure 5.5. Connection Diagram for Internal Voltage Reference

6. Pin Definitions

6.1 EFM8UB2x-QFP48 Pin Definitions

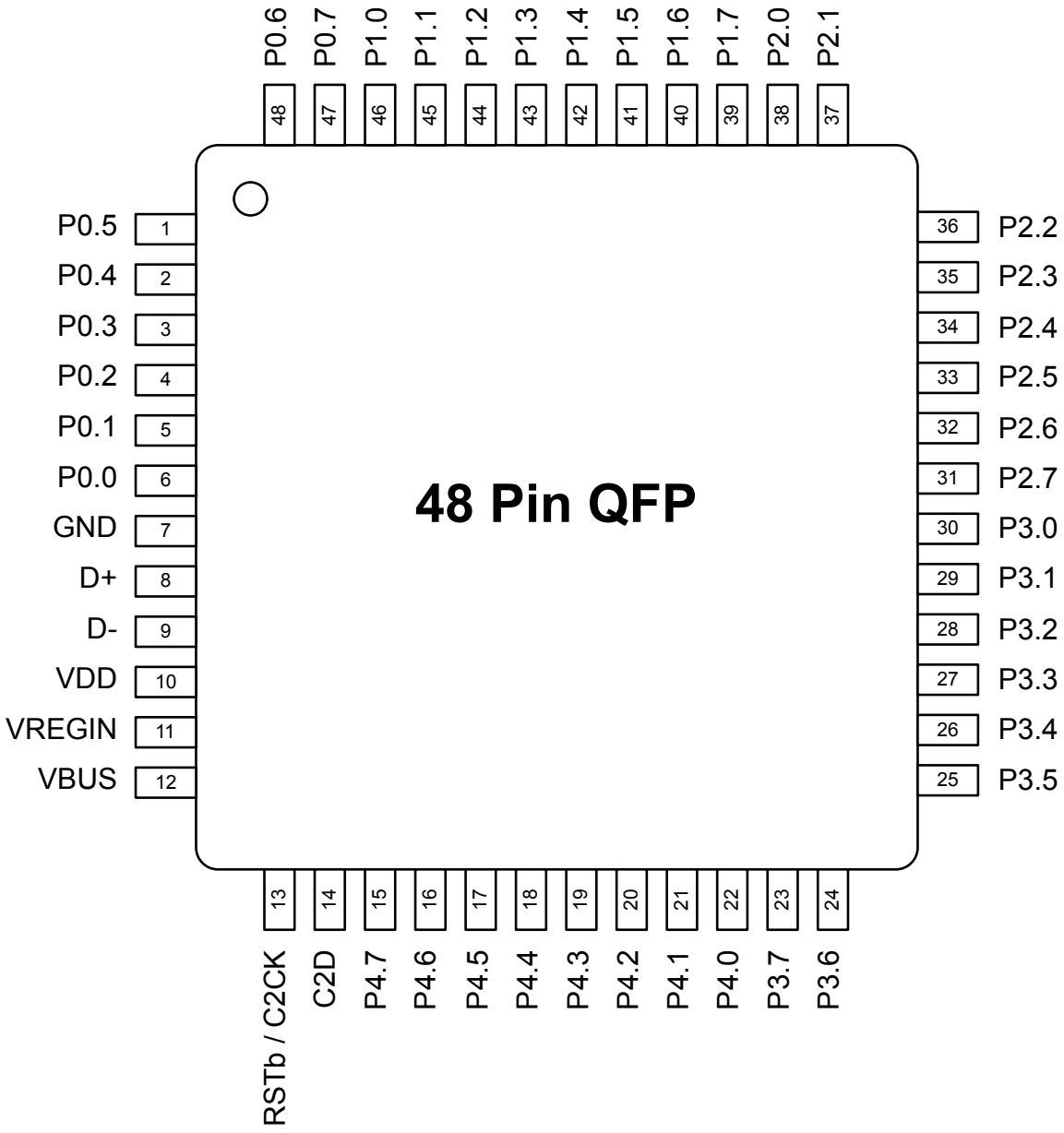

Figure 6.1. EFM8UB2x-QFP48 Pinout

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P4.4	Multifunction I/O		EMIF_D4 EMIF_AD4m	ADC0P.13 ADC0N.13 CMP0N.3
19	P4.3	Multifunction I/O		EMIF_D3 EMIF_AD3m	ADC0P.12 ADC0N.12 CMP0P.3
20	P4.2	Multifunction I/O		EMIF_D2 EMIF_AD2m	ADC0P.33 ADC0N.33
21	P4.1	Multifunction I/O		EMIF_D1 EMIF_AD1m	ADC0P.32 ADC0N.32
22	P4.0	Multifunction I/O		EMIF_D0 EMIF_AD0m	ADC0P.11 ADC0N.11 CMP1N.2
23	P3.7	Multifunction I/O	Yes	EMIF_A7 EMIF_A15m	ADC0P.10 ADC0N.10 CMP1P.2
24	P3.6	Multifunction I/O	Yes	EMIF_A6 EMIF_A14m	ADC0P.29 ADC0N.29
25	P3.5	Multifunction I/O	Yes	EMIF_A5 EMIF_A13m	ADC0P.9 ADC0N.9 CMP0N.2
26	P3.4	Multifunction I/O	Yes	EMIF_A4 EMIF_A12m	ADC0P.8 ADC0N.8 CMP0P.2
27	P3.3	Multifunction I/O	Yes	EMIF_A3 EMIF_A11m	ADC0P.28 ADC0N.28
28	P3.2	Multifunction I/O	Yes	EMIF_A2 EMIF_A10m	ADC0P.27 ADC0N.27
29	P3.1	Multifunction I/O	Yes	EMIF_A1 EMIF_A9m	ADC0P.7 ADC0N.7 CMP1N.1
30	P3.0	Multifunction I/O	Yes	EMIF_A0 EMIF_A8m	ADC0P.6 ADC0N.6 CMP1P.1
31	P2.7	Multifunction I/O	Yes	EMIF_A15	ADC0P.26 ADC0N.26

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
32	P2.6	Multifunction I/O	Yes	EMIF_A14	ADC0P.5 ADC0N.5 CMP0N.1
33	P2.5	Multifunction I/O	Yes	EMIF_A13	ADC0P.4 ADC0N.4 CMP0P.1
34	P2.4	Multifunction I/O	Yes	EMIF_A12	ADC0P.25 ADC0N.25
35	P2.3	Multifunction I/O	Yes	EMIF_A11	ADC0P.3 ADC0N.3 CMP1N.0
36	P2.2	Multifunction I/O	Yes	EMIF_A10	ADC0P.2 ADC0N.2 CMP1P.0
37	P2.1	Multifunction I/O	Yes	EMIF_A9	ADC0P.1 ADC0N.1 CMP0N.0
38	P2.0	Multifunction I/O	Yes	EMIF_A8	ADC0P.0 ADC0N.0 CMP0P.0
39	P1.7	Multifunction I/O	Yes	EMIF_WRb	ADC0P.24 ADC0N.24
40	P1.6	Multifunction I/O	Yes	EMIF_RDb	ADC0P.23 ADC0N.23
41	P1.5	Multifunction I/O	Yes		VREF
42	P1.4	Multifunction I/O	Yes	CNVSTR	
43	P1.3	Multifunction I/O	Yes	EMIF_ALEm	ADC0P.22 ADC0N.22
44	P1.2	Multifunction I/O	Yes		ADC0P.20 ADC0N.20 CMP1N.4
45	P1.1	Multifunction I/O	Yes		ADC0P.19 ADC0N.19 CMP1P.4
46	P1.0	Multifunction I/O	Yes		ADC0P.21 ADC0N.21

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
47	P0.7	Multifunction I/O	Yes	XTAL2 EXTCLK INT0.7 INT1.7	
48	P0.6	Multifunction I/O	Yes	XTAL1 INT0.6 INT1.6	

6.2 EFM8UB2x-QFP32 Pin Definitions

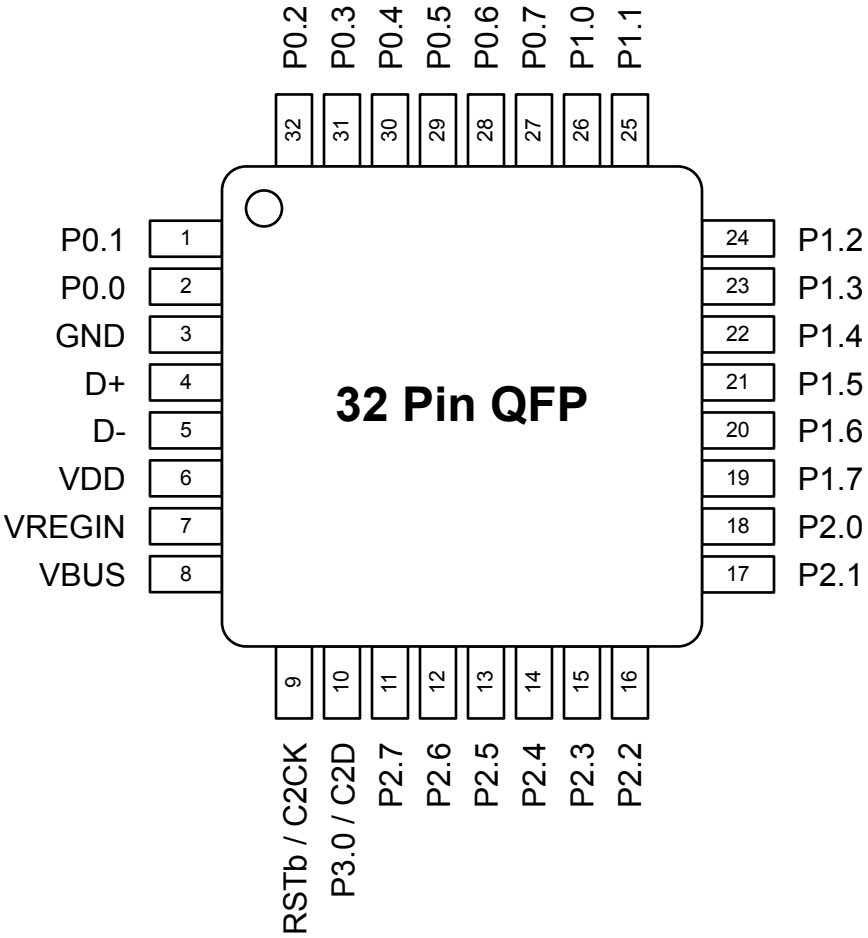

Figure 6.2. EFM8UB2x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8UB2x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	ADC0P.18 ADC0N.18 CMP0N.4
2	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	ADC0P.17 ADC0N.17 CMP0P.4
3	GND	Ground			
4	D+	USB Data Positive			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P2.0	Multifunction I/O	Yes		ADC0P.8 ADC0N.8 CMP0P.2
19	P1.7	Multifunction I/O	Yes		ADC0P.7 ADC0N.7 CMP1N.1
20	P1.6	Multifunction I/O	Yes		ADC0P.6 ADC0N.6 CMP1P.1
21	P1.5	Multifunction I/O	Yes		ADC0P.5 ADC0N.5 CMP0N.1
22	P1.4	Multifunction I/O	Yes		ADC0P.4 ADC0N.4 CMP0P.1
23	P1.3	Multifunction I/O	Yes		ADC0P.3 ADC0N.3 CMP1N.0
24	P1.2	Multifunction I/O	Yes		ADC0P.2 ADC0N.2 CMP1P.0
25	P1.1	Multifunction I/O	Yes		ADC0P.1 ADC0N.1 CMP0N.0
26	P1.0	Multifunction I/O	Yes		ADC0P.0 ADC0N.0 CMP0P.0
27	P0.7	Multifunction I/O	Yes	INT0.7 INT1.7	VREF
28	P0.6	Multifunction I/O	Yes	CNVSTR INT0.6 INT1.6	
29	P0.5	Multifunction I/O	Yes	INT0.5 INT1.5 UART0_RX	ADC0P.20 ADC0N.20 CMP1N.4

Dimension	Min	Typ	Max
ccc		0.08	
ddd		0.08	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 QFP48 Package Marking

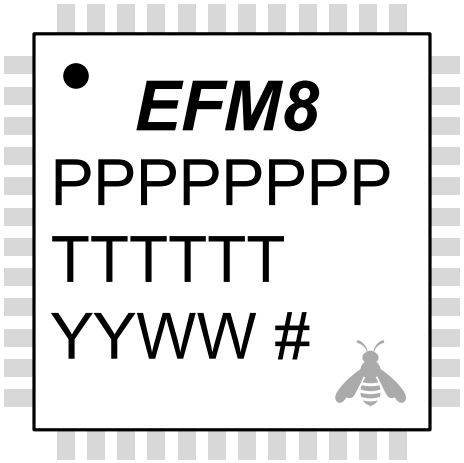

Figure 7.3. QFP48 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

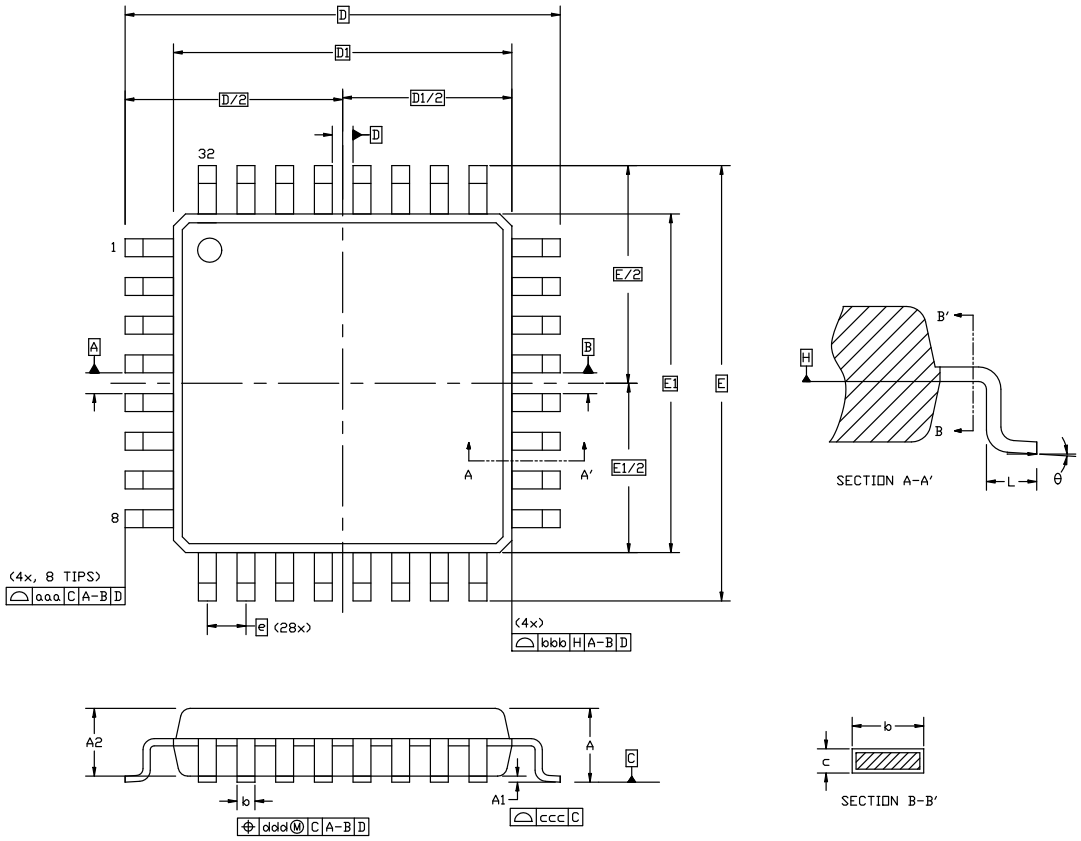

Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D		9.00 BSC	
D1		7.00 BSC	
e		0.80 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
aaa		0.20	

8.2 QFP32 PCB Land Pattern

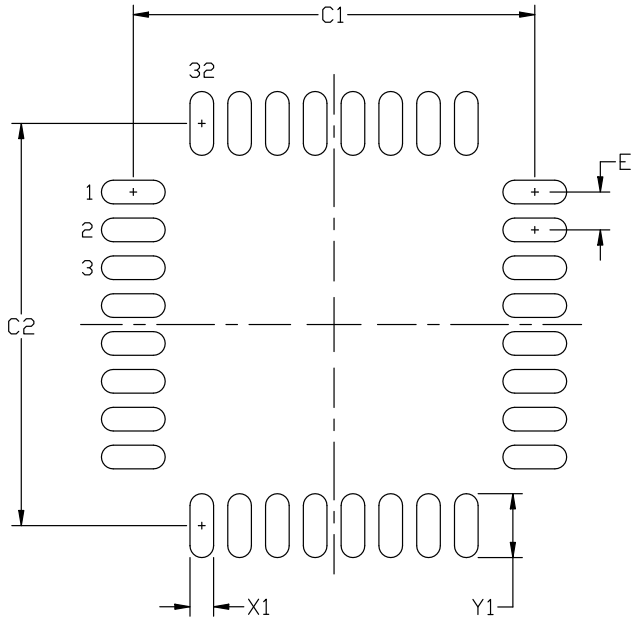

Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
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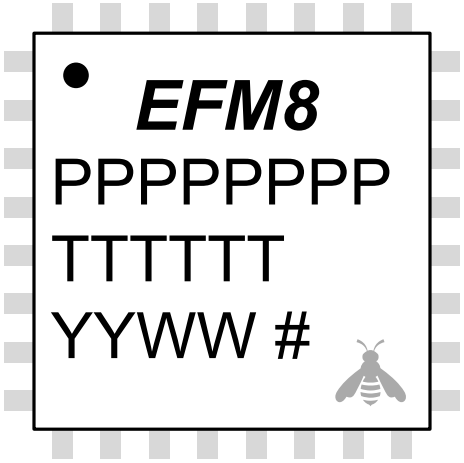
8.3 QFP32 Package Marking



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9. QFN32 Package Specifications

9.1 QFN32 Package Dimensions

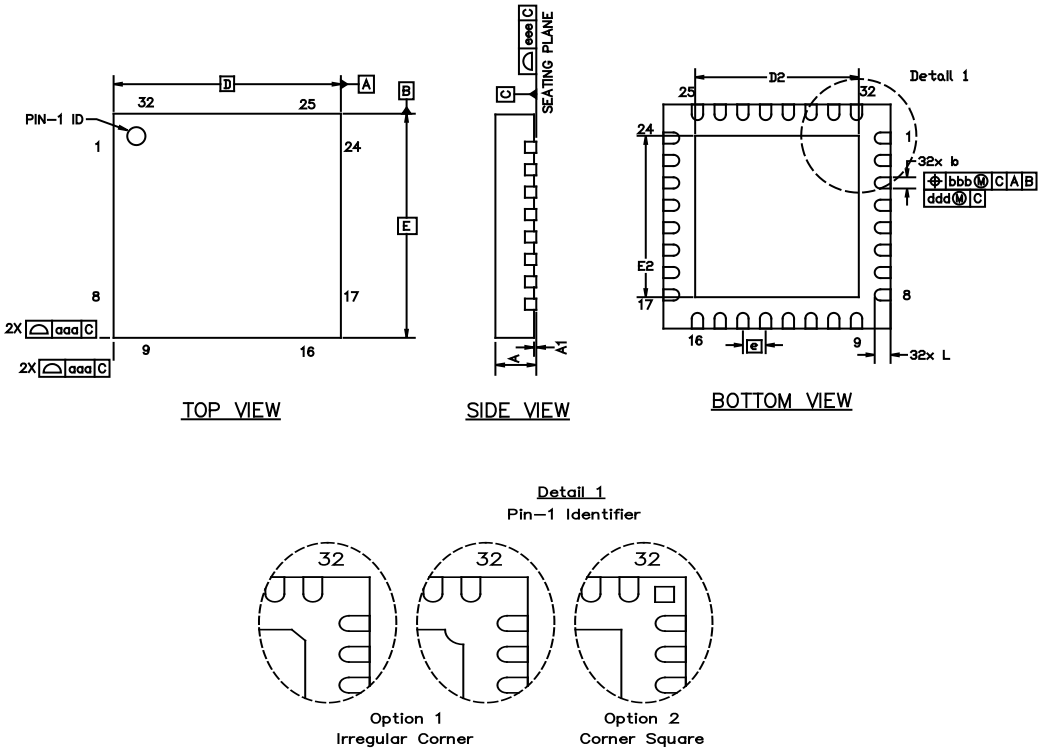

Figure 9.1. QFN32 Package Drawing

Table 9.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC	
D2	3.20	3.30	3.40
e		0.50 BSC	
E		5.00 BSC	
E2	3.20	3.30	3.40
L	0.35	0.40	0.45
aaa	—	—	0.10
bbb	—	—	0.10

9.3 QFN32 Package Marking

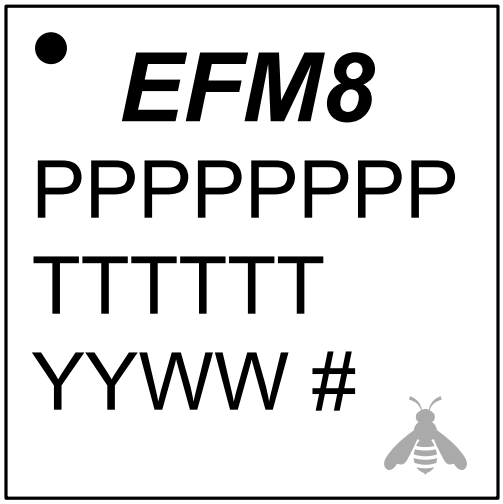

Figure 9.3. QFN32 Package Marking

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