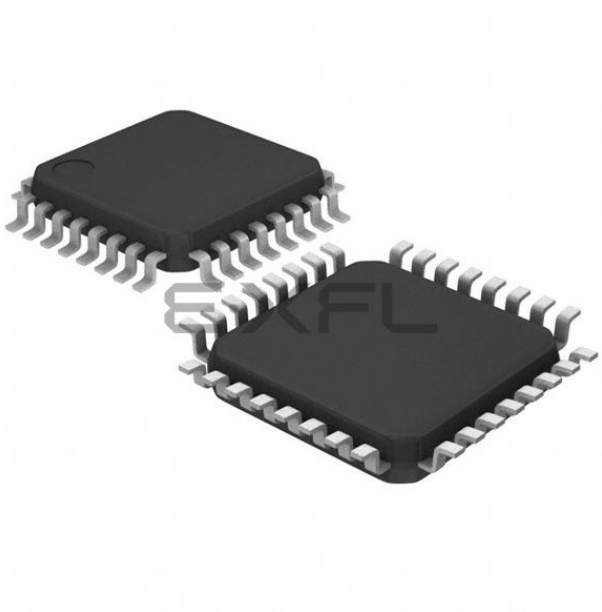

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f64g-a-qfp32r

3.10 Bootloader

All devices come pre-programmed with a USB bootloader. This bootloader resides in the last three pages of code flash, which includes the code security page; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

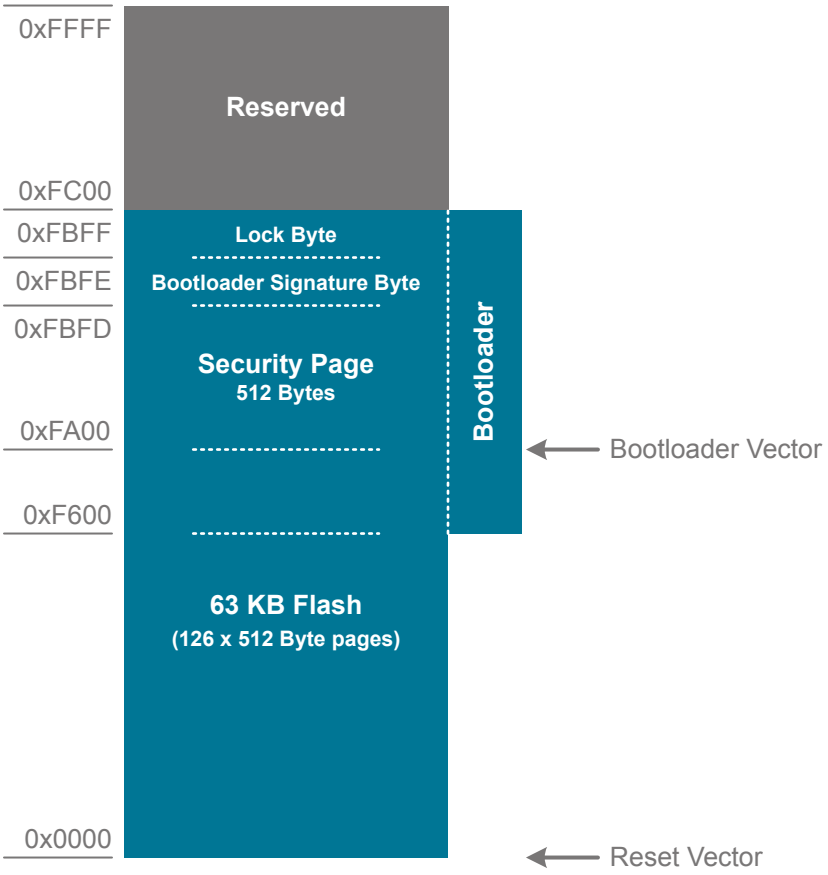

Figure 3.2. Flash Memory Map with Bootloader—64 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5
USB	VBUS
	D+
	D-

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 11, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		2.7[2]	3.3	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}		2.7	—	5.25	V
System Clock Frequency	f_{SYSCLK}		0	—	48	MHz
Operating Ambient Temperature	T_A		-40	—	85	°C

Note:

1. All voltages with respect to GND
2. The USB specification requires 3.0 V minimum supply voltage.

4.1.8 ADC

Table 4.8. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}			10		Bits
Throughput Rate	f_S		—	—	500	ksps
Tracking Time	t_{TRK}		300	—	—	ns
SAR Clock Frequency	f_{SAR}		—	—	8.33	MHz
Conversion Time	t_{CNV}	10-Bit Conversion,	13	—	—	Clocks
Sample/Hold Capacitor	C_{SAR}		—	30	—	pF
Input Mux Impedance	R_{MUX}		—	5	—	kΩ
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Single-Ended (AIN+ - GND)	0	—	V_{REF}	V
		Differential (AIN+ - AIN-)	$-V_{REF}$	—	V_{REF}	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance, VREF = 2.4 V						
Integral Nonlinearity	INL		—	±0.5	±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Offset Error	E_{OFF}		-2	0	2	LSB
Offset Temperature Coefficient	TC_{OFF}		—	0.005	—	LSB/°C
Slope Error	E_M		—	-0.2	±0.5	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, VREF = 2.4 V						
Signal-to-Noise	SNR		55	58	—	dB
Signal-to-Noise Plus Distortion	SNDR		55	58	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD		—	-73	—	dB
Spurious-Free Dynamic Range	SFDR		—	78	—	dB

Note:
1. Absolute input pin voltage is limited by the VDD and GND supply pins.

4.1.11 5 V Voltage Regulator

Table 4.11. 5V Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range[1]	V_{REGIN}		2.7	—	5.25	V
Output Voltage on VDD[2]	V_{REGOUT}	Output Current = 1 to 100 mA	3.0	3.3	3.6	V
Output Current[2]	I_{REGOUT}		—	—	100	mA

Note:
1. Input range specified for regulation. When an external regulator is used, VREGIN should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

4.1.14 USB Transceiver

Table 4.14. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VBUS Detection Input Low Voltage	V_{BUS_L}		—	—	1.0	V
VBUS Detection Input High Voltage	V_{BUS_H}		3.0	—	—	V
Transmitter						
Output High Voltage	V_{OH}	V_{DD} ≥3.0V	2.8	—	—	V
Output Low Voltage	V_{OL}	V_{DD} ≥3.0V	—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High	—	38	—	Ω
		Driving Low	—	38	—	
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up)	1.425	1.5	1.575	kΩ
		Low Speed (D- Pull-up)				
Output Rise Time	T_R	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Output Fall Time	T_F	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Receiver						V
Differential Input Sensitivity	V_{DI}	| (D+) - (D-) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Refer to the USB Specification for timing diagrams and symbol definitions.						

4.1.15 SMBus

Table 4.15. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		0	—	—	µs
Data Setup Time	$t_{SU:DAT}$		4.7	—	—	µs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[3]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	256[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	256[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		0	—	—	µs
Data Setup Time	$t_{SU:DAT}$		1.3	—	—	µs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[3]	µs

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (bus-powered). The VBUS signal is used to detect when USB is connected to a host device.

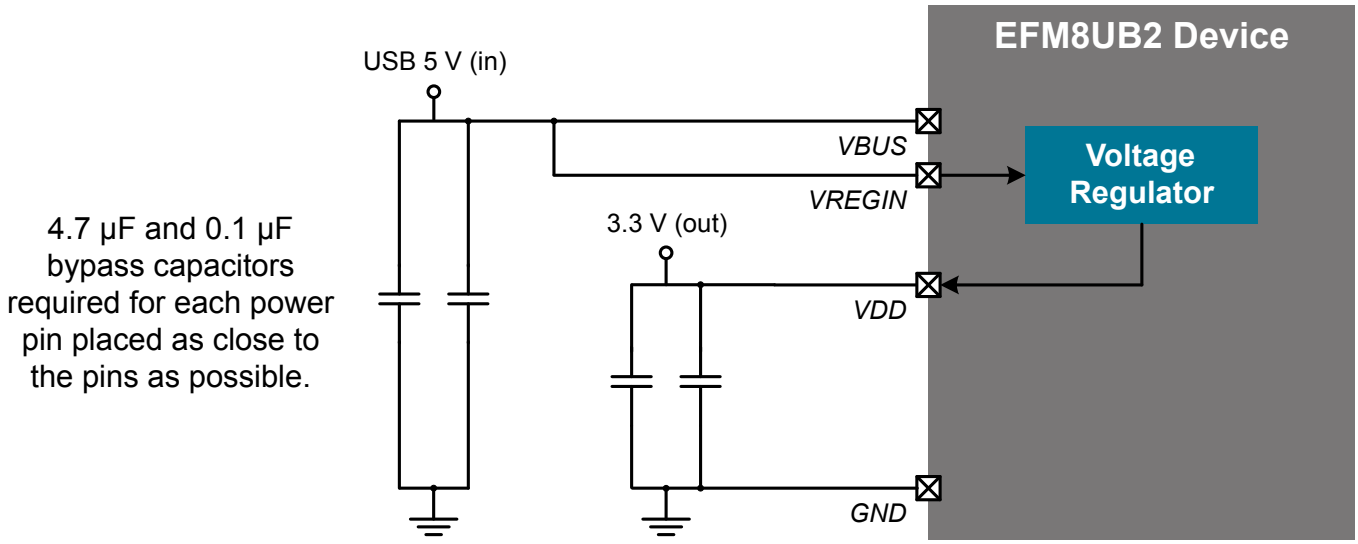

Figure 5.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (self-powered). The VBUS signal is used to detect when USB is connected to a host device and is shown with a resistor divider. This resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification for self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V.

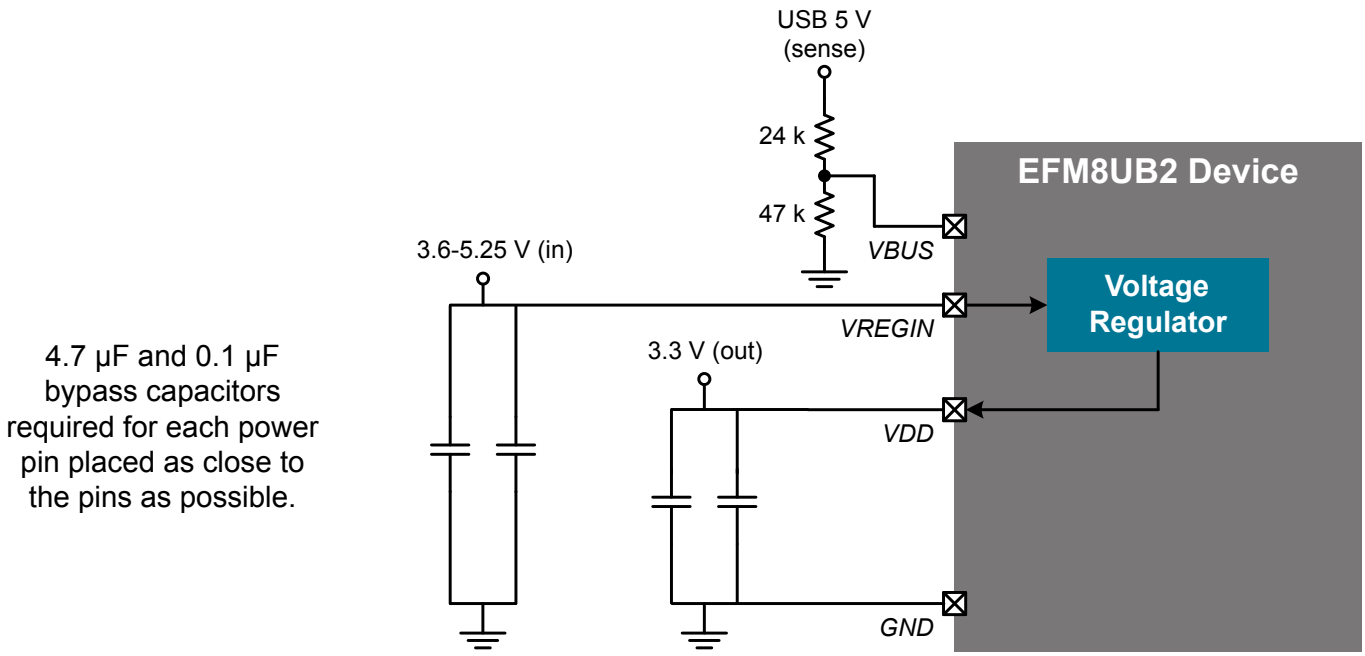

Figure 5.2. Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered)

The figure below shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal 5 V-to-3.3 V regulator is not used.

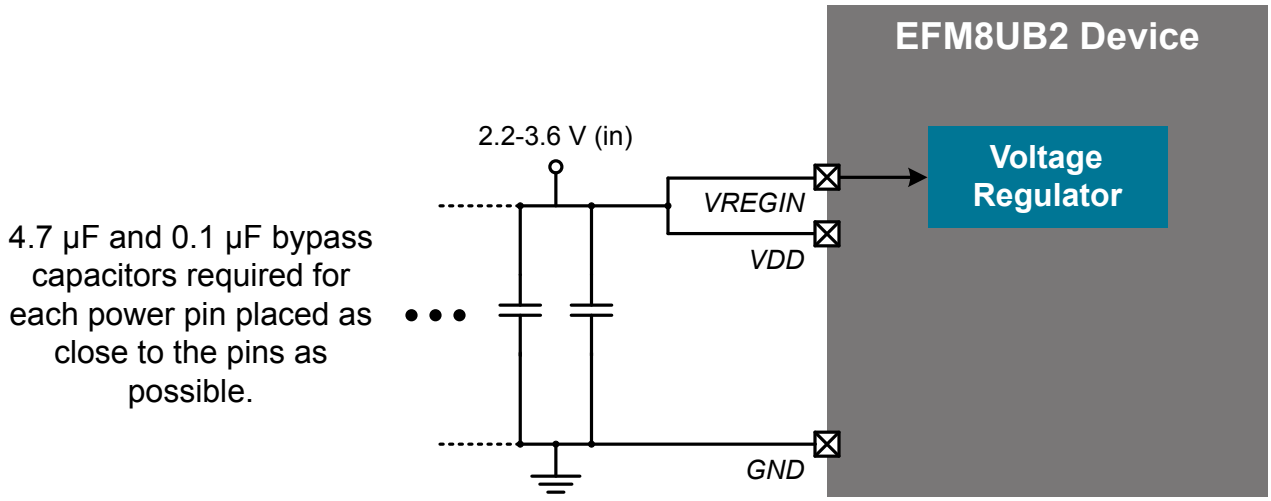

Figure 5.3. Connection Diagram with Voltage Regulator Not Used

6. Pin Definitions

6.1 EFM8UB2x-QFP48 Pin Definitions

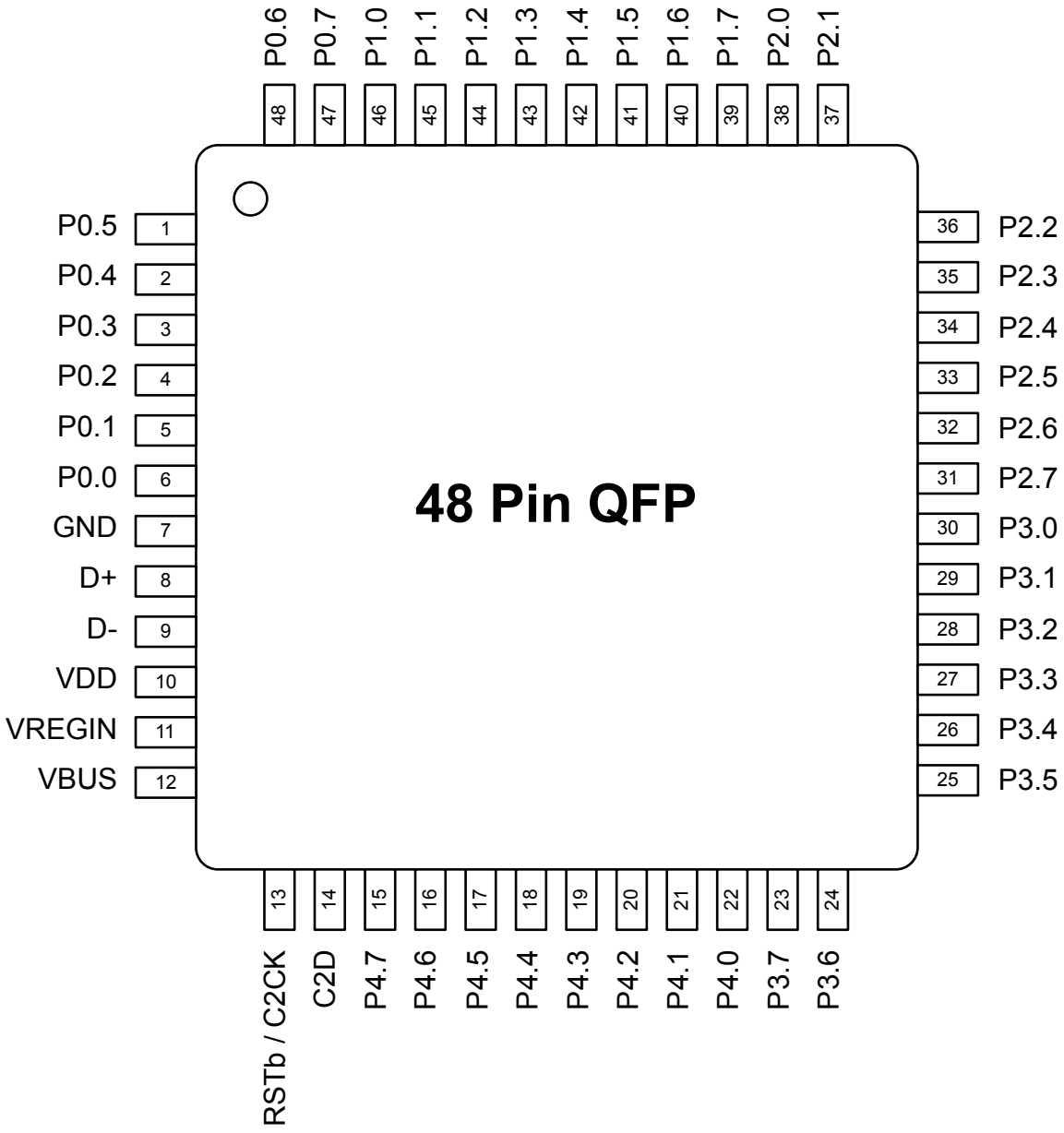

Figure 6.1. EFM8UB2x-QFP48 Pinout

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
47	P0.7	Multifunction I/O	Yes	XTAL2 EXTCLK INT0.7 INT1.7	
48	P0.6	Multifunction I/O	Yes	XTAL1 INT0.6 INT1.6	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
5	D-	USB Data Negative			
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	VBUS	USB VBUS Sense Input		VBUS	
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		ADC0P.16 ADC0N.16
11	P2.7	Multifunction I/O	Yes		ADC0P.15 ADC0N.15
12	P2.6	Multifunction I/O	Yes		ADC0P.14 ADC0N.14
13	P2.5	Multifunction I/O	Yes		ADC0P.13 ADC0N.13 CMP0N.3
14	P2.4	Multifunction I/O	Yes		ADC0P.12 ADC0N.12 CMP0P.3
15	P2.3	Multifunction I/O	Yes		ADC0P.11 ADC0N.11 CMP1N.2
16	P2.2	Multifunction I/O	Yes		ADC0P.10 ADC0N.10 CMP1P.2
17	P2.1	Multifunction I/O	Yes		ADC0P.9 ADC0N.9 CMP0N.2
18	P2.0	Multifunction I/O	Yes		ADC0P.8 ADC0N.8 CMP0P.2
19	P1.7	Multifunction I/O	Yes		ADC0P.7 ADC0N.7 CMP1N.1

6.3 EFM8UB2x-QFN32 Pin Definitions

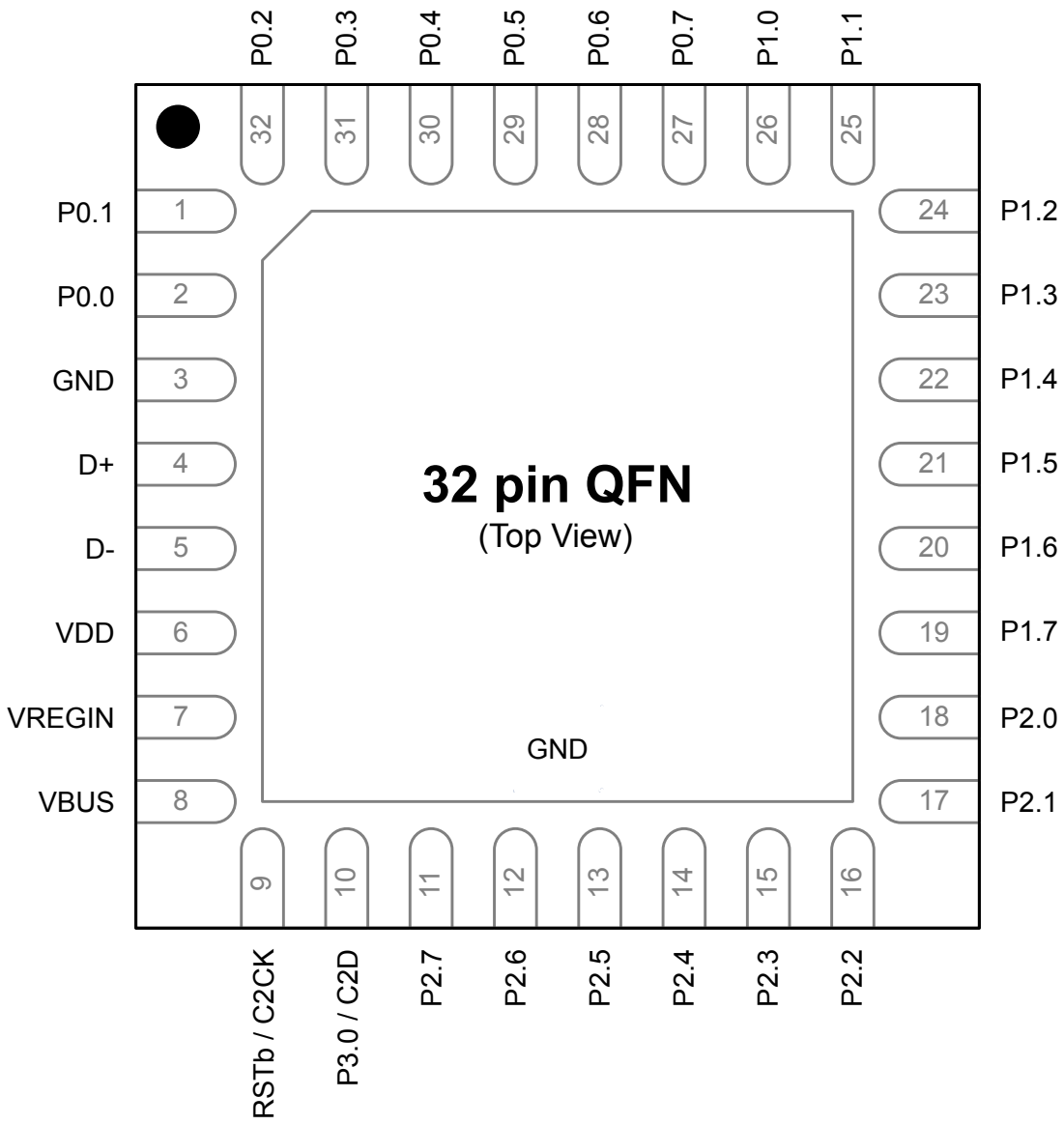

Figure 6.3. EFM8UB2x-QFN32 Pinout

Table 6.3. Pin Definitions for EFM8UB2x-QFN32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	ADC0P.18 ADC0N.18 CMP0N.4

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
2	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	ADC0P.17 ADC0N.17 CMP0P.4
3	GND	Ground			
4	D+	USB Data Positive			
5	D-	USB Data Negative			
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	VBUS	USB VBUS Sense Input		VBUS	
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		ADC0P.16 ADC0N.16
11	P2.7	Multifunction I/O	Yes		ADC0P.15 ADC0N.15
12	P2.6	Multifunction I/O	Yes		ADC0P.14 ADC0N.14
13	P2.5	Multifunction I/O	Yes		ADC0P.13 ADC0N.13 CMP0N.3
14	P2.4	Multifunction I/O	Yes		ADC0P.12 ADC0N.12 CMP0P.3
15	P2.3	Multifunction I/O	Yes		ADC0P.11 ADC0N.11 CMP1N.2
16	P2.2	Multifunction I/O	Yes		ADC0P.10 ADC0N.10 CMP1P.2
17	P2.1	Multifunction I/O	Yes		ADC0P.9 ADC0N.9 CMP0N.2

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

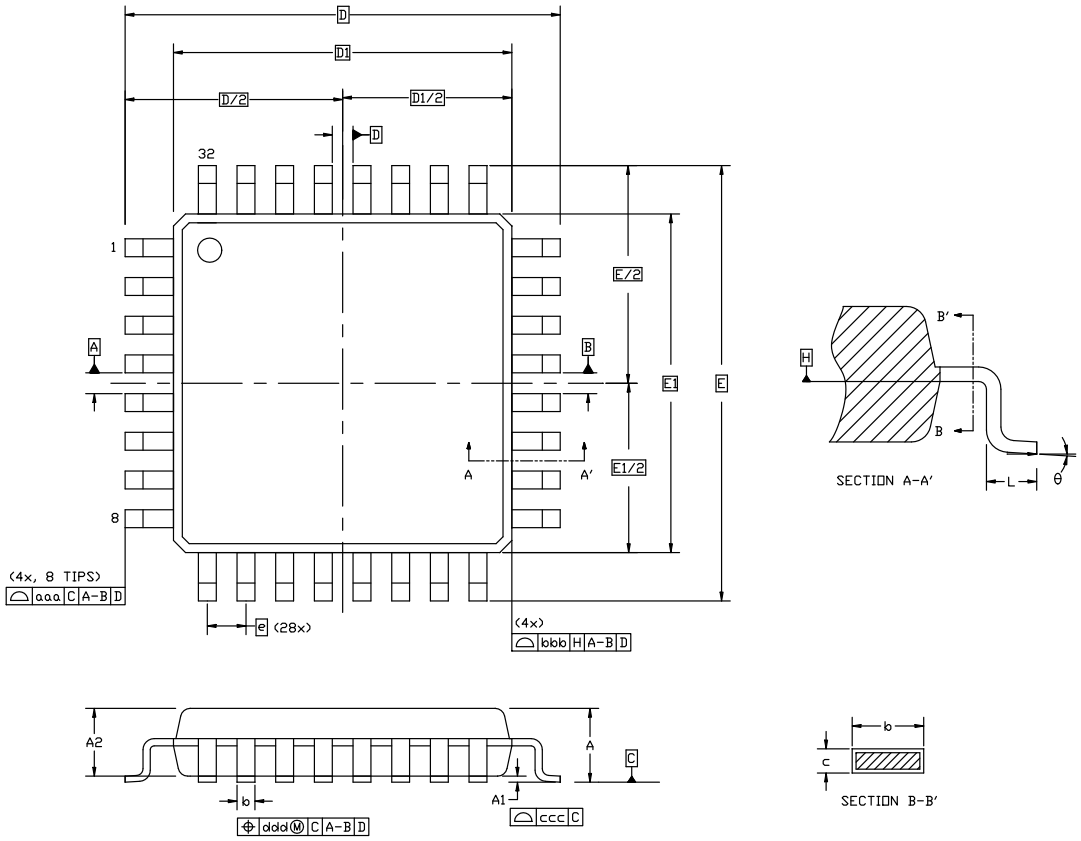

Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D		9.00 BSC	
D1		7.00 BSC	
e		0.80 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
aaa		0.20	

Dimension	Min	Typ	Max
bbb		0.20	
ccc		0.10	
ddd		0.20	
theta	0°	3.5°	7°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.3 QFP32 Package Marking

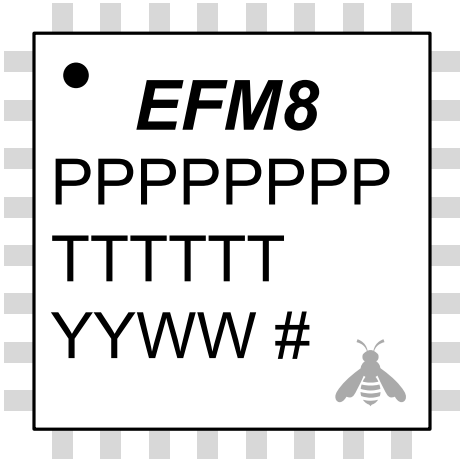

Figure 8.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. QFN32 Package Specifications

9.1 QFN32 Package Dimensions

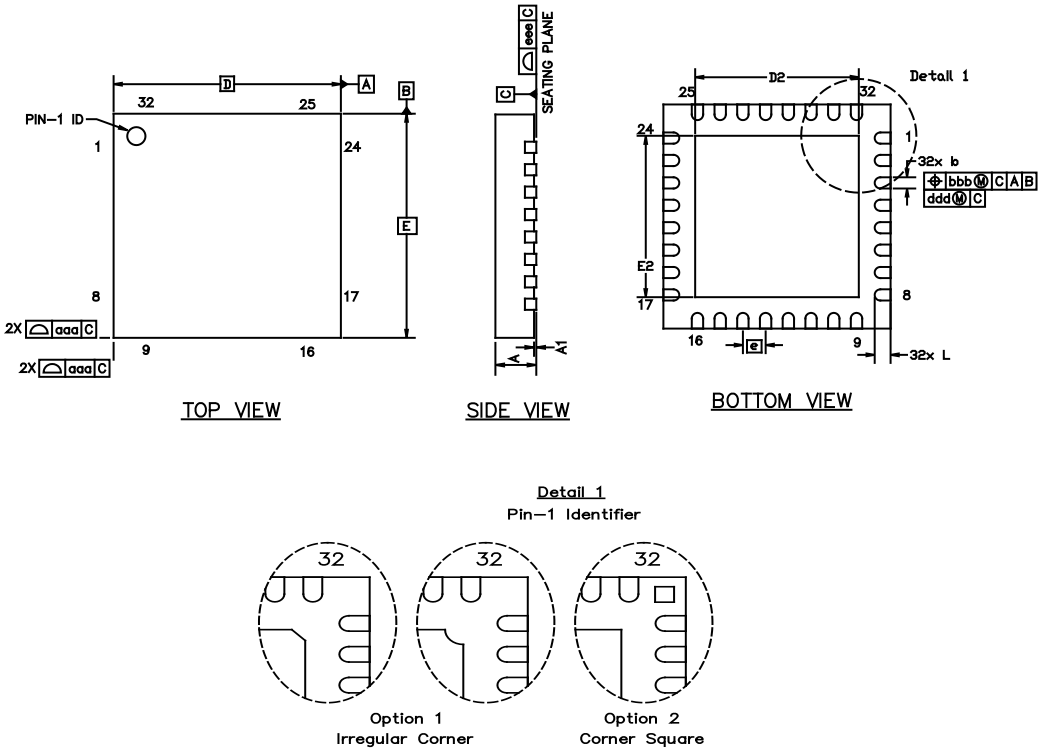

Figure 9.1. QFN32 Package Drawing

Table 9.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC	
D2	3.20	3.30	3.40
e		0.50 BSC	
E		5.00 BSC	
E2	3.20	3.30	3.40
L	0.35	0.40	0.45
aaa	—	—	0.10
bbb	—	—	0.10

9.2 QFN32 PCB Land Pattern

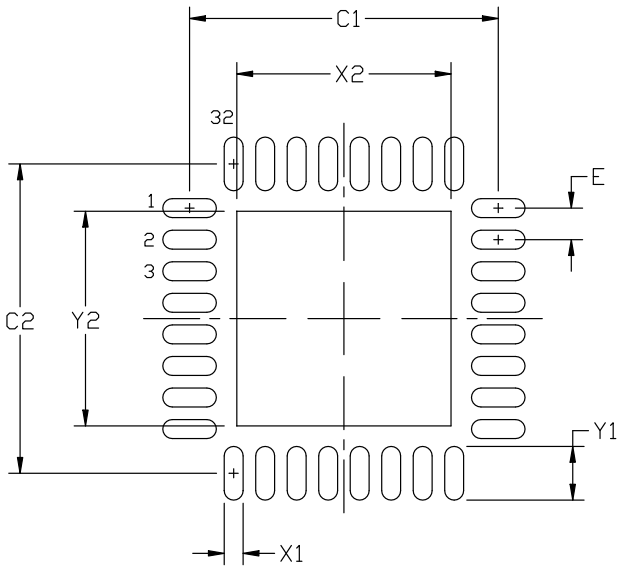

Figure 9.2. QFN32 PCB Land Pattern Drawing

Table 9.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. Revision History

10.1 Revision 1.3

Updated ordering part numbers to revision B.

Added Power-On Reset Threshold and Reset Delay from POR specifications to 4.1.3 Reset and Supply Monitor.

Added CRC Calculation Time specification to 4.1.4 Flash Memory.

Added VBUS Detection Input High Voltage and VBUS Detection Input Low Voltage specifications to Table 4.14 USB Transceiver on page 20.

Added specifications for 4.1.15 SMBus.

Added 5.4 Debug.

Added information about bootloader implementation and bootloader pinout to 3.10 Bootloader.

Added notes to Table 6.3 Pin Definitions for EFM8UB2x-QFN32 on page 37 and Table 6.2 Pin Definitions for EFM8UB2x-QFP32 on page 33 to clarify that XTAL1 and XTAL2 are not available on the 32-pin packages.

Updated Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 and Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 to recommend 4.7 µF capacitors instead of 1.0 µF capacitors.

Added text and Figure 5.3 Connection Diagram with Voltage Regulator Not Used on page 25 to demonstrate the proper connections when the regulator is not used.

Added reference to the Reference Manual in 3.1 Introduction.

10.2 Revision 1.2

Updated the VDD Ramp Time specification in Table 4.3 Reset and Supply Monitor on page 13 to a maximum of 1 ms.

10.3 Revision 1.1

Initial release.

Table of Contents