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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	EBI/EMI, I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f64g-a-qfp48r

2. Ordering Information

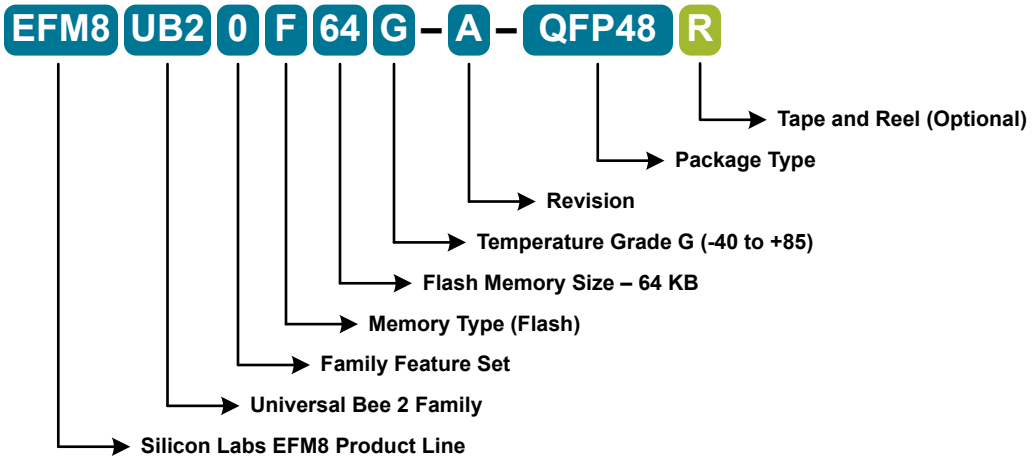


Figure 2.1. EFM8UB2 Part Numbering

All EFM8UB2 family members have the following features:

- CIP-51 Core running up to 48 MHz
- Two Internal Oscillators (48 MHz and 80 kHz)
- USB Full/Low speed Function Controller
- 5 V-In, 3.3 V-Out Regulator
- 2 SMBus/I2C Interfaces
- SPI
- 2 UARTs
- 5-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 6 16-bit Timers
- 2 Analog Comparators
- 10-bit Differential Analog-to-Digital Converter with integrated multiplexer and temperature sensor
- Pre-loaded USB bootloader

In addition to these features, each part number in the EFM8UB2 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Crystal Oscillator	External Memory Interface	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8UB20F64G-B-QFP48	64	4352	40	32	5	5	Yes	Yes	Yes	-40 to +85 °C	QFP48
EFM8UB20F64G-B-QFP32	64	4352	25	20	5	4	—	—	Yes	-40 to +85 °C	QFP32
EFM8UB20F64G-B-QFN32	64	4352	25	20	5	4	—	—	Yes	-40 to +85 °C	QFN32
EFM8UB20F32G-B-QFP48	32	2304	40	32	5	5	Yes	Yes	Yes	-40 to +85 °C	QFP48
EFM8UB20F32G-B-QFP32	32	2304	25	20	5	4	—	—	Yes	-40 to +85 °C	QFP32
EFM8UB20F32G-B-QFN32	32	2304	25	20	5	4	—	—	Yes	-40 to +85 °C	QFN32

3. System Overview

3.1 Introduction

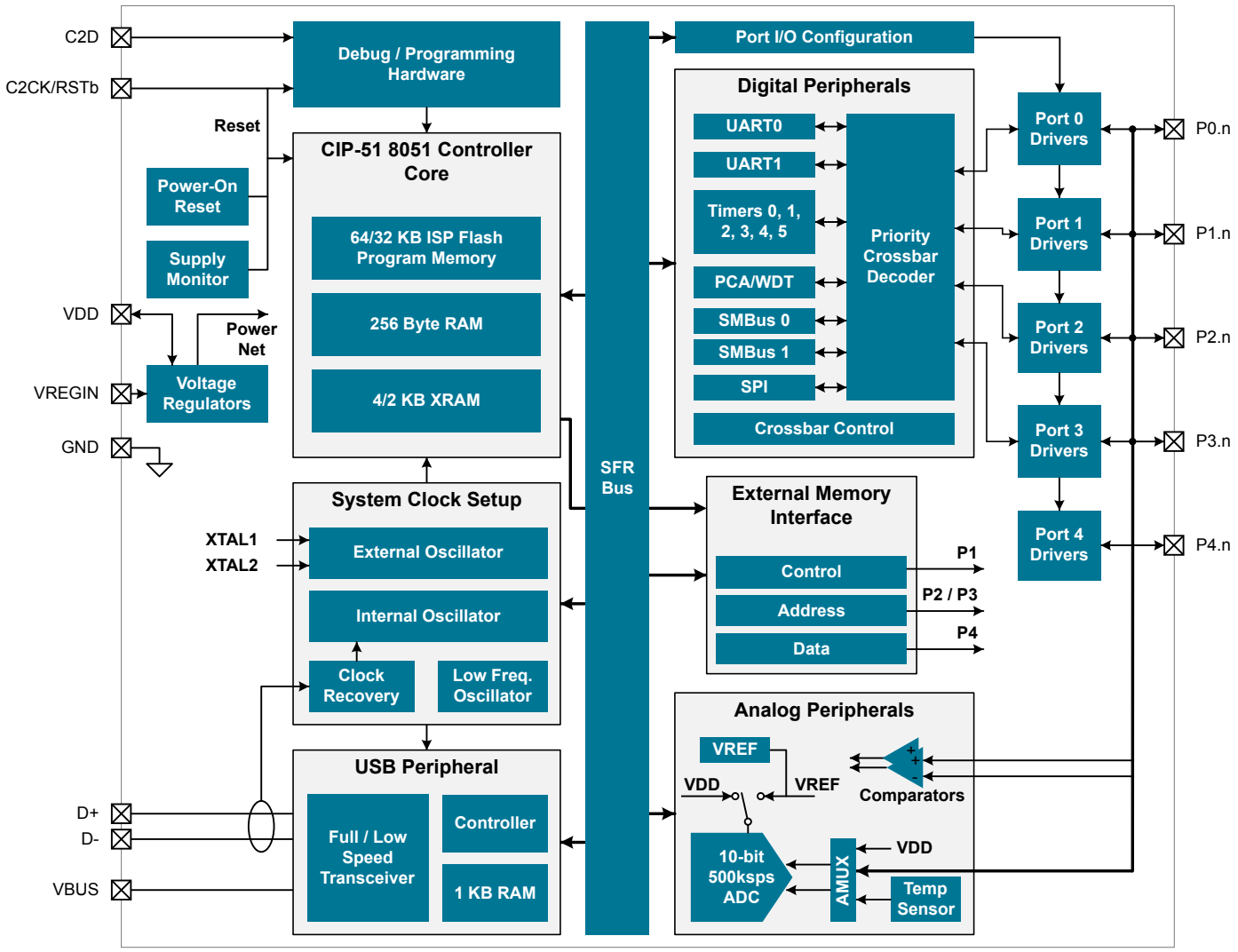


Figure 3.1. Detailed EFM8UB2 Block Diagram

This section describes the EFM8UB2 family at a high level. For more information on each module including register definitions, see the EFM8UB2 Reference Manual.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Up to five independently-configurable channels
- 8- or 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- USB start-of-frame or falling edge of LFOSC0 capture (Timer 2 and Timer 3)

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

System Management Bus / I2C (SMB0 and SMB1)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus modules include the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

External Memory Interface (EMIF0)

The External Memory Interface (EMIF) enables access of off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either 8-bit or 16-bit formats.

- Supports multiplexed and non-multiplexed memory access.
- Four external memory modes:
  - Internal only.
  - Split mode without bank select.
  - Split mode with bank select.
  - External only
- Configurable ALE (address latch enable) timing.
- Configurable address setup and hold times.
- Configurable write and read pulse widths.

3.7 Analog

10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 10-bit mode, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

The ADC module is a Successive Approximation Register (SAR) Analog to Digital Converter (ADC). The key features of this ADC module are:

- Up to 32 external inputs.
- Differential or Single-ended 10-bit operation.
- Supports an output update rate of 500 ksps samples per second.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Two tracking mode options with programmable tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Voltage reference selectable from external reference pin, on-chip precision reference (driven externally on reference pin), or VDD supply.
- Integrated temperature sensor.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I_{DD}	F_{SYSCLK} = 48 MHz[2]	—	12	14	mA
		F_{SYSCLK} = 24 MHz[2]	—	7	8	mA
		F_{SYSCLK} = 80 kHz[3]	—	280	—	µA
Idle Mode—Core halted with peripherals running	I_{DD}	F_{SYSCLK} = 48 MHz[2]	—	6.5	8	mA
		F_{SYSCLK} = 24 MHz[2]	—	3.5	5	mA
		F_{SYSCLK} = 80 kHz[3]	—	220	—	µA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off. Regulators in low-power mode.	I_{DD}	LFO Running	—	105	—	µA
		LFO Stopped	—	100	—	µA
Stop Mode—Core halted and all clocks stopped, Regulators in low-power mode, Supply monitor off.	I_{DD}		—	100	—	µA
Shutdown Mode—Core halted and all clocks stopped,Regulators Off, Supply monitor off.	I_{DD}		—	0.25	—	µA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I_{HFOSC0}	Operating at 48 MHz, T_A = 25 °C	—	900	—	µA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, T_A = 25 °C	—	5	—	µA
ADC0 Supply Current	I_{ADC}	Operating at 500 ksps V_{DD} = 3.0 V	—	750	1000	µA
On-chip Precision Reference	I_{VREFP}		—	75	—	µA
Temperature Sensor	I_{TSENSE}		—	35	—	µA
Comparator 0 (CMP0, CMP1)	I_{CMP}	CPMD = 11	—	1	—	µA
		CPMD = 10	—	4	—	µA
		CPMD = 01	—	10	—	µA
		CPMD = 00	—	20	—	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	50	µA
Regulator Bias Currents	I_{VREG}	Both Regulators in Normal Mode	—	200	—	µA
		Both Regulators in Low Power Mode	—	100	—	µA
		5 V Regulator Off, Internal LDO in Low Power Mode	—	150	—	µA
USB (USB0) Full-Speed	I_{USB}	Active	—	8	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V_{IN}		-0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	60	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	60	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV

4.1.13 Port I/O

Table 4.13. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage	V_{OH}	I_{OH} = -3 mA	V_{DD} - 0.7	—	—	V
		I_{OH} = -10 µA	V_{DD} - 0.1	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
		I_{OL} = 10 µA	—	—	0.1	V
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	-50	-15	—	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{DD}	-1	—	1	µA
Input Leakage Current with V_{IN} above V_{DD}	I_{LK}	V_{DD} < V_{IN} < V_{DD}+2.0 V	0	5	150	µA

4.1.14 USB Transceiver

Table 4.14. USB Transceiver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VBUS Detection Input Low Voltage	V_{BUS_L}		—	—	1.0	V
VBUS Detection Input High Voltage	V_{BUS_H}		3.0	—	—	V
Transmitter						
Output High Voltage	V_{OH}	V_{DD} ≥3.0V	2.8	—	—	V
Output Low Voltage	V_{OL}	V_{DD} ≥3.0V	—	—	0.8	V
Output Crossover Point	V_{CRS}		1.3	—	2.0	V
Output Impedance	Z_{DRV}	Driving High	—	38	—	Ω
		Driving Low	—	38	—	
Pull-up Resistance	R_{PU}	Full Speed (D+ Pull-up)	1.425	1.5	1.575	kΩ
		Low Speed (D- Pull-up)				
Output Rise Time	T_R	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Output Fall Time	T_F	Low Speed	75	—	300	ns
		Full Speed	4	—	20	ns
Receiver						V
Differential Input Sensitivity	V_{DI}	| (D+) - (D-) |	0.2	—	—	V
Differential Input Common Mode Range	V_{CM}		0.8	—	2.5	V
Input Leakage Current	I_L	Pullups Disabled	—	<1.0	—	µA
Refer to the USB Specification for timing diagrams and symbol definitions.						

4.1.15 SMBus

Table 4.15. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	70[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	µs
Data Hold Time	$t_{HD:DAT}$		0	—	—	µs
Data Setup Time	$t_{SU:DAT}$		4.7	—	—	µs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	µs
Clock High Period	t_{HIGH}		9.4	—	50[3]	µs
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	256[2]	kHz
SMBus Operating Frequency	f_{SMB}		40[1]	—	256[2]	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	µs
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	µs
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	µs
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	µs
Data Hold Time	$t_{HD:DAT}$		0	—	—	µs
Data Setup Time	$t_{SU:DAT}$		1.3	—	—	µs
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	µs
Clock High Period	t_{HIGH}		2.6	—	50[3]	µs

Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications.
3. SMBus has a maximum requirement of 50 µs for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 µs. I2C can support periods longer than 50 µs.

Table 4.16. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:
1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

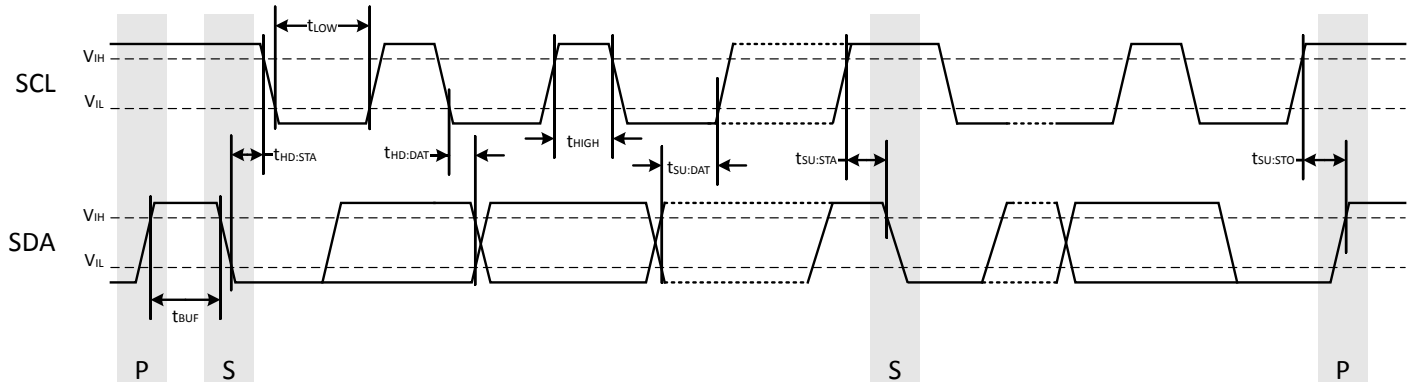


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.17. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFP48 Packages	—	60	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QFN32 Packages	—	28	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (bus-powered). The VBUS signal is used to detect when USB is connected to a host device.

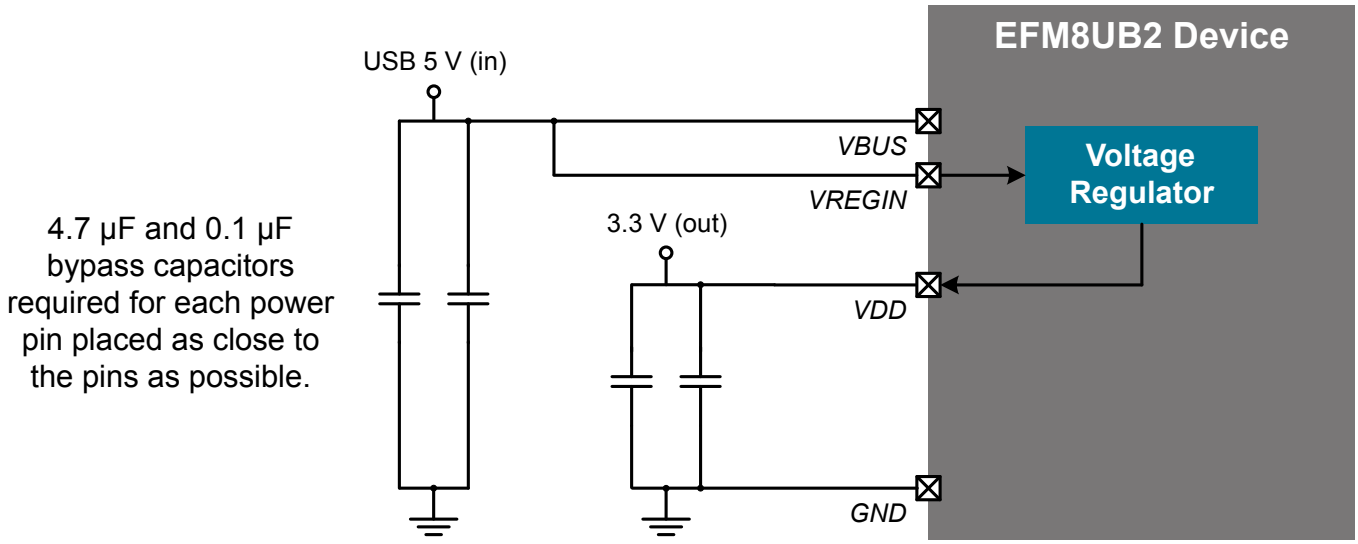


Figure 5.1. Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered)

Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal regulator used and USB is connected (self-powered). The VBUS signal is used to detect when USB is connected to a host device and is shown with a resistor divider. This resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification for self-powered systems where VDD and VIO may be unpowered when VBUS is connected to 5 V.

5.2 USB

Figure 5.4 Connection Diagram for USB Pins on page 26 shows a typical connection diagram for the USB pins of the EFM8UB2 devices including ESD protection diodes on the USB pins.

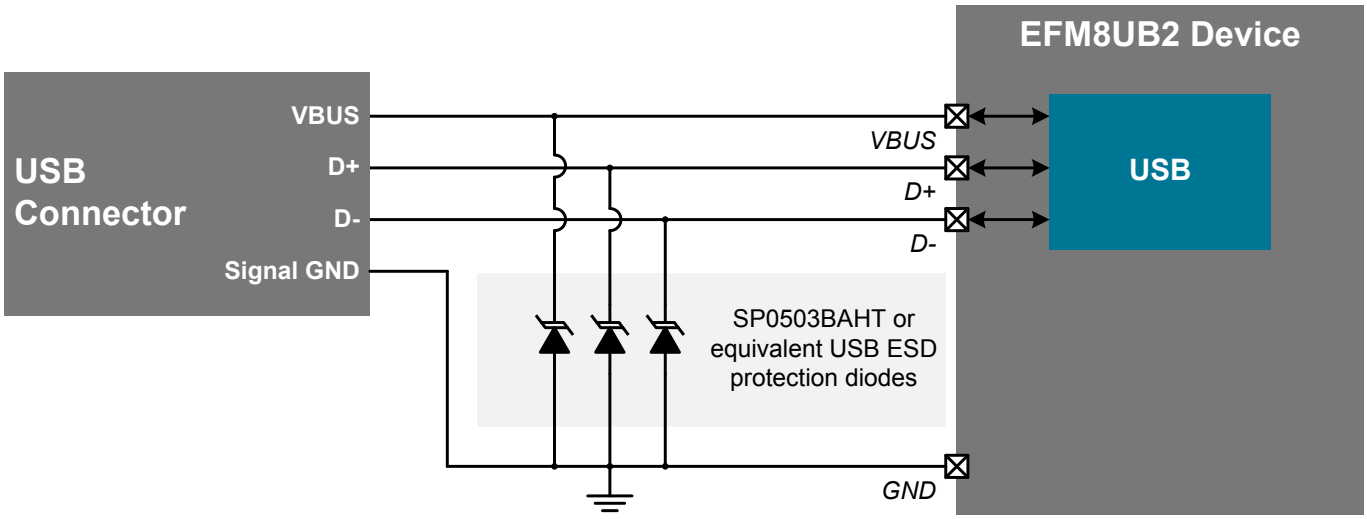


Figure 5.4. Connection Diagram for USB Pins

5.3 Voltage Reference (VREF)

Figure 5.5 Connection Diagram for Internal Voltage Reference on page 26 shows a typical connection diagram for the voltage reference (VREF) pin of the EFM8UB2 devices when using the internal voltage reference. When using an external voltage reference, consult the external reference data sheet for connection recommendations.

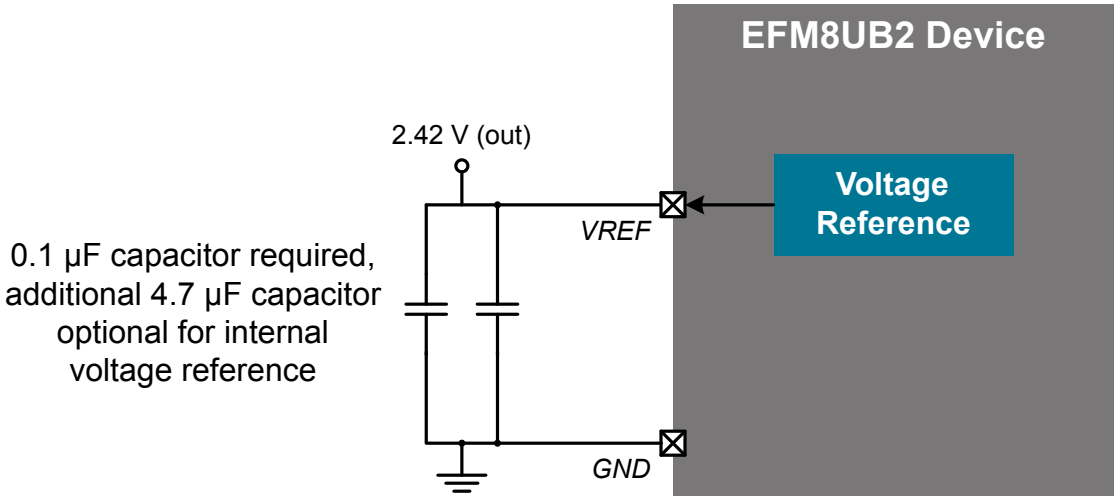


Figure 5.5. Connection Diagram for Internal Voltage Reference

6. Pin Definitions

6.1 EFM8UB2x-QFP48 Pin Definitions

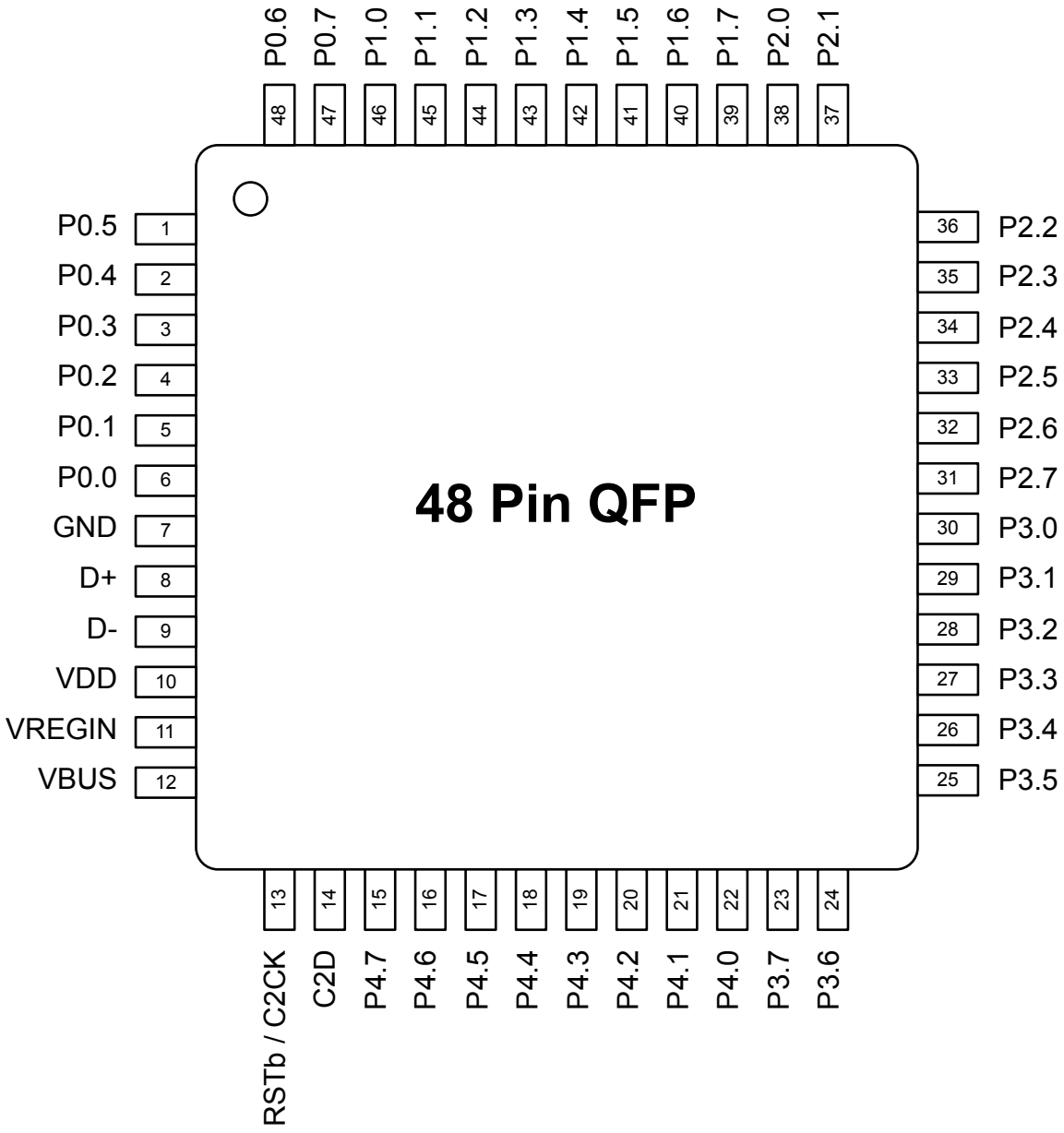


Figure 6.1. EFM8UB2x-QFP48 Pinout

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
47	P0.7	Multifunction I/O	Yes	XTAL2 EXTCLK INT0.7 INT1.7	
48	P0.6	Multifunction I/O	Yes	XTAL1 INT0.6 INT1.6	

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
5	D-	USB Data Negative			
6	VDD	Supply Power Input / 5V Regulator Output			
7	VREGIN	5V Regulator Input			
8	VBUS	USB VBUS Sense Input		VBUS	
9	RST / C2CK	Active-low Reset / C2 Debug Clock			
10	P3.0 / C2D	Multifunction I/O / C2 Debug Data	Yes		ADC0P.16 ADC0N.16
11	P2.7	Multifunction I/O	Yes		ADC0P.15 ADC0N.15
12	P2.6	Multifunction I/O	Yes		ADC0P.14 ADC0N.14
13	P2.5	Multifunction I/O	Yes		ADC0P.13 ADC0N.13 CMP0N.3
14	P2.4	Multifunction I/O	Yes		ADC0P.12 ADC0N.12 CMP0P.3
15	P2.3	Multifunction I/O	Yes		ADC0P.11 ADC0N.11 CMP1N.2
16	P2.2	Multifunction I/O	Yes		ADC0P.10 ADC0N.10 CMP1P.2
17	P2.1	Multifunction I/O	Yes		ADC0P.9 ADC0N.9 CMP0N.2
18	P2.0	Multifunction I/O	Yes		ADC0P.8 ADC0N.8 CMP0P.2
19	P1.7	Multifunction I/O	Yes		ADC0P.7 ADC0N.7 CMP1N.1

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
20	P1.6	Multifunction I/O	Yes		ADC0P.6 ADC0N.6 CMP1P.1
21	P1.5	Multifunction I/O	Yes		ADC0P.5 ADC0N.5 CMP0N.1
22	P1.4	Multifunction I/O	Yes		ADC0P.4 ADC0N.4 CMP0P.1
23	P1.3	Multifunction I/O	Yes		ADC0P.3 ADC0N.3 CMP1N.0
24	P1.2	Multifunction I/O	Yes		ADC0P.2 ADC0N.2 CMP1P.0
25	P1.1	Multifunction I/O	Yes		ADC0P.1 ADC0N.1 CMP0N.0
26	P1.0	Multifunction I/O	Yes		ADC0P.0 ADC0N.0 CMP0P.0
27	P0.7	Multifunction I/O	Yes	INT0.7 INT1.7	VREF
28	P0.6	Multifunction I/O	Yes	CNVSTR INT0.6 INT1.6	
29	P0.5	Multifunction I/O	Yes	INT0.5 INT1.5 UART0_RX	ADC0P.20 ADC0N.20 CMP1N.4
30	P0.4	Multifunction I/O	Yes	INT0.4 INT1.4 UART0_TX	ADC0P.19 ADC0N.19 CMP1P.4
31	P0.3	Multifunction I/O	Yes	EXTCLK INT0.3 INT1.3	

6.3 EFM8UB2x-QFN32 Pin Definitions

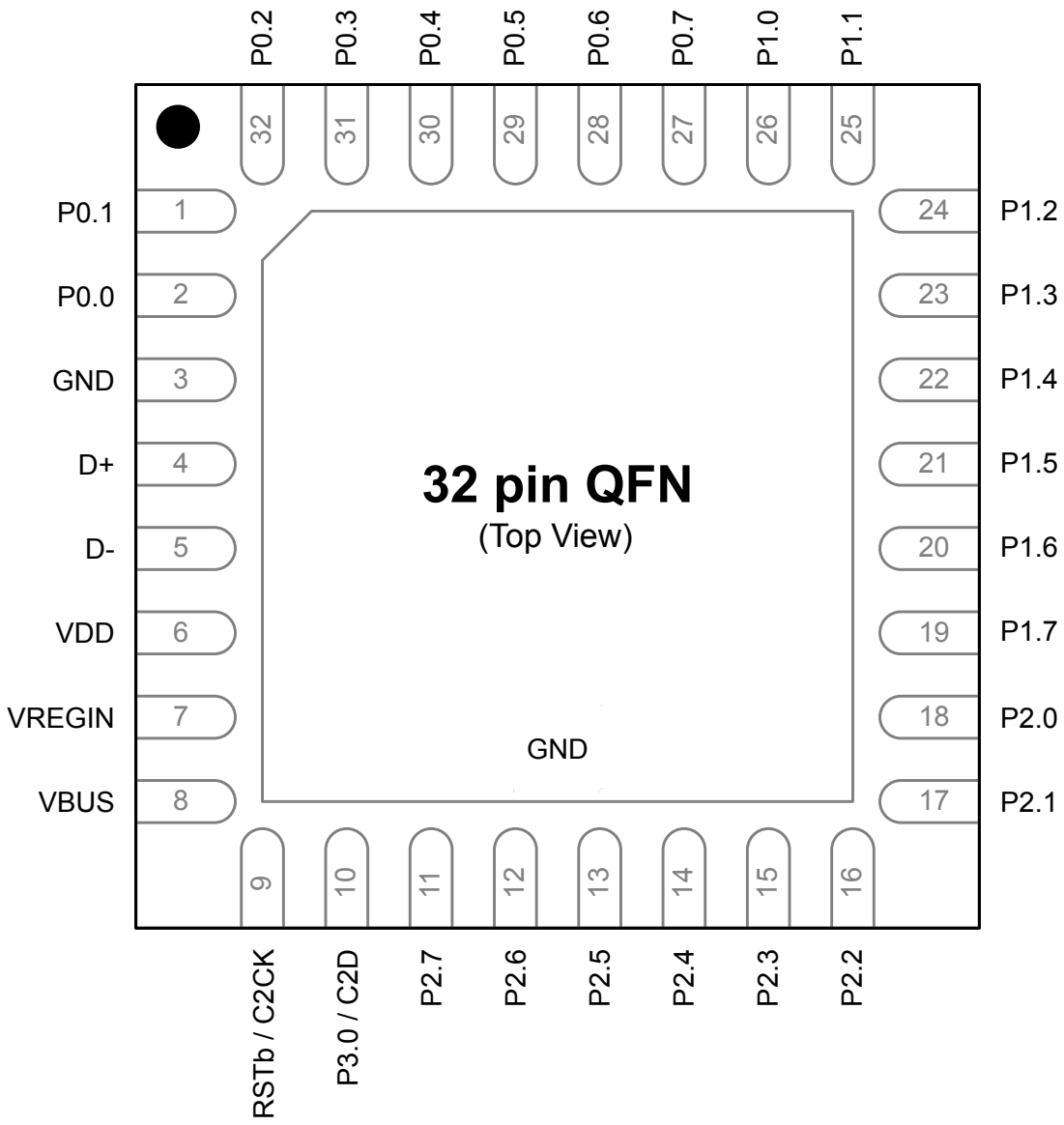


Figure 6.3. EFM8UB2x-QFN32 Pinout

Table 6.3. Pin Definitions for EFM8UB2x-QFN32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	ADC0P.18 ADC0N.18 CMP0N.4

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

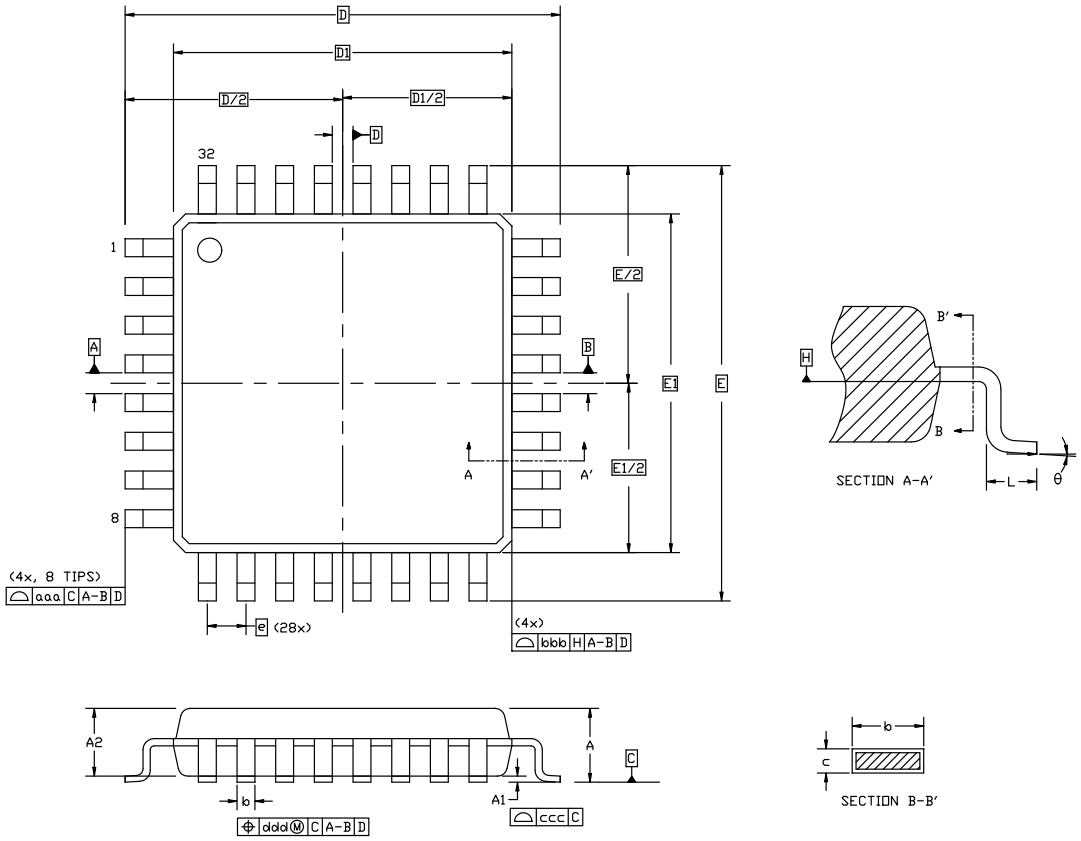


Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D		9.00 BSC	
D1		7.00 BSC	
e		0.80 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
aaa		0.20	

8.3 QFP32 Package Marking

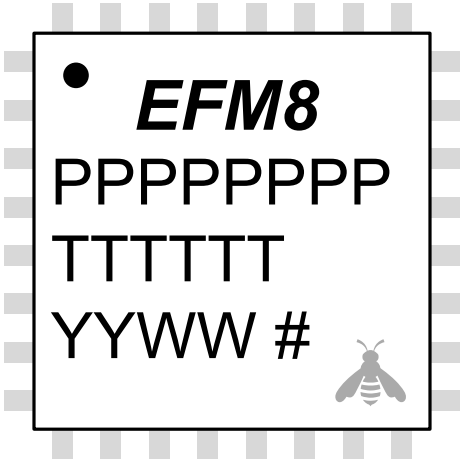
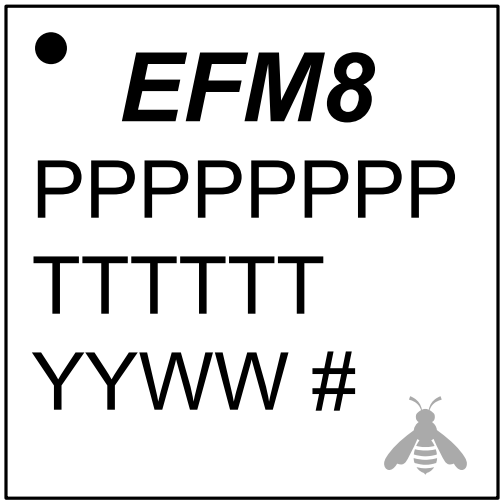


Figure 8.3. QFP32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9.3 QFN32 Package Marking



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