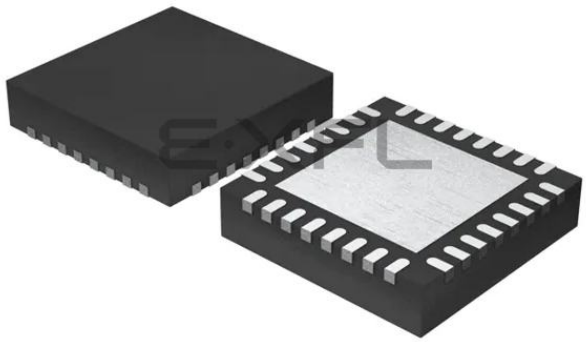

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SMBus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.65V ~ 3.6V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8ub20f64g-b-qfn32r

1. Feature List

The EFM8UB2 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 48 MHz maximum operating frequency
- Memory:
  - Up to 64 KB flash memory, in-system re-programmable from firmware.
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Internal 5-to-3.3 V LDO allows direct connection to USB supply net
  - Power-on reset circuit and brownout detectors
- I/O: Up to 40 total multifunction I/O pins:
  - Flexible peripheral crossbar for peripheral routing
  - 10 mA source, 25 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 48 MHz precision oscillator (±1.5% accuracy without USB clock recovery, ±0.25% accuracy with USB clock recovery)
  - Internal 80 kHz low-frequency oscillator
  - External crystal, RC, C, and CMOS clock options
- Timers/Counters and PWM:
  - 5-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes with watchdog timer function
  - 6 x 16-bit general-purpose timers
- Communications and Digital Peripherals:
  - Universal Serial Bus (USB) Function Controller with eight flexible endpoint pipes, integrated transceiver, and 1 KB FIFO RAM
  - 2 x UART
  - SPI™ Master / Slave
  - 2 x SMBus™/I2C™ Master / Slave
  - External Memory Interface (EMIF)
- Analog:
  - 10-Bit Analog-to-Digital Converter (ADC0)
  - 2 x Low-current analog comparators
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded USB bootloader
- Temperature range -40 to 85 ºC
- Single power supply 2.65 to 3.6 V
- QFP48, QFP32, and QFN32 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.65 to 3.6 V operation and is available in 32-pin QFN, 32-pin QFP, or 48-pin QFP packages. All package options are lead-free and RoHS compliant.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Up to five independently-configurable channels
- 8- or 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- USB start-of-frame or falling edge of LFOSC0 capture (Timer 2 and Timer 3)

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

System Management Bus / I2C (SMB0 and SMB1)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus.

The SMBus modules include the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

External Memory Interface (EMIF0)

The External Memory Interface (EMIF) enables access of off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either 8-bit or 16-bit formats.

- Supports multiplexed and non-multiplexed memory access.
- Four external memory modes:
  - Internal only.
  - Split mode without bank select.
  - Split mode with bank select.
  - External only
- Configurable ALE (address latch enable) timing.
- Configurable address setup and hold times.
- Configurable write and read pulse widths.

3.7 Analog

10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 10-bit mode, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

The ADC module is a Successive Approximation Register (SAR) Analog to Digital Converter (ADC). The key features of this ADC module are:

- Up to 32 external inputs.
- Differential or Single-ended 10-bit operation.
- Supports an output update rate of 500 ksps samples per second.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Two tracking mode options with programmable tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Voltage reference selectable from external reference pin, on-chip precision reference (driven externally on reference pin), or VDD supply.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 5 external positive inputs.
- Up to 5 external negative inputs.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and +/-20 mV.
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- USB reset

3.9 Debugging

The EFM8UB2 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QFN48	P3.7
QFP32	P3.0 / C2D
QFN32	P3.0 / C2D

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from regulators, supply monitor, and High Frequency Oscillator.
3. Includes supply current from regulators, supply monitor, and Low Frequency Oscillator.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}		2.60	2.65	2.70	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t_{RMP}	Time to V_{DD} > 2.7 V	—	—	1	ms
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	—	250	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} >1 MHz	80	580	800	µs
VDD Supply Monitor Turn-On Time	t_{MON}		—	—	100	µs

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1]	t_{WRITE}	One Byte	10	15	20	µs
Erase Time[1]	t_{ERASE}	One Page	10	15	22.5	ms
V_{DD} Voltage During Programming[2]	V_{PROG}		2.7	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		10k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block SYSCLK = 48 MHz	—	5.5	—	µs

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
3. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.11 5 V Voltage Regulator

Table 4.11. 5V Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range[1]	V_{REGIN}		2.7	—	5.25	V
Output Voltage on VDD[2]	V_{REGOUT}	Output Current = 1 to 100 mA	3.0	3.3	3.6	V
Output Current[2]	I_{REGOUT}		—	—	100	mA

Note:
1. Input range specified for regulation. When an external regulator is used, VREGIN should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V_{IN}		-0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	60	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	60	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV

4.1.13 Port I/O

Table 4.13. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage	V_{OH}	I_{OH} = -3 mA	V_{DD} - 0.7	—	—	V
		I_{OH} = -10 µA	V_{DD} - 0.1	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
		I_{OL} = 10 µA	—	—	0.1	V
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Pin Capacitance	C_{IO}		—	7	—	pF
Weak Pull-Up Current (V_{IN} = 0 V)	I_{PU}	V_{DD} = 3.6	-50	-15	—	µA
Input Leakage (Pullups off or Analog)	I_{LK}	GND < V_{IN} < V_{DD}	-1	—	1	µA
Input Leakage Current with V_{IN} above V_{DD}	I_{LK}	V_{DD} < V_{IN} < V_{DD}+2.0 V	0	5	150	µA

Table 4.16. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	f_{CSO} / 3
Bus Free Time Between STOP and START Conditions	t_{BUF}	2 / f_{CSO}
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	1 / f_{CSO}
Repeated START Condition Setup Time	$t_{SU:STA}$	2 / f_{CSO}
STOP Condition Setup Time	$t_{SU:STO}$	2 / f_{CSO}
Clock Low Period	t_{LOW}	1 / f_{CSO}
Clock High Period	t_{HIGH}	2 / f_{CSO}

Note:
1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

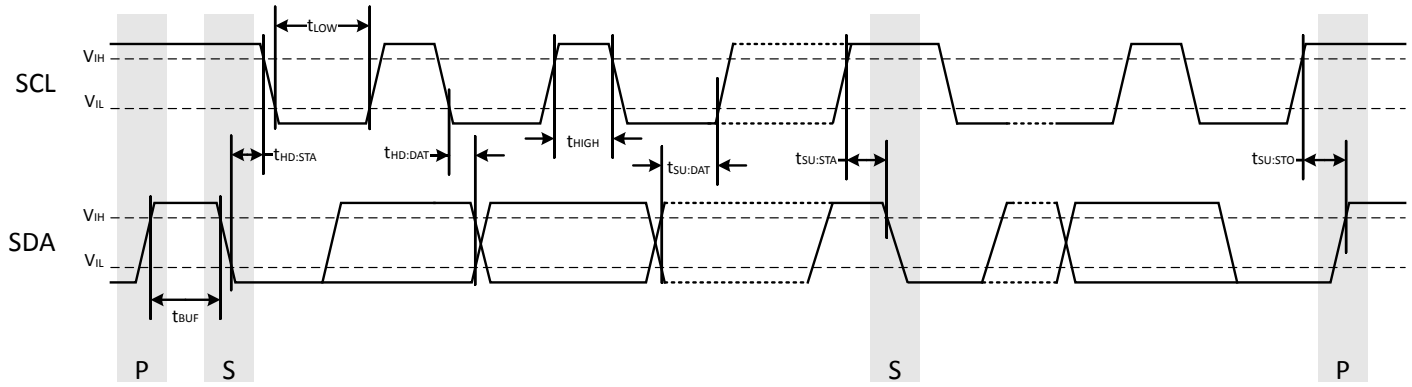

Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.17. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	θ_{JA}	QFP48 Packages	—	60	—	°C/W
		QFP32 Packages	—	80	—	°C/W
		QFN32 Packages	—	28	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

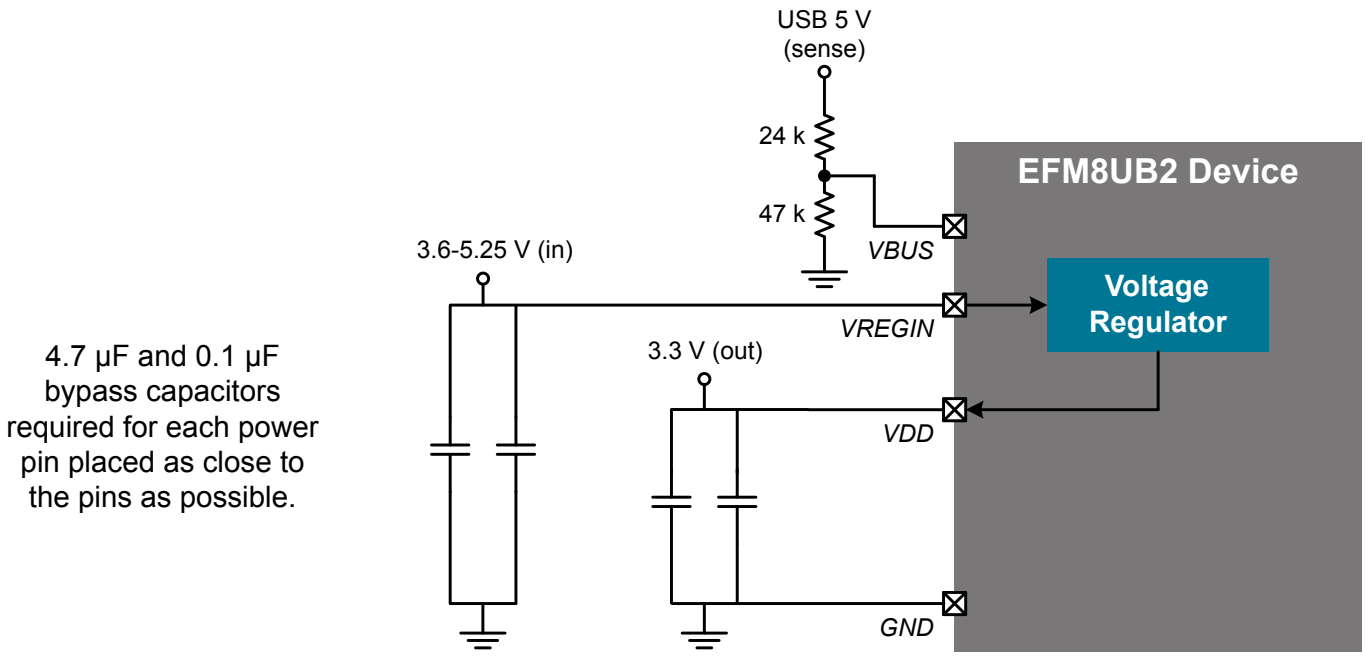

Figure 5.2. Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered)

The figure below shows a typical connection diagram for the power pins of the EFM8UB2 devices when the internal 5 V-to-3.3 V regulator is not used.

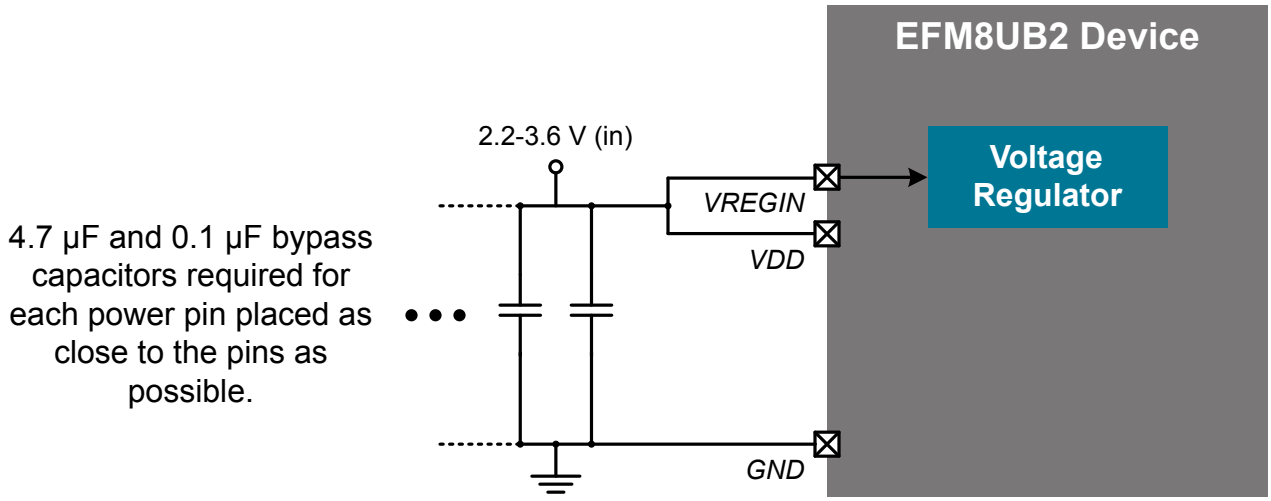

Figure 5.3. Connection Diagram with Voltage Regulator Not Used

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P4.4	Multifunction I/O		EMIF_D4 EMIF_AD4m	ADC0P.13 ADC0N.13 CMP0N.3
19	P4.3	Multifunction I/O		EMIF_D3 EMIF_AD3m	ADC0P.12 ADC0N.12 CMP0P.3
20	P4.2	Multifunction I/O		EMIF_D2 EMIF_AD2m	ADC0P.33 ADC0N.33
21	P4.1	Multifunction I/O		EMIF_D1 EMIF_AD1m	ADC0P.32 ADC0N.32
22	P4.0	Multifunction I/O		EMIF_D0 EMIF_AD0m	ADC0P.11 ADC0N.11 CMP1N.2
23	P3.7	Multifunction I/O	Yes	EMIF_A7 EMIF_A15m	ADC0P.10 ADC0N.10 CMP1P.2
24	P3.6	Multifunction I/O	Yes	EMIF_A6 EMIF_A14m	ADC0P.29 ADC0N.29
25	P3.5	Multifunction I/O	Yes	EMIF_A5 EMIF_A13m	ADC0P.9 ADC0N.9 CMP0N.2
26	P3.4	Multifunction I/O	Yes	EMIF_A4 EMIF_A12m	ADC0P.8 ADC0N.8 CMP0P.2
27	P3.3	Multifunction I/O	Yes	EMIF_A3 EMIF_A11m	ADC0P.28 ADC0N.28
28	P3.2	Multifunction I/O	Yes	EMIF_A2 EMIF_A10m	ADC0P.27 ADC0N.27
29	P3.1	Multifunction I/O	Yes	EMIF_A1 EMIF_A9m	ADC0P.7 ADC0N.7 CMP1N.1
30	P3.0	Multifunction I/O	Yes	EMIF_A0 EMIF_A8m	ADC0P.6 ADC0N.6 CMP1P.1
31	P2.7	Multifunction I/O	Yes	EMIF_A15	ADC0P.26 ADC0N.26

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
32	P2.6	Multifunction I/O	Yes	EMIF_A14	ADC0P.5 ADC0N.5 CMP0N.1
33	P2.5	Multifunction I/O	Yes	EMIF_A13	ADC0P.4 ADC0N.4 CMP0P.1
34	P2.4	Multifunction I/O	Yes	EMIF_A12	ADC0P.25 ADC0N.25
35	P2.3	Multifunction I/O	Yes	EMIF_A11	ADC0P.3 ADC0N.3 CMP1N.0
36	P2.2	Multifunction I/O	Yes	EMIF_A10	ADC0P.2 ADC0N.2 CMP1P.0
37	P2.1	Multifunction I/O	Yes	EMIF_A9	ADC0P.1 ADC0N.1 CMP0N.0
38	P2.0	Multifunction I/O	Yes	EMIF_A8	ADC0P.0 ADC0N.0 CMP0P.0
39	P1.7	Multifunction I/O	Yes	EMIF_WRb	ADC0P.24 ADC0N.24
40	P1.6	Multifunction I/O	Yes	EMIF_RDb	ADC0P.23 ADC0N.23
41	P1.5	Multifunction I/O	Yes		VREF
42	P1.4	Multifunction I/O	Yes	CNVSTR	
43	P1.3	Multifunction I/O	Yes	EMIF_ALEm	ADC0P.22 ADC0N.22
44	P1.2	Multifunction I/O	Yes		ADC0P.20 ADC0N.20 CMP1N.4
45	P1.1	Multifunction I/O	Yes		ADC0P.19 ADC0N.19 CMP1P.4
46	P1.0	Multifunction I/O	Yes		ADC0P.21 ADC0N.21

6.2 EFM8UB2x-QFP32 Pin Definitions

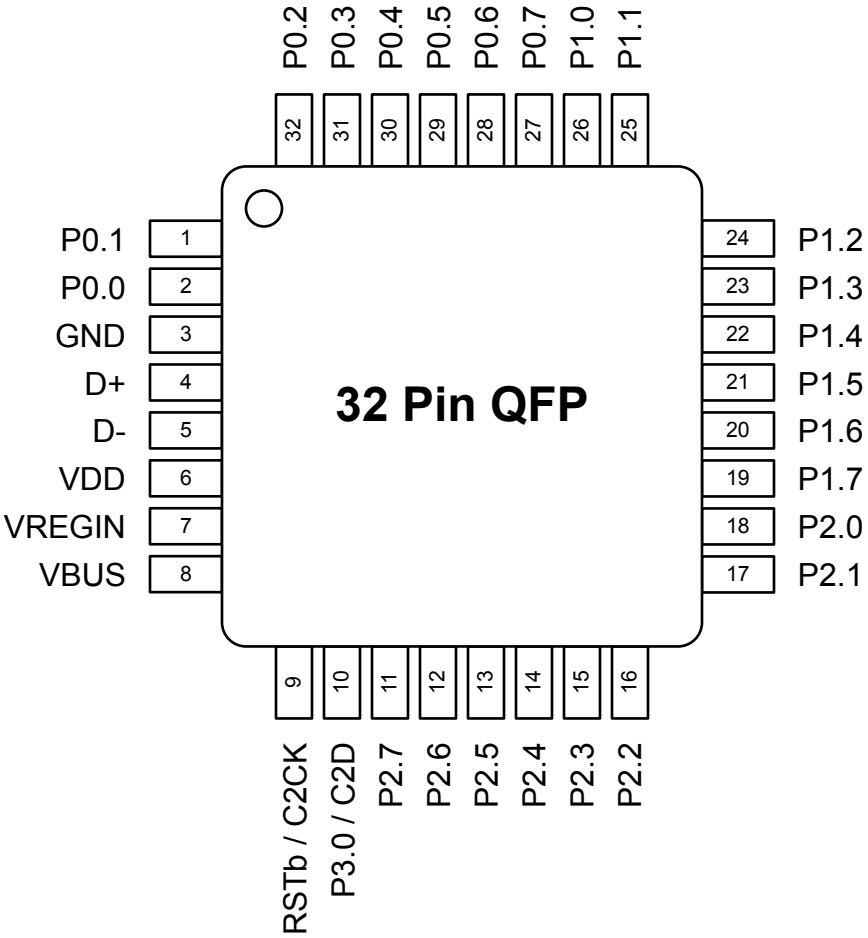

Figure 6.2. EFM8UB2x-QFP32 Pinout

Table 6.2. Pin Definitions for EFM8UB2x-QFP32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	INT0.1 INT1.1	ADC0P.18 ADC0N.18 CMP0N.4
2	P0.0	Multifunction I/O	Yes	INT0.0 INT1.0	ADC0P.17 ADC0N.17 CMP0P.4
3	GND	Ground			
4	D+	USB Data Positive			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
18	P2.0	Multifunction I/O	Yes		ADC0P.8 ADC0N.8 CMP0P.2
19	P1.7	Multifunction I/O	Yes		ADC0P.7 ADC0N.7 CMP1N.1
20	P1.6	Multifunction I/O	Yes		ADC0P.6 ADC0N.6 CMP1P.1
21	P1.5	Multifunction I/O	Yes		ADC0P.5 ADC0N.5 CMP0N.1
22	P1.4	Multifunction I/O	Yes		ADC0P.4 ADC0N.4 CMP0P.1
23	P1.3	Multifunction I/O	Yes		ADC0P.3 ADC0N.3 CMP1N.0
24	P1.2	Multifunction I/O	Yes		ADC0P.2 ADC0N.2 CMP1P.0
25	P1.1	Multifunction I/O	Yes		ADC0P.1 ADC0N.1 CMP0N.0
26	P1.0	Multifunction I/O	Yes		ADC0P.0 ADC0N.0 CMP0P.0
27	P0.7	Multifunction I/O	Yes	INT0.7 INT1.7	VREF
28	P0.6	Multifunction I/O	Yes	CNVSTR INT0.6 INT1.6	
29	P0.5	Multifunction I/O	Yes	INT0.5 INT1.5 UART0_RX	ADC0P.20 ADC0N.20 CMP1N.4

8. QFP32 Package Specifications

8.1 QFP32 Package Dimensions

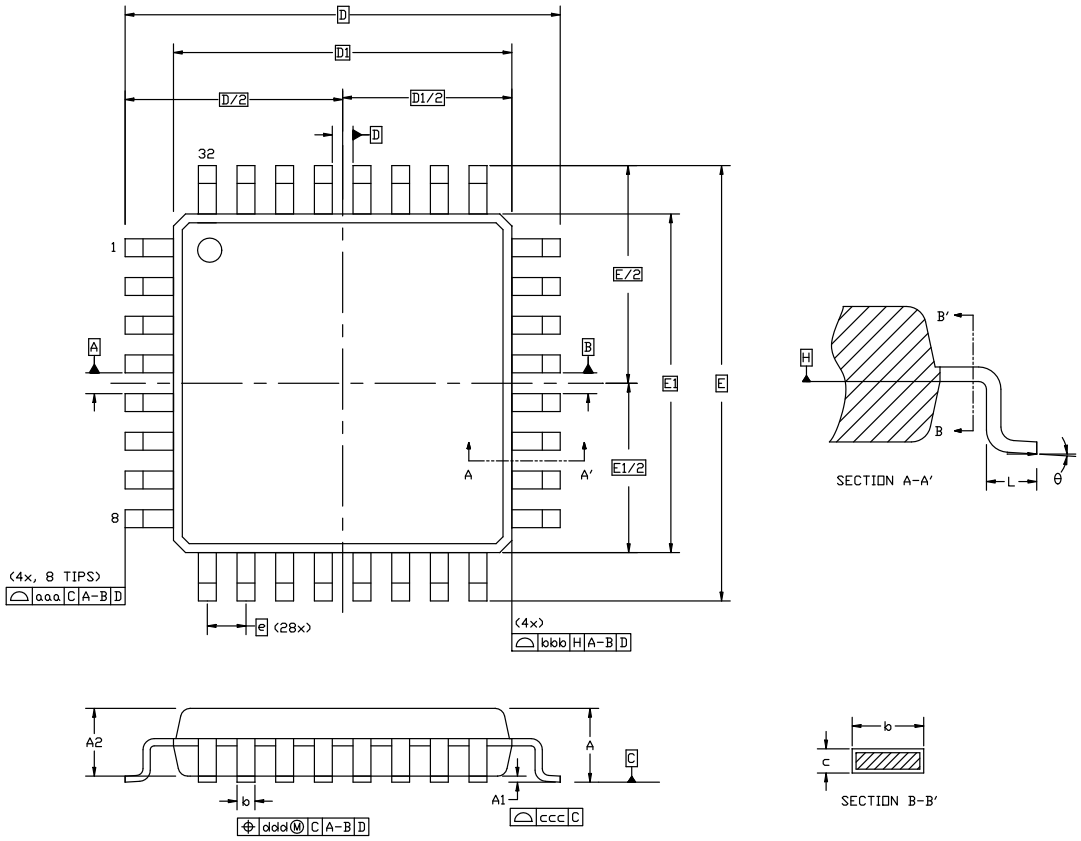

Figure 8.1. QFP32 Package Drawing

Table 8.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D		9.00 BSC	
D1		7.00 BSC	
e		0.80 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
aaa		0.20	

8.2 QFP32 PCB Land Pattern

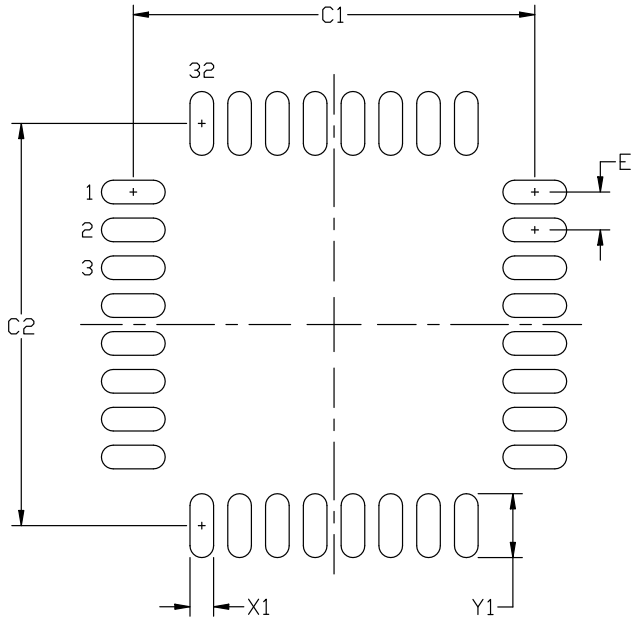

Figure 8.2. QFP32 PCB Land Pattern Drawing

Table 8.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.2 QFN32 PCB Land Pattern

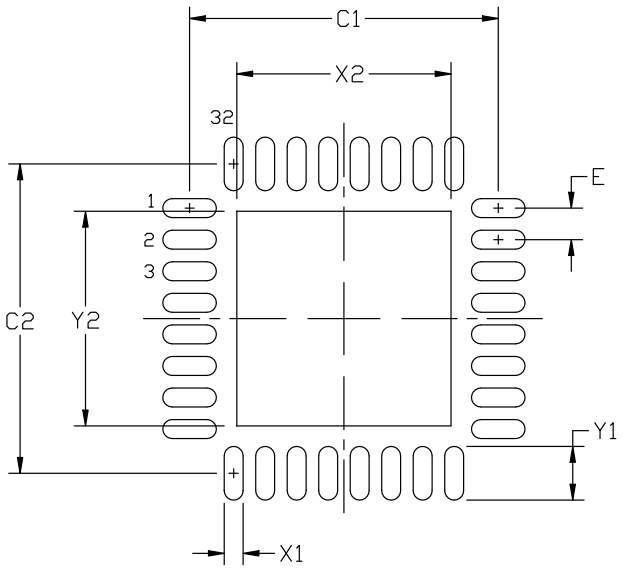

Figure 9.2. QFN32 PCB Land Pattern Drawing

Table 9.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.3 QFN32 Package Marking

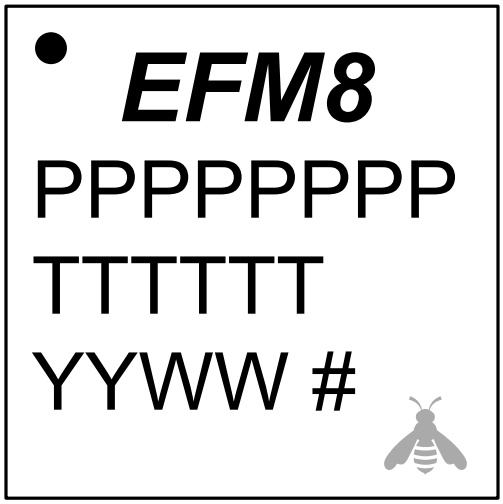

Figure 9.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. Revision History

10.1 Revision 1.3

Updated ordering part numbers to revision B.

Added Power-On Reset Threshold and Reset Delay from POR specifications to 4.1.3 Reset and Supply Monitor.

Added CRC Calculation Time specification to 4.1.4 Flash Memory.

Added VBUS Detection Input High Voltage and VBUS Detection Input Low Voltage specifications to Table 4.14 USB Transceiver on page 20.

Added specifications for 4.1.15 SMBus.

Added 5.4 Debug.

Added information about bootloader implementation and bootloader pinout to 3.10 Bootloader.

Added notes to Table 6.3 Pin Definitions for EFM8UB2x-QFN32 on page 37 and Table 6.2 Pin Definitions for EFM8UB2x-QFP32 on page 33 to clarify that XTAL1 and XTAL2 are not available on the 32-pin packages.

Updated Figure 5.1 Connection Diagram with Voltage Regulator Used and USB Connected (Bus-Powered) on page 24 and Figure 5.2 Connection Diagram with Voltage Regulator Used and USB Connected (Self-Powered) on page 25 to recommend 4.7 µF capacitors instead of 1.0 µF capacitors.

Added text and Figure 5.3 Connection Diagram with Voltage Regulator Not Used on page 25 to demonstrate the proper connections when the regulator is not used.

Added reference to the Reference Manual in 3.1 Introduction.

10.2 Revision 1.2

Updated the VDD Ramp Time specification in Table 4.3 Reset and Supply Monitor on page 13 to a maximum of 1 ms.

10.3 Revision 1.1

Initial release.