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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l100rct6tr

Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lxxxxx and STM32Lxxxxx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, your old applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx, STM32L15xxx and STM32L162xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy.

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx and STM32L162xx family uses a common architecture:

- Same power supply range from 1.65 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 15 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 2 to 512 Kbytes

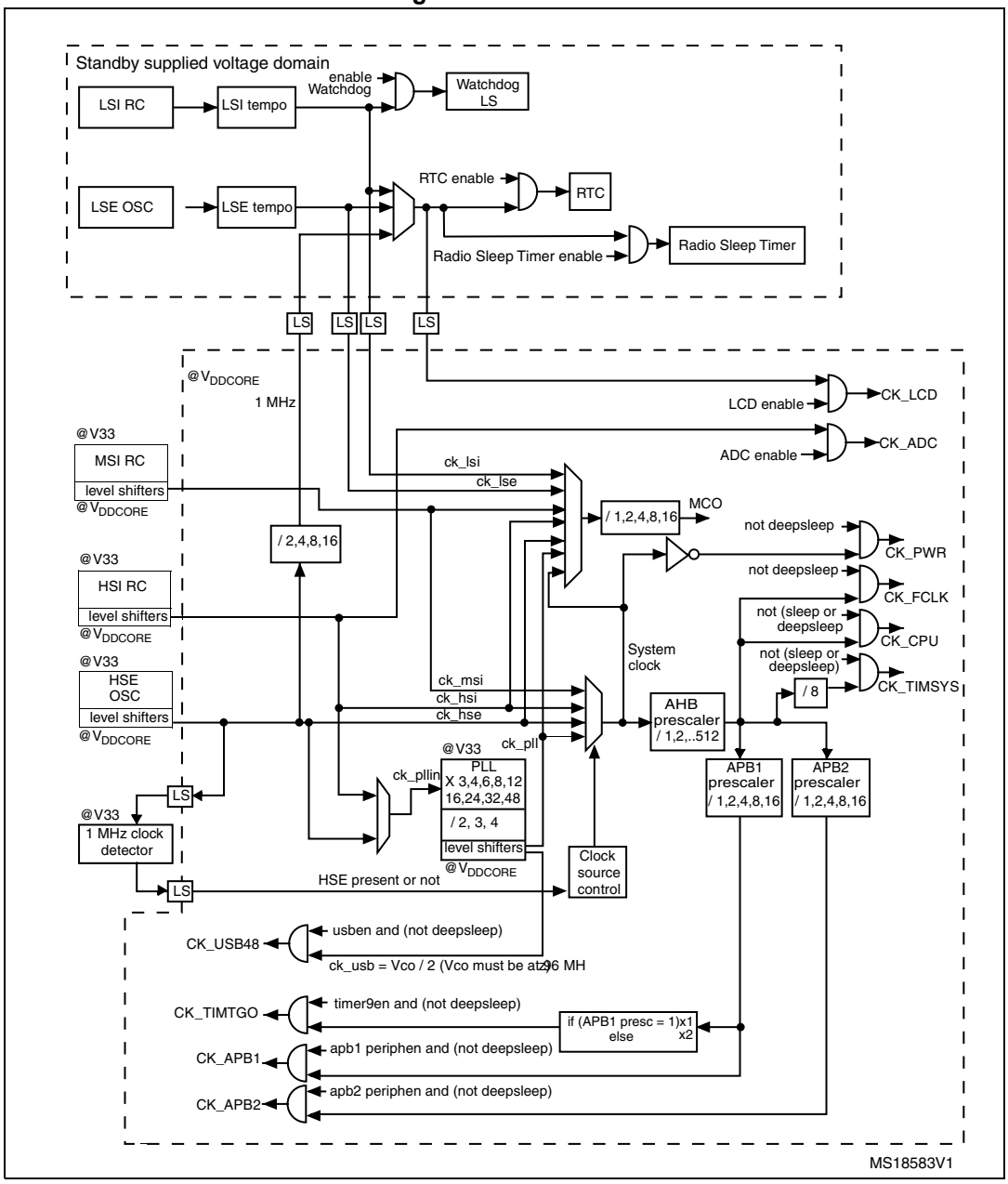
3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**: three different clock sources can be used to drive the master clock SYSCLK:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



1. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 24 MHz or 32 MHz.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels, independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L100RC device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L100RC device embeds two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.14.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.14.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.15 Communication interfaces

3.15.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

The three USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They support IrDA SIR ENDEC and have LIN Master/Slave capability. The three USARTs provide hardware management of the CTS and RTS signals and are ISO 7816 compliant.

All USART interfaces can be served by the DMA controller.

Table 7. STM32L100RC pin definitions (continued)

Pins	Pin name	Type(1)	I / O Level(2)	Main function (after reset)	Pin functions	
LQFP64					Alternate functions	Additional functions
17	PA3	I/O	-	PA3	TIM2_CH4/TIM9_CH2 /USART2_RX/LCD_SEG2	ADC_IN3/ COMP1_INP/OPAMP1_VOUT
18	V_{SS_4}	S	-	V_{SS_4}	-	-
19	V_{DD_4}	S	-	V_{DD_4}	-	-
20	PA4	I/O	-	PA4	SPI1_NSS/SPI3_NSS/ I2S3_WS/USART2_CK	ADC_IN4/DAC_OUT1/ COMP1_INP
21	PA5	I/O	-	PA5	TIM2_CH1_ETR/SPI1_SCK	ADC_IN5/ DAC_OUT2/COMP1_INP
22	PA6	I/O	FT	PA6	TIM3_CH1/TIM10_CH1/ SPI1_MISO/LCD_SEG3	ADC_IN6/COMP1_INP/ OPAMP2_VINP
23	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/LCD_SEG4	ADC_IN7/COMP1_INP /OPAMP2_VINM
24	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/COMP1_INP
25	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/COMP1_INP
26	PB0	I/O	-	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/COMP1_INP/ OPAMP2_VOUT/VREF_OUT
27	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/VREF_OUT
28	PB2	I/O	FT	PB2/BOOT1	BOOT1	COMP1_INP
29	PB10	I/O	FT	PB10	TIM2_CH3/I2C2_SCL/ USART3_TX/LCD_SEG10	-
30	PB11	I/O	FT	PB11	TIM2_CH4/I2C2_SDA/ USART3_RX/LCD_SEG11	-
31	V_{SS_1}	S	-	V_{SS_1}	-	-
32	V_{DD_1}	S	-	V_{DD_1}	-	-
33	PB12	I/O	FT	PB12	TIM10_CH1/I2C2_SMBA/ SPI2_NSS/I2S2_WS/ USART3_CK/LCD_SEG12	ADC_IN18/COMP1_INP
34	PB13	I/O	FT	PB13	TIM9_CH1/SPI2_SCK/ I2S2_CK/ USART3_CTS/ LCD_SEG13	ADC_IN19/COMP1_INP
35	PB14	I/O	FT	PB14	TIM9_CH2/SPI2_MISO/ USART3_RTS/LCD_SEG14	ADC_IN20/COMP1_INP

Table 7. STM32L100RC pin definitions (continued)

Pins	Pin name	Type(1)	I / O Level(2)	Main function (after reset)	Pin functions	
LQFP64					Alternate functions	Additional functions
36	PB15	I/O	FT	PB15	TIM11_CH1/SPI2_MOSI/ I2S2_SD/LCD_SEG15	ADC_IN21/COMP1_INP/ RTC_REFIN
37	PC6	I/O	FT	PC6	TIM3_CH1/I2S2_MCK/ LCD_SEG24	-
38	PC7	I/O	FT	PC7	TIM3_CH2/I2S3_MCK/ LCD_SEG25	-
39	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
40	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-
41	PA8	I/O	FT	PA8	USART1_CK/MCO/ LCD_COM0	-
42	PA9	I/O	FT	PA9	USART1_TX/LCD_COM1	-
43	PA10	I/O	FT	PA10	USART1_RX/LCD_COM2	-
44	PA11	I/O	FT	PA11	USART1_CTS/SPI1_MISO	USB_DM
45	PA12	I/O	FT	PA12	USART1_RTS/SPI1_MOSI	USB_DP
46	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
47	V_{SS_2}	S		V_{SS_2}	-	-
48	V_{DD_2}	S		V_{DD_2}	-	-
49	PA14	I/O	FT	JTCK-SWCLK	JTCK-SWCLK	-
50	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/SPI1_NSS/ SPI3_NSS/ I2S3_WS/LCD_SEG17/JTDI	-
51	PC10	I/O	FT	PC10	SPI3_SCK/I2S3_CK/ USART3_TX/LCD_SEG28/ LCD_SEG40/LCD_COM4	-
52	PC11	I/O	FT	PC11	SPI3_MISO/USART3_RX/ LCD_SEG29 /LCD_SEG41/LCD_COM5	-
53	PC12	I/O	FT	PC12	SPI3_MOSI/I2S3_SD/ USART3_CK/LCD_SEG30/ LCD_SEG42/LCD_COM6	-
54	PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31/ LCD_SEG43/LCD_COM7	-

Alternate functions

Table 8. Alternate function input/output

Port name	Digital alternate function number												
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function												
	SYSTEM	TIM2	TIM3/4	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3		LCD		CPRI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-		-		-	EVENT OUT
NRST	NRST	-	-	-	-	-	-	-		-		-	-
PA0-WKUP1	-	TIM2_CH1_ETR	-	-	-	-	-	USART2_CTS		-		TIMx_IC1	EVENT OUT
PA1	-	TIM2_CH2	-	-	-	-	-	USART2_RTS		SEG0		TIMx_IC2	EVENT OUT
PA2	-	TIM2_CH3	-	TIM9_CH1	-	-	-	USART2_TX		SEG1		TIMx_IC3	EVENT OUT
PA3	-	TIM2_CH4	-	TIM9_CH2	-	-	-	USART2_RX		SEG2		TIMx_IC4	EVENT OUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK		-		TIMx_IC1	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-		-		TIMx_IC2	EVENT OUT
PA6	-	-	TIM3_CH1	TIM10_ CH1	-	SPI1_MISO	-	-		SEG3		TIMx_IC3	EVENT OUT
PA7	-	-	TIM3_CH2	TIM11_ CH1	-	SPI1_MOSI	-	-		SEG4		TIMx_IC4	EVENT OUT
PA8	MCO	-	-	-	-	-	-	USART1_CK		COM0		TIMx_IC1	EVENT OUT
PA9	-	-	-	-	-	-	-	USART1_TX		COM1		TIMx_IC2	EVENT OUT
PA10	-	-	-	-	-	-	-	USART1_RX		COM2		TIMx_IC3	EVENT OUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS		-		TIMx_IC4	EVENT OUT

5 Memory mapping

Figure 4. Memory map

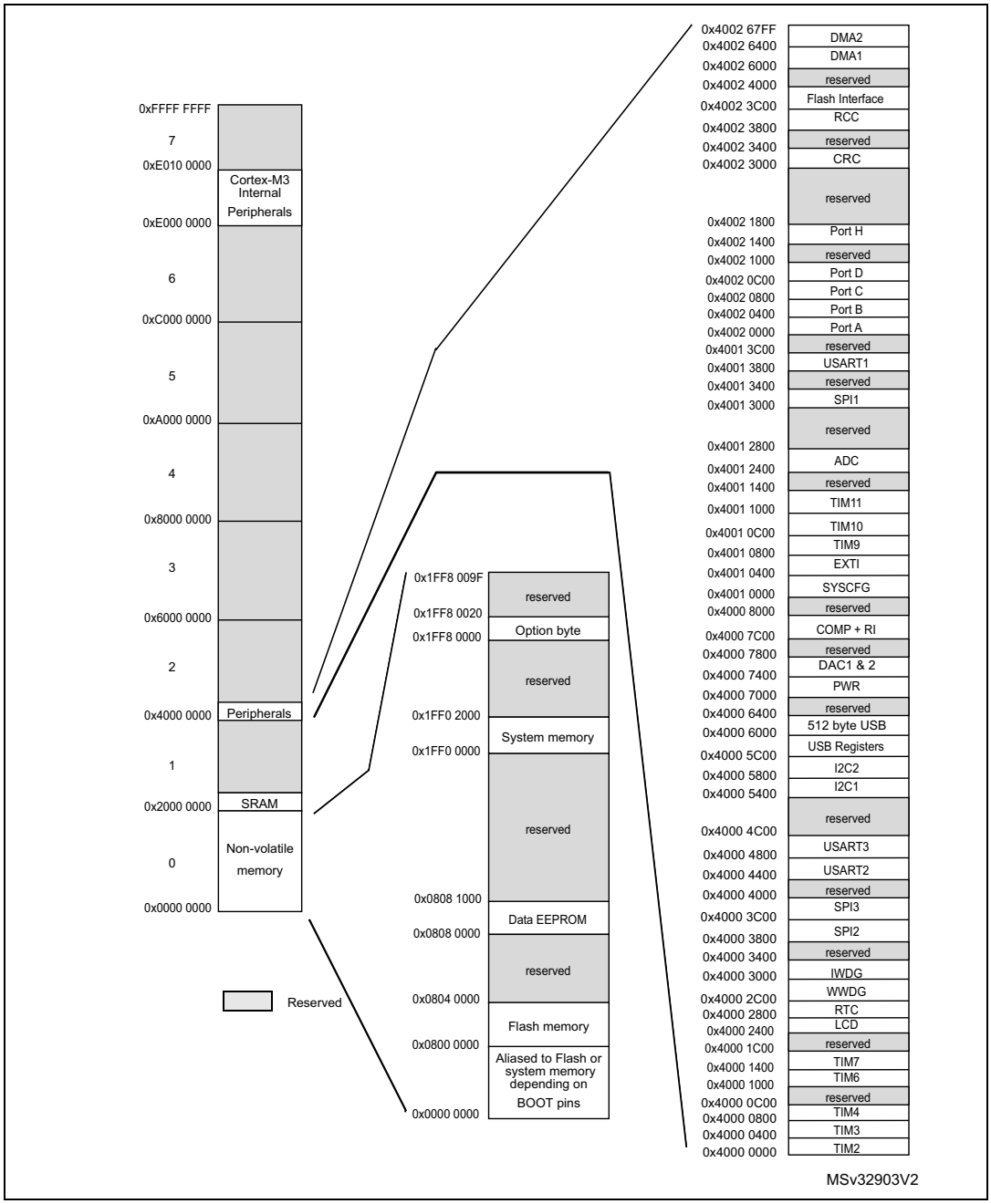


Table 18. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	50	130	µA
				2 MHz	78.5	195	
				4 MHz	140	310	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	165	310	
				8 MHz	310	440	
				16 MHz	590	830	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	350	550	
				16 MHz	680	990	
				32 MHz	1600	2100	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	640	890	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1600	2200	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	19	60	
		MSI clock, 524 kHz		524 kHz	33	99	
		MSI clock, 4.2 MHz		4.2 MHz	145	210	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	60.5	130	
				2 MHz	89.5	190	
				4 MHz	150	320	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	180	320	
				8 MHz	320	460	
				16 MHz	605	840	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	380	540	
				16 MHz	695	1000	
				32 MHz	1600	2100	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	650	910	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1600	2200	
	Supply current in Sleep mode, Flash ON	MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	30	90	
		MSI clock, 524 kHz		524 kHz	44	96	
		MSI clock, 4.2 MHz		4.2 MHz	155	220	

1. Guaranteed by characterization results, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

6.3.7 Internal clock source characteristics

The parameters given in *Table 29* are derived from tests performed under the conditions summarized in *Table 12*.

High-speed internal (HSI) RC oscillator

Table 29. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	±0.4	0.7	%
		Trimming code is a multiple of 16	-	-	±1.5	%
$ACC_{HSI}^{(2)}$	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI)}^{(2)}$	HSI oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI)}^{(2)}$	HSI oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by test in production.

Low-speed internal (LSI) RC oscillator

Table 30. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{LSI}^{(2)}$	LSI oscillator frequency drift 0°C ≤T_A ≤105°C	-10	-	4	%
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design, not tested in production.

Table 31. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{STAB(MSI)}$ (2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results, not tested in production.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 47* are derived from tests performed under the conditions summarized in *Table 12*. All I/Os are CMOS and TTL compliant.

Table 41. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC and FT I/O	-	-	0.3 V_{DD}(1)(2)	V
		BOOT0	-	-	0.14 V_{DD}(2)	
V_{IH}	Input high level voltage	TC I/O	0.45 V_{DD}+0.38(2)	-	-	
		FT I/O	0.39 V_{DD}+0.59(2)	-	-	
		BOOT0	0.15 V_{DD}+0.56(2)	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	TC and FT I/O	-	10% V_{DD}(3)	-	
		BOOT0	-	0.01	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB	-	-	±250	
		$V_{SS} \le V_{IN} \le V_{DD}$ TC and FT I/Os	-	-	±50	
		FT I/O $V_{DD} \le V_{IN} \le 5V$	-	-	±10	µA
R_{PU}	Weak pull-up equivalent resistor(5)(1)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by test in production
2. Guaranteed by design, not tested in production.
3. With a minimum of 200 mV.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA with the non-standard V_{OL}/V_{OH} specifications given in *Table 42*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD(\Sigma)}$ (see *Table 10*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $I_{VSS(\Sigma)}$ (see *Table 10*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under the conditions summarized in *Table 12*. All I/Os are CMOS and TTL compliant.

Table 42. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(2)	Output low level voltage for an I/O pin	I_{IO} = 8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)(3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL} (3)(4)	Output low level voltage for an I/O pin	I_{IO} = 4 mA 1.65 V < V_{DD} < 3.6 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = 20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 10* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. Guaranteed by test in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 10* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results, not tested in production.

Table 51. USB: full speed electrical characteristics (continued)

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

I2S characteristics

Table 52. I2S characteristics

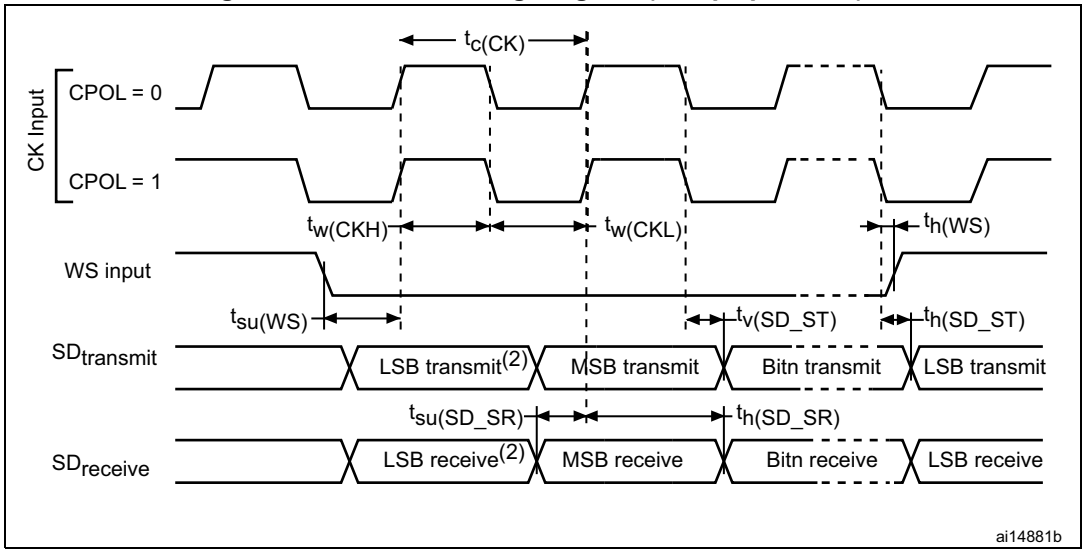
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main Clock Output		256 x 8K	256xFs (1)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver, 48KHz	30	70	%
$t_{r(CK)}$	I2S clock rise time	Capacitive load CL=30pF	-	8	ns
$t_{f(CK)}$	I2S clock fall time			8	
$t_{v(WS)}$	WS valid time	Master mode	4	24	
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	15	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	8	-	
$t_{su(SD\_SR)}$	Data input setup time	Slave receiver	9	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_SR)}$		Slave receiver	4	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	64	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	22	-	
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	12	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	8	-	

1. The maximum for 256xFs is 8 MHz

Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the

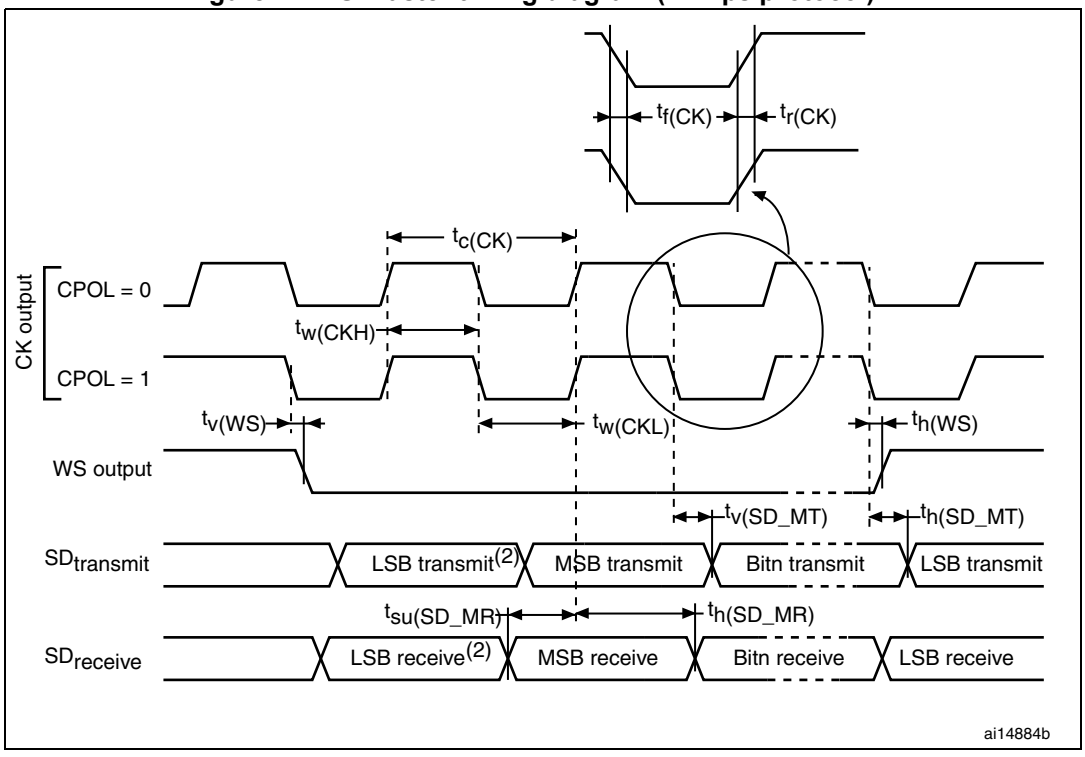
*ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Figure 21. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 22. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are guaranteed by design.

Table 53. ADC clock frequency

Symbol	Parameter	Conditions			Min	Max	Unit
f_{ADC}	ADC clock frequency	Voltage range 1 & 2	2.4 V ≤V_{DDA} ≤3.6 V	V_{REF+} = V_{DDA}	0.480	16	MHz
				V_{REF+} < V_{DDA} V_{REF+} > 2.4 V		8	
				V_{REF+} < V_{DDA} V_{REF+} ≤2.4 V		4	
			1.8 V ≤V_{DDA} ≤2.4 V	V_{REF+} = V_{DDA}		8	
				V_{REF+} < V_{DDA}		4	
		Voltage range 3				4	

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	V_{SSA}	-	
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF}(2)	Current on the V_{REF} input pin	Peak	-	400	700	
		Average			450	
V_{AIN}	Conversion voltage range(3)	-	0(4)	-	V_{REF+}	V
f_S	12-bit sampling rate	Direct channels	-	-	1	Msps
		Multiplexed channels	-	-	0.76	
	10-bit sampling rate	Direct channels	-	-	1.07	Msps
		Multiplexed channels	-	-	0.8	
	8-bit sampling rate	Direct channels	-	-	1.23	Msps
		Multiplexed channels	-	-	0.89	
	6-bit sampling rate	Direct channels	-	-	1.45	Msps
		Multiplexed channels	-	-	1	

Table 54. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S (5)	Sampling time	Direct channels 2.4 V ≤V_{DDA} ≤3.6 V	0.25	-	-	µs
		Multiplexed channels 2.4 V ≤V_{DDA} ≤3.6 V	0.56	-	-	
		Direct channels 1.8 V ≤V_{DDA} ≤2.4 V	0.56	-	-	
		Multiplexed channels 1.8 V ≤V_{DDA} ≤2.4 V	1	-	-	
		-	4	-	384	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	1	-	24.75	µs
		-	4 to 384 (sampling phase) +12 (successive approximation)			$1/f_{ADC}$
C_{ADC}	Internal sample and hold capacitor	Direct channels	-	16	-	pF
		Multiplexed channels	-		-	
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN} (6)	Signal source impedance		-	-	50	kΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

1. The Vref+ input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through VREF is composed of two parameters:

   - one constant (max 300 µA)

   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses

   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. V_{SSA} or V_{REF-} must be tied to ground.
5. Minimum sampling time is reached for an external input impedance limited to a value as defined in *Table 56: Maximum source impedance RAIN max*
6. External impedance has another high value limitation when using short sampling time as defined in *Table 56: Maximum source impedance RAIN max*

Table 58. Operational amplifier characteristics (continued)

Symbol	Parameter		Condition[1]	Min[2]	Typ	Max[2]	Unit
PSRR	Power supply rejection ratio	Normal mode	DC	-	-85	-	dB
		Low-power mode		-	-90	-	
GBW	Bandwidth	Normal mode	V_{DD}>2.4 V	400	1000	3000	kHZ
		Low-power mode		150	300	800	
		Normal mode	V_{DD}<2.4 V	200	500	2200	
		Low-power mode		70	150	800	
SR	Slew rate	Normal mode	V_{DD}>2.4 V (between 0.1 V and V_{DD}-0.1 V)	-	700	-	V/ms
		Low-power mode	V_{DD}>2.4 V	-	100	-	
		Normal mode	V_{DD}<2.4 V	-	300	-	
		Low-power mode		-	50	-	
AO	Open loop gain	Normal mode		55	100	-	dB
		Low-power mode		65	110	-	
R_L	Resistive load	Normal mode	V_{DD}<2.4 V	4	-	-	kΩ
		Low-power mode		20	-	-	
C_L	Capacitive load		-	-	-	50	pF
VOH_{SAT}	High saturation voltage	Normal mode	I_{LOAD} = max or R_L = min	V_{DD}-100	-	-	mV
		Low-power mode		V_{DD}-50	-	-	
VOL_{SAT}	Low saturation voltage	Normal mode		-	-	100	
		Low-power mode		-	-	50	
φm	Phase margin		-	-	60	-	°
GM	Gain margin		-	-	-12	-	dB
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		-	-	1	-	ms
t_{WAKEUP}	Wakeup time	Normal mode	C_L ≤50 pf, R_L ≥ 4 kΩ	-	10	-	µs
		Low-power mode	C_L ≤50 pf, R_L ≥ 20 kΩ	-	30	-	

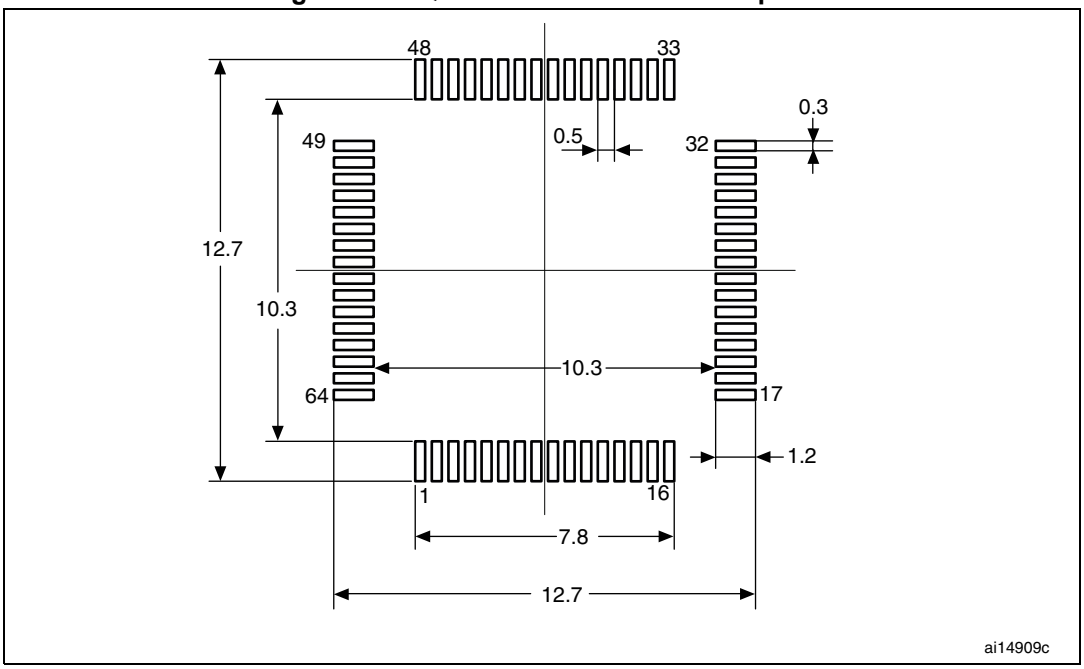
1. Operating conditions are limited to junction temperature (0 °C to 105 °C) when V_{DD} is below 2 V. Otherwise to the full ambient temperature range (-40 °C to 85 °C, -40 °C to 105 °C).
2. Guaranteed by characterization results, not tested in production.

Table 62. LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D3	-	7.500	-	-	0.2953	-
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031
K	0.0	3.5	7.0	0.0	3.5	7.0

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 28. LQFP64 Recommended footprint



1. Dimensions are in millimeters.