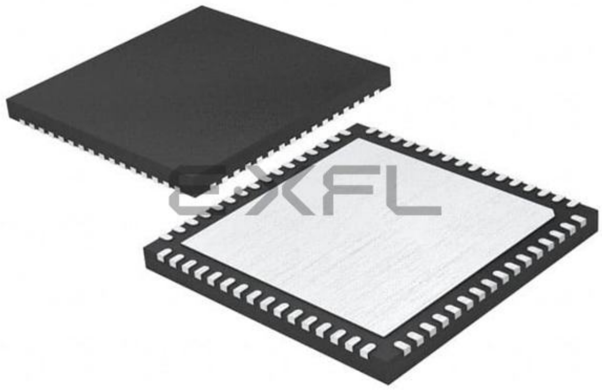


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ecg064-i-mr

TABLE 1-22: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
JTAG							
TCK	27	38	B21	56	I	ST	JTAG Test Clock Input Pin
TDI	28	39	A26	57	I	ST	JTAG Test Data Input Pin
TDO	24	40	B22	58	O	—	JTAG Test Data Output Pin
TMS	23	17	A11	22	I	ST	JTAG Test Mode Select Pin
Trace							
TRCLK	57	89	A61	129	O	—	Trace Clock
TRD0	58	97	B55	141	O	—	Trace Data bits 0-3
TRD1	61	96	A65	140	O	—	
TRD2	62	95	B54	139	O	—	
TRD3	63	90	B51	130	O	—	
Programming/Debugging							
PGED1	16	25	A18	36	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	15	24	A17	35	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	18	27	A19	38	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	17	26	B14	37	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
$\overline{MCLR}$	9	15	A10	20	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

The MIPS architecture defines that the result of a multiply or divide operation be placed in one of four pairs of HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

The MDU also implements various shift instructions operating on the HI/LO register and multiply instructions as defined in the DSP ASE. The MDU supports all of the data types required for this purpose and includes three extra HI/LO registers as defined by the ASE.

Table 3-2 lists the latencies and repeat rates for the DSP multiply and dot-product operations. The approximate latencies and repeat rates are listed in terms of pipeline clocks.

TABLE 3-2: DSP-RELATED LATENCIES AND REPEAT RATES

Op code	Latency	Repeat Rate
Multiply and dot-product without saturation after accumulation	5	1
Multiply and dot-product with saturation after accumulation	5	1
Multiply without accumulation	5	1

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation and cache protocols, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as cache size and set associativity, and the presence of options like microMIPS, is also available by accessing the CP0 registers, listed in Table 3-3.

NOTES:

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
12A0	DCH3CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
12B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
12C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
12D0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
12E0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
12F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1360	DCH4CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1370	DCH4ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1380	DCH4INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000

Legend: x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

11.0 HI-SPEED USB WITH ON-THE-GO (OTG)

Note:	This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 51. "Hi-Speed USB with On-The-Go (OTG)"** (DS60001232), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 embedded host, device, or OTG implementation with a minimum of external components.

The module supports Hi-Speed, Full-Speed, or Low-Speed in any of the operating modes. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the RAM controller, packet encode/decode, UTM synchronization, end-point control, a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

Note:	To avoid cache coherency problems on devices with L1 cache, USB buffers must only be allocated or accessed from the KSEG1 segment.

The USB module includes the following features:

- USB Hi-Speed, Full-Speed, and Low-Speed support for host and device
- USB OTG support with one or more Hi-Speed, Full-Speed, or Low-Speed device
- Integrated signaling resistors
- Integrated analog comparators for V_{BUS} monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Integrated 8-channel DMA to access system RAM and Flash
- Seven transmit endpoints and seven receive endpoints, in addition to Endpoint 0
- Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) support
- Suspend and resume signaling support
- Dynamic FIFO sizing
- Integrated RAM for the FIFOs, eliminating the need for system RAM for the FIFOs
- Link power management support

Note 1:	The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.
2:	If the USB module is used, the Primary Oscillator (POSC) is limited to either 12 MHz or 24 MHz.

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 19-16 **TXFIFOSZ<3:0>:** TX Endpoint FIFO packet size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = 4096 bytes
1000 = 2048 bytes
0111 = 1024 bytes
0110 = 512 bytes
0101 = 256 bytes
0100 = 128 bytes
0011 = 64 bytes
0010 = 32 bytes
0001 = 16 bytes
0000 = 8 bytes

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **TXEDMA:** TX Endpoint DMA Assertion Control bit
1 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.
0 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 8 **RXEDMA:** RX Endpoint DMA Assertion Control bit
1 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.
0 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 7 **BDEV:** USB Device Type bit
1 = USB is operating as a 'B' device
0 = USB is operating as an 'A' device

bit 6 **FSDEV:** Full-Speed/Hi-Speed device detection bit (*Host mode*)
1 = A Full-Speed or Hi-Speed device has been detected being connected to the port
0 = No Full-Speed or Hi-Speed device detected

bit 5 **LSDEV:** Low-Speed Device Detection bit (*Host mode*)
1 = A Low-Speed device has been detected being connected to the port
0 = No Low-Speed device detected

bit 4-3 **VBUS<1:0>:** VBUS Level Detection bits
11 = Above VBUS Valid
10 = Above AValid, below VBUS Valid
01 = Above Session End, below AValid
00 = Below Session End

bit 2 **HOSTMODE:** Host Mode bit
1 = USB module is acting as a Host
0 = USB module is not acting as a Host

bit 1 **HOSTREQ:** Host Request Control bit
'B' device only:
1 = USB module initiates the Host Negotiation when Suspend mode is entered. This bit is cleared when Host Negotiation is completed.
0 = Host Negotiation is not taking place

18.1 Output Compare Control Registers

TABLE 18-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
4000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
4020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
4200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
4220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
4400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
4420	OC3RS	31:16	OC3RS<31:0>																xxxx
		15:0																	xxxx
4600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
4620	OC4RS	31:16	OC4RS<31:0>																xxxx
		15:0																	xxxx
4800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
4820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 19-3: SPIxSTAT: SPI STATUS REGISTER

bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit

1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty

Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.

Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit

1 = Transmit not yet started, SPITXB is full
0 = Transmit buffer is not full

Standard Buffer Mode:

Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.

Enhanced Buffer Mode:

Set when CWPTR + 1 = SRPTR; cleared otherwise

bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit

1 = Receive buffer, SPIxRXB is full
0 = Receive buffer, SPIxRXB is not full

Standard Buffer Mode:

Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer Mode:

Set when SWPTR + 1 = CRPTR; cleared otherwise

REGISTER 20-5: SQI1CLKCON: SQI CLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CLKDIV<7:0>(1)							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R/W-0
	—	—	—	—	—	—	STABLE	EN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-8 **CLKDIV<7:0>:** SQI Clock TSQI Frequency Select bit(1)
10000000 = Base clock TBC is divided by 512
01000000 = Base clock TBC is divided by 256
00100000 = Base clock TBC is divided by 128
00010000 = Base clock TBC is divided by 64
00001000 = Base clock TBC is divided by 32
00000100 = Base clock TBC is divided by 16
00000010 = Base clock TBC is divided by 8
00000001 = Base clock TBC is divided by 4
00000000 = Base clock TBC is divided by 2

Setting these bits to ‘00000000’ specifies the highest frequency of the SQI clock.

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **STABLE:** TSQI Clock Stable Select bit
This bit is set to ‘1’ when the SQI clock, TSQI, is stable after writing a ‘1’ to the EN bit.
1 = TSQI clock is stable
0 = TSQI clock is not stable

bit 0 **EN:** TSQI Clock Enable Select bit
When clock oscillation is stable, the SQI module will set the STABLE bit to ‘1’.
1 = Enable the SQI clock (TSQI) (when clock oscillation is stable, the SQI module sets the STABLE bit to ‘1’)
0 = Disable the SQI clock (TSQI) (the SQI module should stop its clock to enter a low power state); SFRs can still be accessed, as they use PBCLK5

Note 1: Refer to Table in **Section 37.0 “Electrical Characteristics”** for the maximum clock frequency specifications.

REGISTER 22-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>(1)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** UARTx Enable bit
- 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
- 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation in Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **UEN<1:0>:** UARTx Enable bits(1)
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
- 1 = Wake-up enabled
- 0 = Wake-up disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **Section 12.3 “Peripheral Pin Select (PPS)”** for more information).

Figure 22-2 and Figure 22-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 22-2: UART RECEPTION

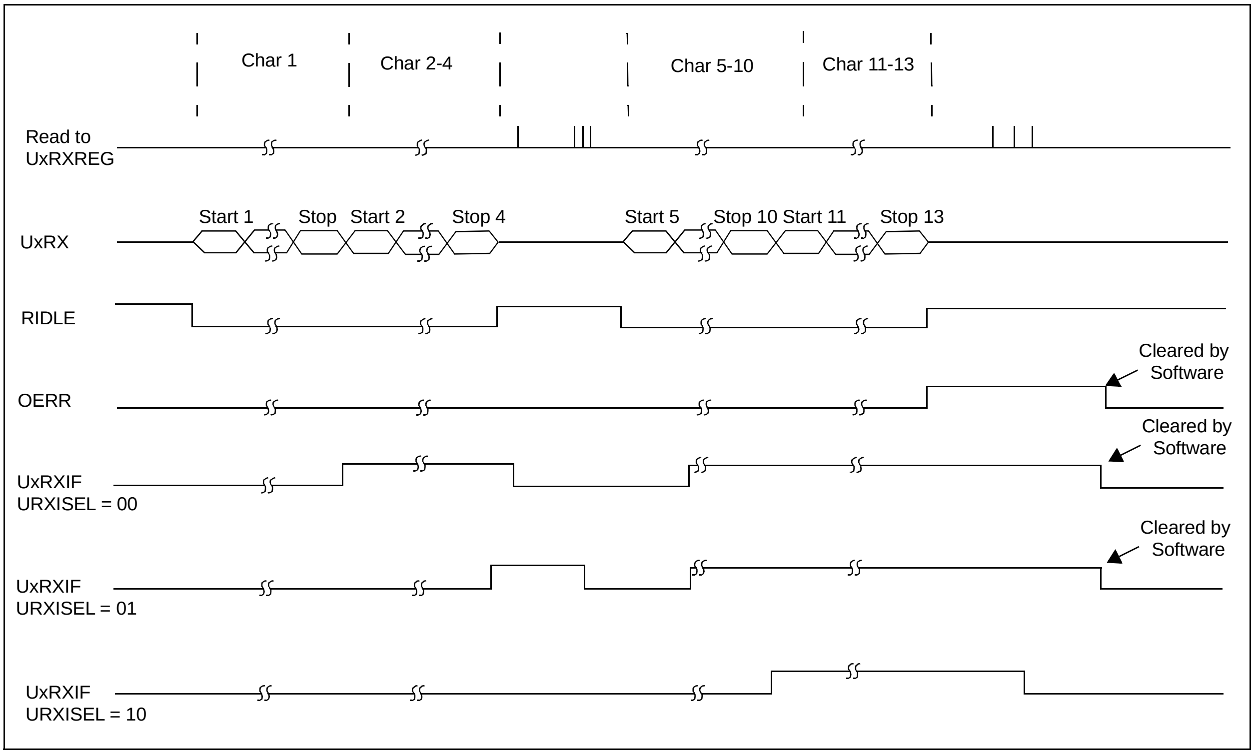
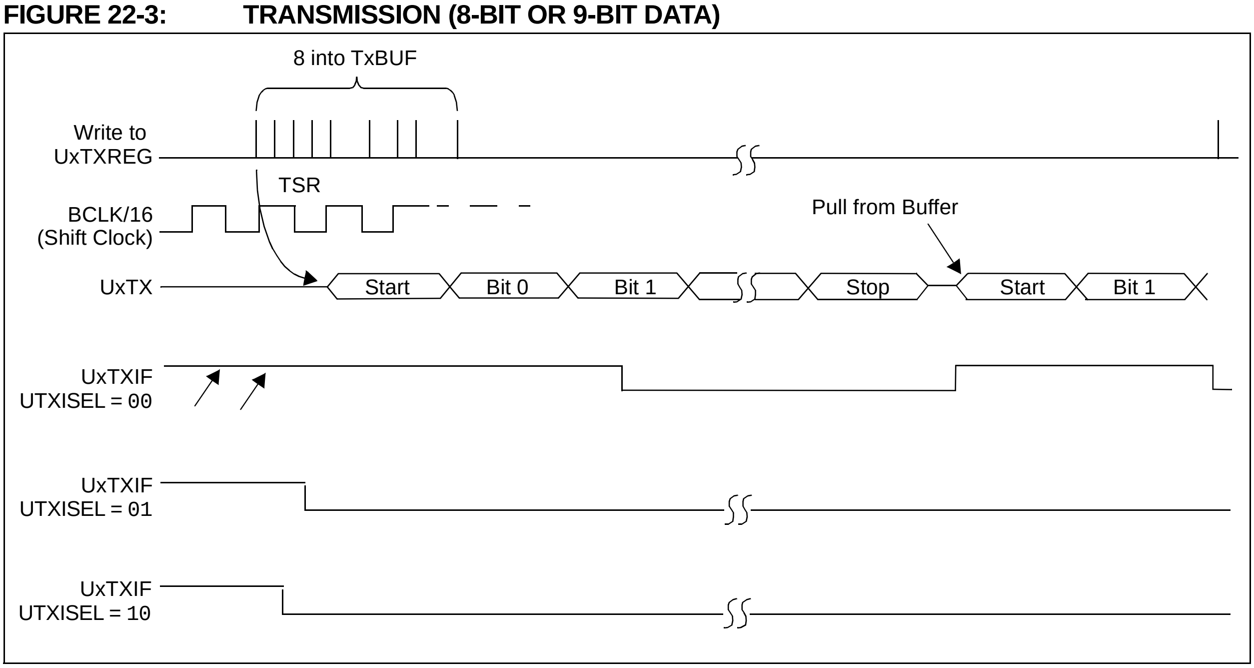


FIGURE 22-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



REGISTER 27-1: RNGVER: RANDOM NUMBER GENERATOR VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **ID<15:0>:** Block Identification bits

bit 15-8 **VERSION<7:0>:** Block Version bits

bit 7-0 **REVISION<7:0>:** Block Revision bits

REGISTER 28-3: AD1CON3: ADC1 CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0, HC	R/W-0, HC	R/W-0, HC	U-0	U-0	U-0	U-0	U-0
	CAL(2)	GSWTRG	RQCNVRT	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	—	—	—	VREFSEL<2:0>(1)			—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	ADINSEL<5:0>					

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **CAL:** Calibration bit(2)
1 = Initiate an ADC calibration cycle
0 = Calibration cycle is not in progress

bit 30 **GSWTRG:** Global Software Trigger bit
1 = Trigger analog-to-digital conversion for ADC inputs that have selected the GSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the AD1TRGn registers or through the STRGSRC<4:0> bits in the AD1CON1 register
0 = This bit is automatically cleared

bit 29 **RQCNVRT:** Individual ADC Input Conversion Request bit
This bit and its associated ADINSEL<5:0> bits enable the user to individually request an analog-to-digital conversion of an analog input without having to reprogram the TRGSRC<4:0> bits or the STRGSRC<4:0> bits. This is very useful during debugging or error handling situations where the user software needs to obtain an immediate ADC result of a specific input.
1 = Trigger the conversion of the selected ADC input as specified by the ADINSEL<5:0> bits
0 = This bit is automatically cleared

bit 28-13 **Unimplemented:** Read as '0'

bit 12-10 **VREFSEL<2:0>:** VREF Input Selection bits(1)

VREFSEL<2:0>	VREFH	VREFL
111	Reserved	Reserved
110	Reserved	Reserved
101	Reserved	Reserved
100	Reserved	Reserved
011	VREF+	VREF-
010	AVDD	VREF-
001	VREF+	AVSS
000	AVDD	AVSS

bit 9-6 **Unimplemented:** Read as '0'

Note 1: These bits should be configured prior to enabling the ADC module by setting the ADCEN bit (AD1CON1<15> = 1).

2: See **28.1 "ADC Configuration Requirements"** for detailed ADC calibration information.

REGISTER 29-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN19	MSEL19<1:0>		FSEL19<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN18	MSEL18<1:0>		FSEL18<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN17	MSEL17<1:0>		FSEL17<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN16	MSEL16<1:0>		FSEL16<4:0>				

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN19:** Filter 19 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL19<1:0>:** Filter 19 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL19<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN18:** Filter 18 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL18<1:0>:** Filter 18 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL18<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘0’.

REGISTER 29-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN23:** Filter 23 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN22:** Filter 22 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘0’.

34.3 On-Chip Voltage Regulator

The core and digital logic for all PIC32MZ EC devices is designed to operate at a nominal 1.8V. To simplify system designs, devices in the PIC32MZ EC family incorporate an on-chip regulator providing the required core logic voltage from VDD.

34.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

34.3.2 ON-CHIP REGULATOR AND BOR

PIC32MZ EC devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 37.1 "DC Characteristics"**.

34.4 On-chip Temperature Sensor

PIC32MZ EC devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **Section 37.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **Section 28.0 "Pipelined Analog-to-Digital Converter (ADC)"** for more information).

34.5 Programming and Diagnostics

PIC32MZ EC devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 34-1: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS

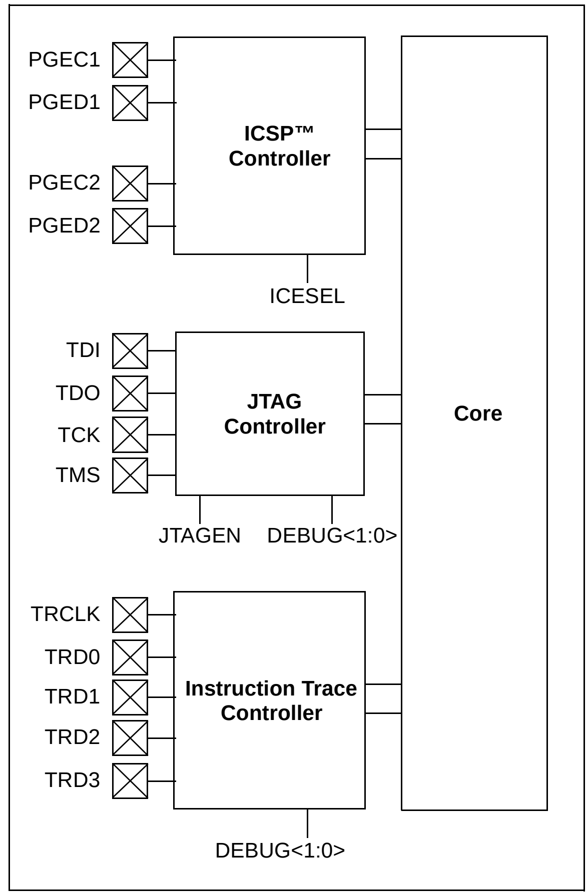


TABLE 37-40: TEMPERATURE SENSOR SPECIFICATIONS

AC CHARACTERISTICS			**Standard Operating Conditions (see Note 1): 2.3V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TS10	V_{TS}	Rate of Change	—	-5	—	mV/ºC	—
TS11	T_R	Resolution	—	±2	—	ºC	—
TS12	IV_{TEMP}	Voltage Range	0.2	—	1.2	V	—
TS13	T_{MIN}	Minimum Temperature	—	-40	—	ºC	IV_{TEMP} = 1.2V
TS14	T_{MAX}	Maximum Temperature	—	125	—	ºC	IV_{TEMP} = 0.38V

Note 1: The temperature sensor is functional at V_{BORMIN} < V_{DD} < V_{DDMIN}, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 37-23: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

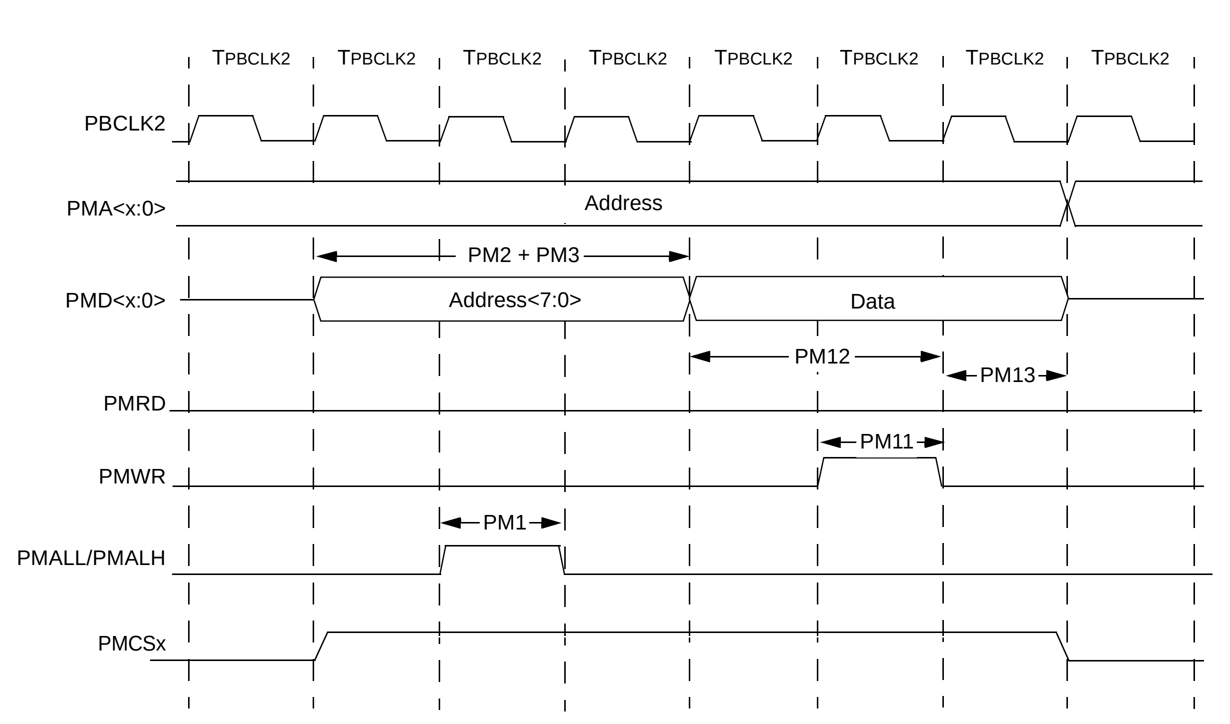


TABLE 37-43: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics(1)	Min.	Typ.	Max.	Units	Conditions
PM11	TWR	PMWR Pulse Width	—	1 TPBCLK2	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPBCLK2	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPBCLK2	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.

A.3 CPU

The CPU in the PIC32MZ family of devices has been changed to the MIPS microAptiv™ MPU architecture. This CPU includes DSP ASE, internal data and instruction L1 caches, and a TLB-based MMU.

Table A-4 summarizes some of the key differences (indicated by **Bold** type) in the internal CPU registers.

TABLE A-4: CPU DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
L1 Data and Instruction Cache and Prefetch Wait States	
On PIC32MX devices, the cache was included in the prefetch module outside the CPU.	On PIC32MZ devices, the CPU has a separate L1 instruction and data cache in the core. The PREFEN<1:0> bits still enable the prefetch module; however, the K0<2:0> bits in the CP0 registers controls the internal L1 cache for the designated regions.
PREFEN<1:0> (**CHECON**<5:4>) **11 = Enable predictive prefetch for both cacheable and non-cacheable regions** **10 = Enable predictive prefetch for non-cacheable regions only** **01 = Enable predictive prefetch for cacheable regions only** 00 = Disable predictive prefetch	PREFEN<1:0> (**PRECON**<5:4>) **11 = Enable predictive prefetch for any address** **10 = Enable predictive prefetch for CPU instructions and CPU data** **01 = Enable predictive prefetch for CPU instructions only** 00 = Disable predictive prefetch
DCSZ<1:0> (CHECON<9:8>) Changing these bits causes all lines to be reinitialized to the "invalid" state. 11 = Enable data caching with a size of 4 lines 10 = Enable data caching with a size of 2 lines 01 = Enable data caching with a size of 1 line 00 = Disable data caching CHECOH (CHECON<16>) 1 = Invalidate all data and instruction lines 0 = Invalidate all data and instruction lines that are not locked	**K0<2:0> (CP0 Reg 16, Select 0)** **011 = Cacheable, non-coherent, write-back, write allocate** **010 = Uncached** **001 = Cacheable, non-coherent, write-through, write allocate** **000 = Cacheable, non-coherent, write-through, no write allocate**
	The Program Flash Memory read wait state frequency points have changed in PIC32MZ devices. The register for accessing the PFMWS field has changed from CHECON to PRECON.
PFMWS<2:0> (**CHECON**<2:0>) 111 = Seven Wait states 110 = Six Wait states 101 = Five Wait states 100 = Four Wait states 011 = Three Wait states 010 = Two Wait states **(61-80 MHz)** 001 = One Wait state **(31-60 MHz)** 000 = Zero Wait state **(0-30 MHz)**	PFMWS<2:0> (**PRECON**<2:0>) 111 = Seven Wait states • • • 011 = Three Wait states 010 = Two Wait states **(133-200 MHz)** 001 = One Wait state **(66-133 MHz)** 000 = Zero Wait states **(0-66 MHz)** **Note:** Wait states listed are for ECC enabled.

TABLE A-4: CPU DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
Core Instruction Execution	
On PIC32MX devices, the CPU can execute MIPS16e instructions and uses a 16-bit instruction set, which reduces memory size. **MIPS16e®**	On PIC32MZ devices, the CPU can operate a mode called microMIPS. microMIPS mode is an enhanced MIPS32® instruction set that uses both 16-bit and 32-bit opcodes. This mode of operation reduces memory size with minimum performance impact. **microMIPS™** The BOOTISA (DEVCFG0<6>) Configuration bit controls the MIPS32 and microMIPS modes for boot and exception code. 1 = Boot code and Exception code is MIPS32® (ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register) 0 = Boot code and Exception code is microMIPS™ (ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

A.4 Resets

The PIC32MZ family of devices has updated the resets modules to incorporate the new handling of NMI resets from the WDT, DMT, and the FSCM. In addition, some bits have been moved, as summarized in Table A-5.

TABLE A-5: RESET DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
Power Reset	
VREGS (**RCON<8>**) 1 = Regulator is enabled and is on during Sleep mode 0 = Regulator is disabled and is off during Sleep mode	The VREGS bit, which controls whether the internal regulator is enabled in Sleep mode, has been moved from RCON in PIC32MX5XX/6XX/7XX devices to a new PWRCON register in PIC32MZ devices. VREGS (**PWRCON<0>**) 1 = Voltage regulator will remain active during Sleep 0 = Voltage regulator will go to Stand-by mode during Sleep
Watchdog Timer Reset	
On PIC32MX devices, a WDT expiration immediately triggers a device reset. **WDT expiration immediately causes a device reset.**	On PIC32MZ devices, the WDT expiration now causes a NMI. The WDTO bit in RNMICON indicates that the WDT caused the NMI. A new timer, NMICNT, runs when the WDT NMI is triggered, and if it expires, the device is reset. **WDT expiration causes a NMI, which can then trigger the device reset.** **WDTO (RNMICON<24>)** **1 = WDT time-out has occurred and caused a NMI** **0 = WDT time-out has not occurred** **NMICNT<7:0> (RNMICON<7:0>)**

