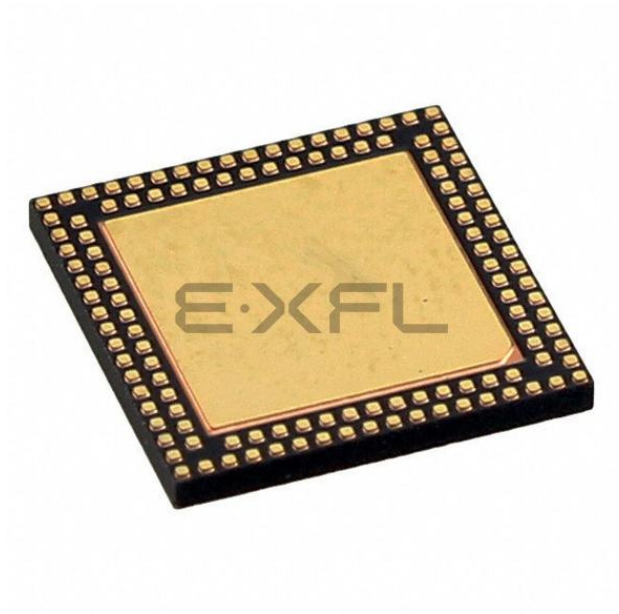

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	98
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ecg124-i-tl

NOTES:

TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 4-18: SYSTEM BUS TARGET 10 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A820	SBT10ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
A824	SBT10ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
A828	SBT10ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
A830	SBT10ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A838	SBT10ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A840	SBT10REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A850	SBT10RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A858	SBT10WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 5-7: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

bit 4 **UBWP4:** Upper Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF enabled
0 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF disabled

bit 3 **UBWP3:** Upper Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF enabled
0 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF disabled

bit 2 **UBWP2:** Upper Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF enabled
0 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF disabled

bit 1 **UBWP1:** Upper Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF enabled
0 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF disabled

bit 0 **UBWP0:** Upper Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF enabled
0 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF disabled

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0790	OFF148(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0794	OFF149(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0798	OFF150(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
079C	OFF151(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A0	OFF152(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A4	OFF153	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A8	OFF154	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07AC	OFF155	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B0	OFF156	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B4	OFF157	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B8	OFF158	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07BC	OFF159	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C0	OFF160	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C4	OFF161	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C8	OFF162	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXINTERV<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **RXFIFOSZ<3:0>:** Receive FIFO Size bits
1111 = Reserved
1110 = Reserved
1101 = 8192 bytes
1100 = 4096 bytes
•
•
•
0011 = 8 bytes
0010 = Reserved
0001 = Reserved
0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 27-24 **TXFIFOSZ<3:0>:** Transmit FIFO Size bits
1111 = Reserved
1110 = Reserved
1101 = 8192 bytes
1100 = 4096 bytes
•
•
•
0011 = 8 bytes
0010 = Reserved
0001 = Reserved
0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 23-16 **Unimplemented:** Read as '0'

REGISTER 11-18: USBExTXA: USB ENDPOINT 'x' TRANSMIT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	TXHUBPRT<6:0>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULTTRAN	TXHUBADD<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	TXFADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-24 **TXHUBPRT<6:0>:** TX Hub Port bits (*Host mode*)

When a low- or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, this field records the port number of that USB 2.0 hub.

bit 23 **MULTTRAN:** TX Hub Multiple Translators bit (*Host mode*)
1 = The USB 2.0 hub has multiple transaction translators
0 = The USB 2.0 hub has a single transaction translator

bit 22-16 **TXHUBADD<6:0>:** TX Hub Address bits (*Host mode*)

When a Low-Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, these bits record the address of the USB 2.0 hub.

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **TXFADDR<6:0>:** TX Functional Address bits (*Host mode*)

Specifies the address for the target function that is be accessed through the associated endpoint. It needs to be defined for each TX endpoint that is used.

TABLE 12-1: INPUT PIN SELECTION

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT3	INT3R	INT3R<3:0>	0000 = RPD2 0001 = RPG8 0010 = RPF4 0011 = RPD10 0100 = RPF1 0101 = RPB9 0110 = RPB10 0111 = RPC14 1000 = RPB5 1001 = Reserved 1010 = RPC1(1) 1011 = RPD14(1) 1100 = RPG1(1) 1101 = RPA14(1) 1110 = RPD6(2) 1111 = Reserved
T2CK	T2CKR	T2CKR<3:0>	
T6CK	T6CKR	T6CKR<3:0>	
IC3	IC3R	IC3R<3:0>	
IC7	IC7R	IC7R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	
$\overline{\text{U2CTS}}$	U2CTSR	U2CTSR<3:0>	
U5RX	U5RXR	U5RXR<3:0>	
$\overline{\text{U6CTS}}$	U6CTSR	U6CTSR<3:0>	
SDI1	SDI1R	SDI1R<3:0>	
SDI3	SDI3R	SDI3R<3:0>	
SDI5(1)	SDI5R(1)	SDI5R<3:0>(1)	
$\overline{\text{SS6}}$(1)	SS6R(1)	SS6R<3:0>(1)	
REFCLKI1	REFCLKI1R	REFCLKI1R<3:0>	
INT4	INT4R	INT4R<3:0>	0000 = RPD3 0001 = RPG7 0010 = RPF5 0011 = RPD11 0100 = RPF0 0101 = RPB1 0110 = RPE5 0111 = RPC13 1000 = RPB3 1001 = Reserved 1010 = RPC4(1) 1011 = RPD15(1) 1100 = RPG0(1) 1101 = RPA15(1) 1110 = RPD7(2) 1111 = Reserved
T5CK	T5CKR	T5CKR<3:0>	
T7CK	T7CKR	T7CKR<3:0>	
IC4	IC4R	IC4R<3:0>	
IC8	IC8R	IC8R<3:0>	
U3RX	U3RXR	U3RXR<3:0>	
$\overline{\text{U4CTS}}$	U4CTSR	U4CTSR<3:0>	
SDI2	SDI2R	SDI2R<3:0>	
SDI4	SDI4R	SDI4R<3:0>	
C1RX(3)	C1RXR(3)	C1RXR<3:0>(3)	
REFCLKI4	REFCLKI4R	REFCLKI4R<3:0>	
INT2	INT2R	INT2R<3:0>	0000 = RPD9 0001 = RPG6 0010 = RPB8 0011 = RPB15 0100 = RPD4 0101 = RPB0 0110 = RPE3 0111 = RPB7 1000 = Reserved 1001 = RPF12(1) 1010 = RPD12(1) 1011 = RPF8(1) 1100 = RPC3(1) 1101 = RPE9(1) 1110 = Reserved 1111 = Reserved
T3CK	T3CKR	T3CKR<3:0>	
T8CK	T8CKR	T8CKR<3:0>	
IC2	IC2R	IC2R<3:0>	
IC5	IC5R	IC5R<3:0>	
IC9	IC9R	IC9R<3:0>	
$\overline{\text{U1CTS}}$	U1CTSR	U1CTSR<3:0>	
U2RX	U2RXR	U2RXR<3:0>	
$\overline{\text{U5CTS}}$	U5CTSR	U5CTSR<3:0>	
$\overline{\text{SS1}}$	SS1R	SS1R<3:0>	
$\overline{\text{SS3}}$	SS3R	SS3R<3:0>	
$\overline{\text{SS4}}$	SS4R	SS4R<3:0>	
$\overline{\text{SS5}}$(1)	SS5R(1)	SS5R<3:0>(1)	
C2RX(3)	C2RXR(3)	C2RXR<3:0>(3)	

Note 1: This selection is not available on 64-pin devices.

2: This selection is not available on 64-pin or 100-pin devices.

3: This selection is not available on devices without a CAN module.

REGISTER 24-1: EBICSx: EXTERNAL BUS INTERFACE CHIP SELECT REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CSADDR<15:0>:** Base Address for Device bits
Address in physical memory, which will select the external device.

bit 15-0 **Unimplemented:** Read as '0'

REGISTER 28-1: AD1CON1: ADC1 CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FILTRDLY<4:0>					STRGSRC<4:2>		
23:16	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	STRGSRC<1:0>		—	—	—	EIE<2:0>(1)		
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0
	ADCEN(2,4)	—	ADSIDL	—	FRACT	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **FILTRDLY<4:0>:** Oversampling Digital Filter Delay bits
Specifies the sampling time for subsequent automatic triggers when using the Oversampling Digital Filter. Sample time is 1.5 + FILTRDLY<4:0> TAD.
11111 = Sample time is 32.5 TAD
11110 = Sample time is 31.5 TAD
•
•
•
00001 = Sample time is 2.5 TAD
00000 = Sample time is 1.5 TAD

bit 26-22 **STRGSRC<4:0>:** Scan Trigger Source Select bits
11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 COUT(3)
01011 = Comparator 1 COUT(3)
01010 = OCMP5(3)
01001 = OCMP3(3)
01000 = OCMP1(3)
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0
00011 = Reserved
00010 = Reserved
00001 = Global software trigger (GSWTRG)
00000 = No trigger

Note 1: The early interrupt feature should not be used if polling any of the ARDY bits to determine if the conversion is complete. Early interrupts should be used only when all results from the ADC module are retrieved using an individual interrupt routine to fetch ADC results.

2: The ADCEN bit should be set only after the ADC module has been configured. Changing ADC Configuration bits when ADCEN = 1, will result in unpredictable behavior. When ADCEN = 0, the ADC clocks are disabled, the internal control logic is reset, and all status flags used by the module are cleared. However, the SFRs are available for reading and writing.

3: The rising edge of the module output signal triggers an ADC conversion. See Figure 18-1 in **Section 18.0 "Output Compare"** and Figure 31-1 in **Section 31.0 "Comparator"** for more information.

4: See **28.1 "ADC Configuration Requirements"** for detailed ADC calibration information.

Note: The ADC module is not available for normal operations until the ADCRDY bit (AD1CON2<31>) is set.

REGISTER 28-9: AD1DSTAT1: ADC1 DATA READY STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY31	ARDY30	ARDY29	ARDY28	ARDY27	ARDY26	ARDY25	ARDY24
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY23	ARDY22	ARDY21	ARDY20	ARDY19	ARDY18	ARDY17	ARDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ARDYx:** Conversion Data Ready for Corresponding Analog Input Ready bits ('x' = 31-0)

1 = This bit is set when data is ready in the buffer. An interrupt will be generated if the appropriate bit in the IECx register is set or if enabled for the ADC Global interrupt in the AD1GIRQEN register.

0 = This bit is cleared when the associated data register is read

Note: ARDYx = ANx, where 'x' = 0-31.

REGISTER 28-10: AD1DSTAT2: ADC1 DATA READY STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	ARDY44	ARDY43	ARDY42	ARDY41	ARDY40
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY39	ARDY38	ARDY37	ARDY36	ARDY35	ARDY34	ARDY33	ARDY32

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **ARDYx:** Conversion Data Ready for Corresponding Analog Input Ready bits ('x' = 32-44)

1 = This bit is set when data is ready in the buffer. An interrupt will be generated if the appropriate bit in the IECx register is set or if enabled for the ADC Global interrupt in the AD1GIRQEN register.

0 = This bit is cleared when the associated data register is read

Note: ARDYx = ANx, where 'x' =32-42, ARDY43 = IV_{REF}, and ARDY44 = IV_{TEMP}.

REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER (CONTINUED)

bit 6 **TXBUSY:** Transmit Busy bit(2,6)

1 = TX logic is receiving data
0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

bit 5 **RXBUSY:** Receive Busy bit(3,6)

1 = RX logic is receiving data
0 = RX logic is idle

This bit indicates that a packet is currently being received. A change in this status bit is not necessarily reflected by the RXDONE interrupt, as RX packets may be aborted or rejected by the RX filter.

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is only used for RX operations.
2: This bit is only affected by TX operations.
3: This bit is only affected by RX operations.
4: This bit is affected by TX and RX operations.
5: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
6: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

32.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

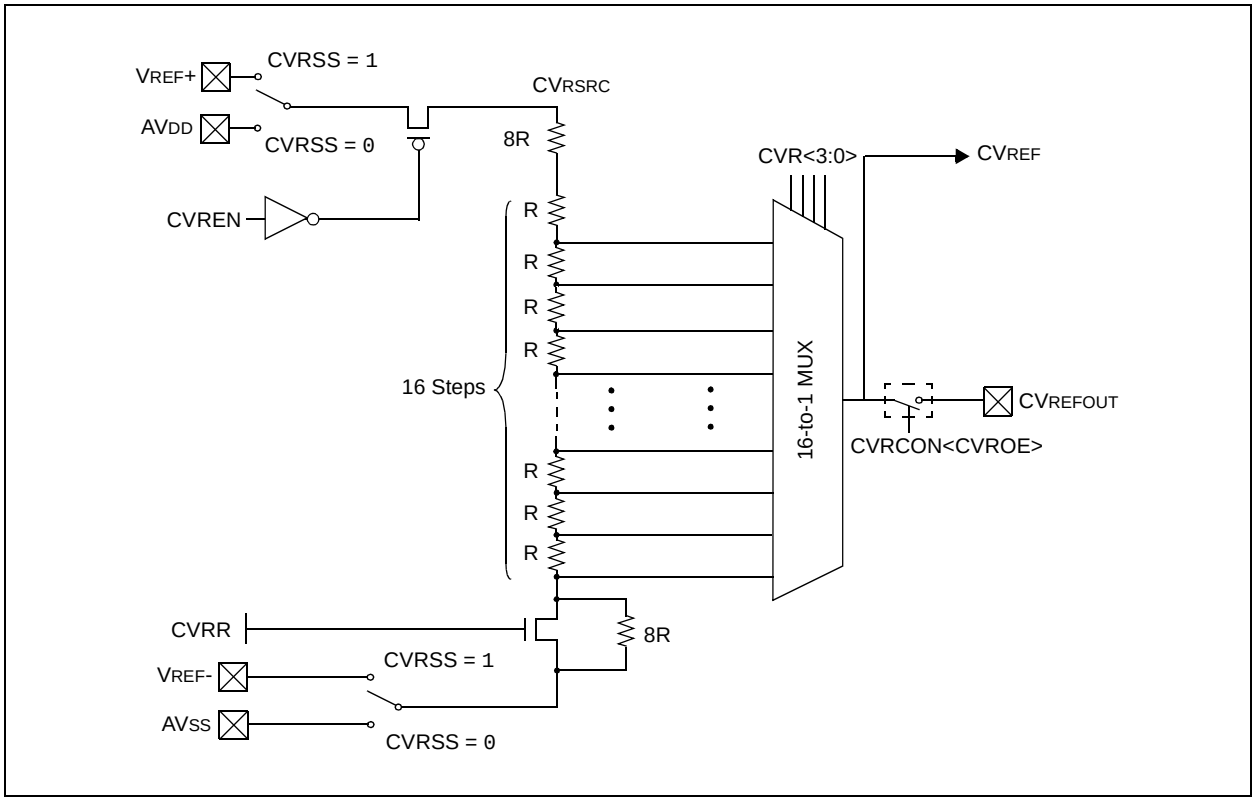
The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

A block diagram of the CVREF module is illustrated in Figure 32-1.

FIGURE 32-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



NOTES:

33.3 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 33-1 for more information.

Note:	Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TABLE 33-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS(1)

Peripheral	PMDx bit Name	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Input Capture 6	IC6MD	PMD3<5>
Input Capture 7	IC7MD	PMD3<6>
Input Capture 8	IC8MD	PMD3<7>
Input Capture 9	IC9MD	PMD3<8>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Output Compare 6	OC6MD	PMD3<21>
Output Compare 7	OC7MD	PMD3<22>
Output Compare 8	OC8MD	PMD3<23>
Output Compare 9	OC9MD	PMD3<24>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
Timer6	T6MD	PMD4<5>
Timer7	T7MD	PMD4<6>
Timer8	T8MD	PMD4<7>
Timer9	T9MD	PMD4<8>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MZ EC Family Features"** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

REGISTER 34-7: CFGCON: CONFIGURATION CONTROL REGISTER (CONTINUED)

bit 5-4 **ECCCON<1:0>:** Flash ECC Configuration bits
11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

bit 3 **JTAGEN:** JTAG Port Enable bit
1 = Enable the JTAG port
0 = Disable the JTAG port

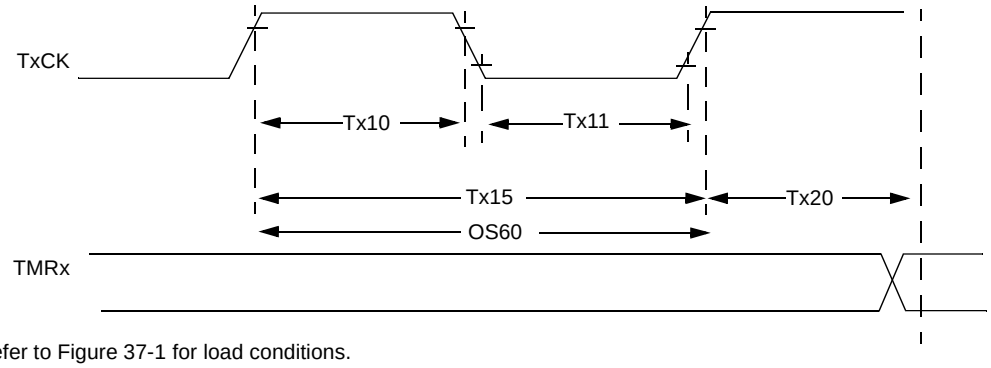
bit 2 **TROEN:** Trace Output Enable bit
1 = Enable trace outputs and start trace clock (trace probe must be present)
0 = Disable trace outputs and stop trace clock

bit 1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG
1 = 2-wire JTAG protocol uses TDO
0 = 2-wire JTAG protocol does not use TDO

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

FIGURE 37-6: TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

TABLE 37-25: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(2)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 20 ns or 2 TPBCLK3)/N] + 30 ns	—	—	ns	VDD > 2.7V (**Note 3**)
				[(Greater of 20 ns or 2 TPBCLK3)/N] + 50 ns	—	—	ns	VDD < 2.7V (**Note 3**)
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V
				50	—	—	ns	VDD < 2.7V
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	50	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPBCLK3	—

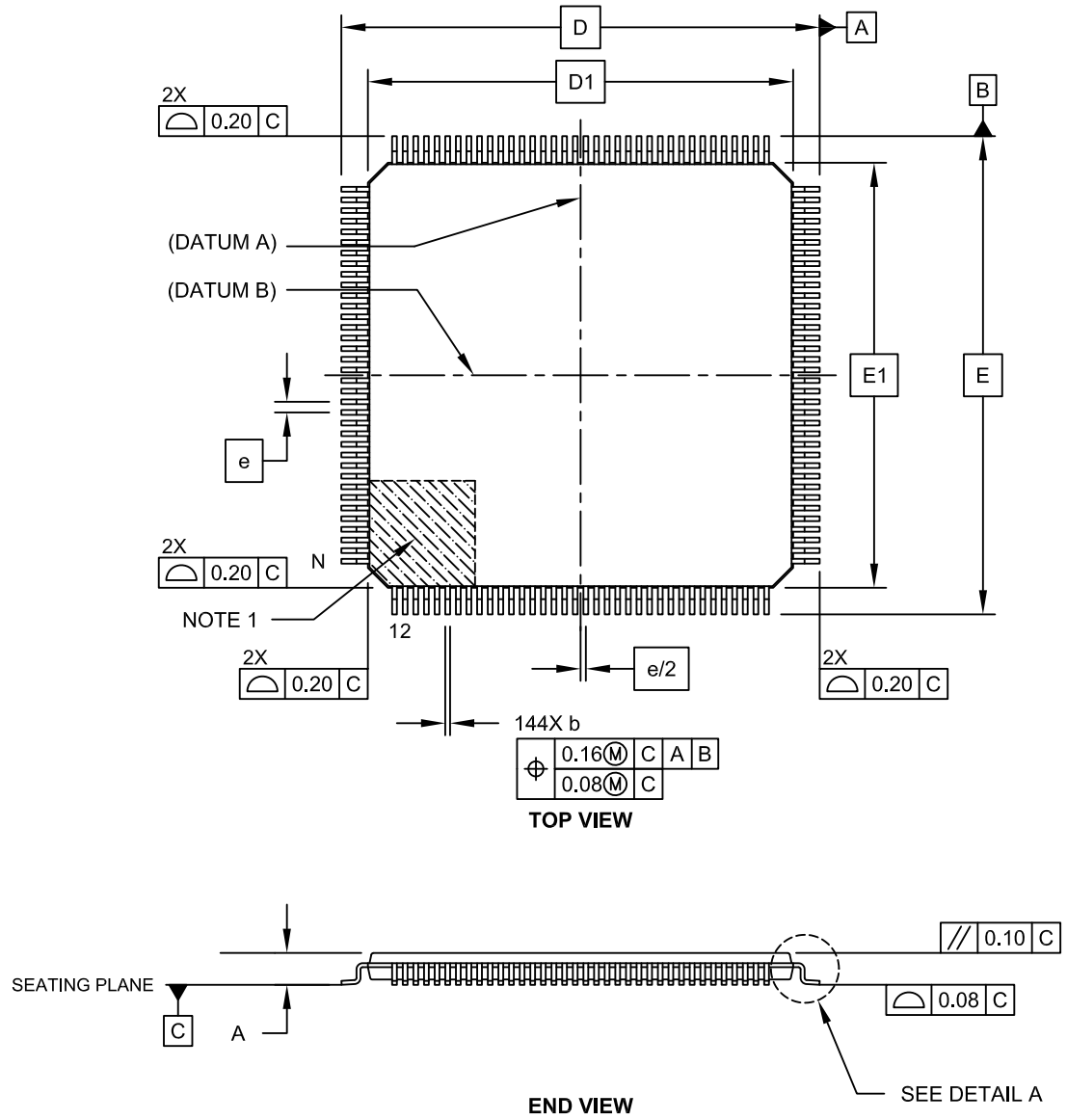
Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

144-Lead Plastic Thin Quad Flatpack (PH)-16x16x1mm Body, 2.00 mm Footprint [TQFP]

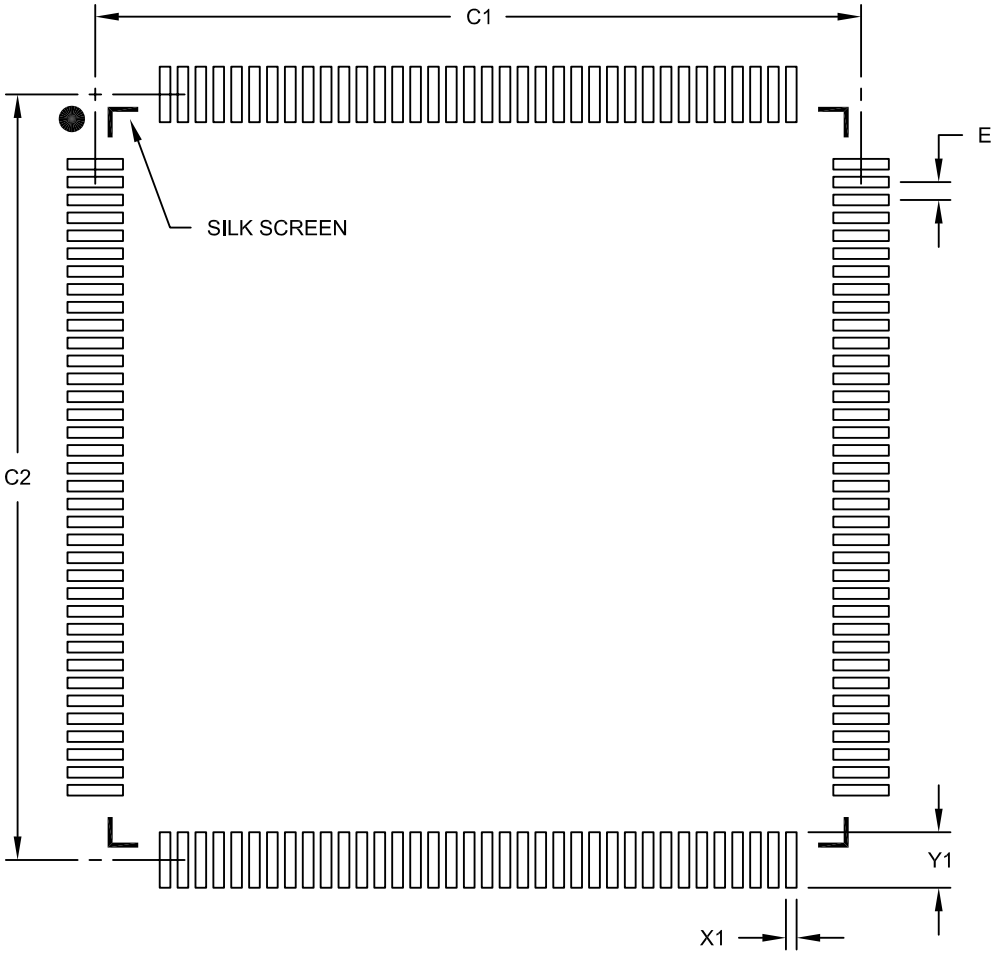
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-155B Sheet 1 of 2

144-Lead Plastic Low Profile Quad Flatpack (PL) - 20x20x1.40 mm Body [LQFP]
2.00 mm Footprint

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		21.40	
Contact Pad Spacing	C2		21.40	
Contact Pad Width (X144)	X1			0.30
Contact Pad Length (X144)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2044B