



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ecg144-i-pl

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Output Compare							
OC1	PPS	PPS	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	PPS	O	—	
OC6	PPS	PPS	PPS	PPS	O	—	
OC7	PPS	PPS	PPS	PPS	O	—	
OC8	PPS	PPS	PPS	PPS	O	—	
OC9	PPS	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	B24	62	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer

Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select

P = Power
 I = Input

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
External Interrupts							
INT0	46	71	A48	104	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer

Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select

P = Power
 I = Input

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-16: ETHERNET MII I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
ERXD0	61	41	B32	81	I	ST	Ethernet Receive Data 0
ERXD1	58	42	B26	66	I	ST	Ethernet Receive Data 1
ERXD2	57	43	A31	67	I	ST	Ethernet Receive Data 2
ERXD3	56	44	A40	82	I	ST	Ethernet Receive Data 3
ERXERR	64	35	A30	65	I	ST	Ethernet Receive Error Input
ERXDV	62	12	B40	101	I	ST	Ethernet Receive Data Valid
ERXCLK	63	16	B12	27	I	ST	Ethernet Receive Clock
ETXD0	2	86	A5	7	O	—	Ethernet Transmit Data 0
ETXD1	3	85	B4	8	O	—	Ethernet Transmit Data 1
ETXD2	43	79	B17	43	O	—	Ethernet Transmit Data 2
ETXD3	46	80	A22	44	O	—	Ethernet Transmit Data 3
ETXERR	50	87	B44	114	O	—	Ethernet Transmit Error
ETXEN	1	77	A57	120	O	—	Ethernet Transmit Enable
ETXCLK	51	78	B47	121	I	ST	Ethernet Transmit Clock
ECOL	44	10	B33	83	I	ST	Ethernet Collision Detect
ECRS	45	11	A47	100	I	ST	Ethernet Carrier Sense
EMDC	30	70	B39	99	O	—	Ethernet Management Data Clock
EMDIO	49	71	A55	115	I/O	—	Ethernet Management Data

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

TABLE 1-17: ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Ethernet MII Interface							
ERXD0	61	41	B32	81	I	ST	Ethernet Receive Data 0
ERXD1	58	42	B26	66	I	ST	Ethernet Receive Data 1
ERXERR	64	35	A30	65	I	ST	Ethernet Receive Error Input
ETXD0	2	86	A5	7	O	—	Ethernet Transmit Data 0
ETXD1	3	85	B4	8	O	—	Ethernet Transmit Data 1
ETXEN	1	77	A57	120	O	—	Ethernet Transmit Enable
EMDC	30	70	B39	99	O	—	Ethernet Management Data Clock
EMDIO	49	71	A55	115	I/O	—	Ethernet Management Data
EREFCLK	63	16	B12	27	I	ST	Ethernet Reference Clock
ECRSDV	62	12	B40	101	I	ST	Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

PIC32MZ Embedded Connectivity (EC) Family

FIGURE 4-5: BOOT AND ALIAS MEMORY MAP

Physical Memory Map ⁽¹⁾	
Sequence/Configuration Space ⁽³⁾	0x1FC70000 0x1FC6FF00
Boot Flash 2	0x1FC60000
Reserved	0x1FC54028
Serial Number ⁽⁵⁾	0x1FC54020
ADC Calibration Space ⁽³⁾	0x1FC54000
Sequence/Configuration Space ⁽⁴⁾	0x1FC50000 0x1FC4FF00
Boot Flash 1	0x1FC40000
Reserved	0x1FC34000
Unused Configuration Space ⁽⁶⁾	0x1FC30000 0x1FC2FF00
Upper Boot Alias	0x1FC20000
Reserved	0x1FC14000
Configuration Space ^(2,3)	0x1FC10000 0x1FC0FF00
Lower Boot Alias	0x1FC00000

Note 1: Memory areas are not shown to scale.

Note 2: Memory locations 0x1FC0FF40 through 0x1FC0FFFC are used to initialize Configuration registers (see **Section 34.0 “Special Features”**).

Note 3: Memory locations 0x1FC54000 through 0x1FC54010 are used to initialize the ADC Calibration registers (see **Section 34.0 “Special Features”**).

Note 4: Refer to **Section 4.1.1 “Boot Flash Sequence and Configuration Spaces”** for more information.

Note 5: Memory locations 0x1FC54020 and 0x1FC54024 contain a unique device serial number (see **Section 34.0 “Special Features”**).

Note 6: This configuration space cannot be used for executing code in the upper boot alias.

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
System Bus ⁽¹⁾	0xBF8F0000	0x0000
RNG	0xBF8E0000	0x6000
Crypto		0x5000
USB		0x3000
SQI1		0x2000
EBI		0x1000
Prefetch	0xBF880000	0x0000
Ethernet		0x2000
CAN1 and CAN2		0x0000
PORTA-PORTK	0xBF860000	0x0000
Comparator 1, 2	0xBF840000	0xC000
ADC1		0xB000
OC1-OC9		0x4000
IC1-IC9		0x2000
Timer1-Timer9	0xBF820000	0x0000
PMP		0xE000
UART1-UART6		0x2000
SPI1-SPI6		0x1000
I2C1-I2C5	0xBF810000	0x0000
DMA		0x1000
Interrupt Controller		0x0000
PPS	0xBF800000	0x1400
Oscillator		0x1200
CVREF		0x0E00
RTCC		0x0C00
Deadman Timer		0x0A00
Watchdog Timer		0x0800
Flash Controller		0x0600
Configuration		0x0000

Note 1: Refer to **4.2 “System Bus Arbitration”** for important legal information.

TABLE 4-3: BOOT FLASH 2 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC6_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF2DEVCFG3	31:0	Note: See Table 34-2 for the bit descriptions.																XXXX
FF44	ABF2DEVCFG2	31:0																	XXXX
FF48	ABF2DEVCFG1	31:0																	XXXX
FF4C	ABF2DEVCFG0	31:0																	XXXX
FF50	ABF2DEVCP3	31:0																	XXXX
FF54	ABF2DEVCP2	31:0																	XXXX
FF58	ABF2DEVCP1	31:0																	XXXX
FF5C	ABF2DEVCP0	31:0																	XXXX
FF60	ABF2DEVSIGN3	31:0																	XXXX
FF64	ABF2DEVSIGN2	31:0																	XXXX
FF68	ABF2DEVSIGN1	31:0																	XXXX
FF6C	ABF2DEVSIGN0	31:0																	XXXX
FF70	ABF2SEQ3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FF74	ABF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FF78	ABF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FF7C	ABF2SEQ0	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX
FFC0	BF2DEVCFG3	31:0	Note: See Table 34-1 for the bit descriptions.																XXXX
FFC4	BF2DEVCFG2	31:0																	XXXX
FFC8	BF2DEVCFG1	31:0																	XXXX
FFCC	BF2DEVCFG0	31:0																	XXXX
FFD0	BF2DEVCP3	31:0																	XXXX
FFD4	BF2DEVCP2	31:0																	XXXX
FFD8	BF2DEVCP1	31:0																	XXXX
FFDC	BF2DEVCP0	31:0																	XXXX
FFE0	BF2DEVSIGN3	31:0																	XXXX
FFE4	BF2DEVSIGN2	31:0																	XXXX
FFE8	BF2DEVSIGN1	31:0																	XXXX
FFEC	BF2DEVSIGN0	31:0																	XXXX
FFF0	BF2SEQ3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFF4	BF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFF8	BF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFFC	BF2SEQ0	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

PIC32MZ Embedded Connectivity (EC) Family

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 52. “Flash Program Memory with Support for Live Update”** (DS60001193), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MZ EC devices contain an internal Flash program memory for executing user code, which includes the following features:

- Two Flash banks for live update support
- Dual boot support
- Write protection for program and boot Flash
- ECC support

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 52. “Flash Program Memory with Support for Live Update”** (DS60001193) in the *“PIC32 Family Reference Manual”*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *“PIC32 Flash Programming Specification”* (DS60001145), which is available for download from the Microchip website.

Note: In PIC32MZ EC devices, the Flash page size is 16 KB (4096 IW) and the row size is 2 KB (512 IW).

7.1 CPU Exceptions

CPU coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® microAptiv™ MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Assertion of a software Reset.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480	—	DINT	—	—
NMI	Assertion of NMI signal.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Machine Check	TLB write that conflicts with an existing entry.	EBASE+0x180	MCHECK, EXL	—	0x18	_general_exception_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2.	IPL<2:0>	—	0x00	See Table 7-2.
Deferred Watch	Deferred watch (unmasked by K DM=>!(K DM) transition).	EBASE+0x180	WP, EXL	—	0x17	_general_exception_handler
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480	—	DIB	—	—
WATCH	A reference to an address that is in one of the Watch registers (fetch).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Fetch address alignment error. Fetch reference to protected address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
TLBL	Fetch TLB miss or fetch TLB hit to page with V = 0.	EBASE if Status.EXL = 0	—	—	0x02	—
		EBASE+0x180 if Status.EXL == 1	—	—	0x02	_general_exception_handler
TLBL Execute Inhibit	An instruction fetch matched a valid TLB entry that had the XI bit set.	EBASE+0x180	EXL	—	0x14	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE+0x180	EXL	—	0x06	_general_exception_handler

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
0100	IEC4	31:16	U3TXIE	U3RXIE	U3EIE	SPI3TXIE	SPI3RXIE	SPI3EIE	ETHIE	CAN2IE ⁽³⁾	CAN1IE ⁽³⁾	I2C2MIE ⁽²⁾	I2C2SIE ⁽²⁾	I2C2BIE ⁽²⁾	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	0000	
		15:0	SPI2RXIE	SPI2EIE	DMA7IE	DMA6IE	DMA5IE	DMA4IE	DMA3IE	DMA2IE	DMA1IE	DMA0IE	USBDMAIE	USBIE	CMP2IE	CMP1IE	PMPEIE	PMPIE	0000	
0110	IEC5	31:16	—	U6TXIE	U6RXIE	U6EIE	SPI6TXIE ⁽²⁾	SPI6RXIE ⁽²⁾	SPI6IE ⁽²⁾	I2C5MIE	I2C5SIE	I2C5BIE	U5TXIE	U5RXIE	U5EIE	SPI5TXIE ⁽²⁾	SPI5RXIE ⁽²⁾	SPI5EIE ⁽²⁾	0000	
		15:0	I2C4MIE	I2C4SIE	I2C4BIE	U4TXIE	U4RXIE	U4EIE	SQ1IE	PREIE	FCEIE	RTCCIE	SPI4TXIE	SPI4RXIE	SPI4EIE	I2C3MIE	I2C3SIE	I2C3BIE	0000	
0140	IPC0	31:16	—	—	—	INT0IP<2:0>				INT0IS<1:0>			—	—	—	CS1IP<2:0>			CS1IS<1:0>	0000
		15:0	—	—	—	CS0IP<2:0>				CS0IS<1:0>			—	—	—	CTIP<2:0>			CTIS<1:0>	0000
0150	IPC1	31:16	—	—	—	OC1IP<2:0>				OC1IS<1:0>			—	—	—	IC1IP<2:0>			IC1IS<1:0>	0000
		15:0	—	—	—	IC1EIP<2:0>				IC1EIS<1:0>			—	—	—	T1IP<2:0>			T1IS<1:0>	0000
0160	IPC2	31:16	—	—	—	IC2IP<2:0>				IC2IS<1:0>			—	—	—	IC2EIP<2:0>			IC2EIS<1:0>	0000
		15:0	—	—	—	T2IP<2:0>				T2IS<1:0>			—	—	—	INT1IP<2:0>			INT1IS<1:0>	0000
0170	IPC3	31:16	—	—	—	IC3EIP<2:0>				IC3EIS<1:0>			—	—	—	T3IP<2:0>			T3IS<1:0>	0000
		15:0	—	—	—	INT2IP<2:0>				INT2IS<1:0>			—	—	—	OC2IP<2:0>			OC2IS<1:0>	0000
0180	IPC4	31:16	—	—	—	T4IP<2:0>				T4IS<1:0>			—	—	—	INT3IP<2:0>			INT3IS<1:0>	0000
		15:0	—	—	—	OC3IP<2:0>				OC3IS<1:0>			—	—	—	IC3IP<2:0>			IC3IS<1:0>	0000
0190	IPC5	31:16	—	—	—	INT4IP<2:0>				INT4IS<1:0>			—	—	—	OC4IP<2:0>			OC4IS<1:0>	0000
		15:0	—	—	—	IC4IP<2:0>				IC4IS<1:0>			—	—	—	IC4EIP<2:0>			IC4EIS<1:0>	0000
01A0	IPC6	31:16	—	—	—	OC5IP<2:0>				OC5IS<1:0>			—	—	—	IC5IP<2:0>			IC5IS<1:0>	0000
		15:0	—	—	—	IC5EIP<2:0>				IC5EIS<1:0>			—	—	—	T5IP<2:0>			T5IS<1:0>	0000
01B0	IPC7	31:16	—	—	—	OC6IP<2:0>				OC6IS<1:0>			—	—	—	IC6IP<2:0>			IC6IS<1:0>	0000
		15:0	—	—	—	IC6EIP<2:0>				IC6EIS<1:0>			—	—	—	T6IP<2:0>			T6IS<1:0>	0000
01C0	IPC8	31:16	—	—	—	OC7IP<2:0>				OC7IS<1:0>			—	—	—	IC7IP<2:0>			IC7IS<1:0>	0000
		15:0	—	—	—	IC7EIP<2:0>				IC7EIS<1:0>			—	—	—	T7IP<2:0>			T7IS<1:0>	0000
01D0	IPC9	31:16	—	—	—	OC8IP<2:0>				OC8IS<1:0>			—	—	—	IC8IP<2:0>			IC8IS<1:0>	0000
		15:0	—	—	—	IC8EIP<2:0>				IC8EIS<1:0>			—	—	—	T8IP<2:0>			T8IS<1:0>	0000
01E0	IPC10	31:16	—	—	—	OC9IP<2:0>				OC9IS<1:0>			—	—	—	IC9IP<2:0>			IC9IS<1:0>	0000
		15:0	—	—	—	IC9EIP<2:0>				IC9EIS<1:0>			—	—	—	T9IP<2:0>			T9IS<1:0>	0000
01F0	IPC11	31:16	—	—	—	AD1DC2IP<2:0>				AD1DC2IS<1:0>			—	—	—	AD1DC1IP<2:0>			AD1DC1IS<1:0>	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AD1IP<2:0>			AD1IS<1:0>	0000	
0200	IPC12	31:16	—	—	—	AD1DC6IP<2:0>				AD1DC6IS<1:0>			—	—	—	AD1DC5IP<2:0>			AD1DC5IS<1:0>	0000
		15:0	—	—	—	AD1DC4IP<2:0>				AD1DC4IS<1:0>			—	—	—	AD1DC3IP<2:0>			AD1DC3IS<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
0300	IPC28	31:16	—	—	—	I2C1BIP<2:0>			I2C1BIS<1:0>			—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
		15:0	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>			—	—	—	U1EIP<2:0>			U1EIS<1:0>		0000
0310	IPC29	31:16	—	—	—	CNBIP<2:0>			CNBIS<1:0>			—	—	—	CNAIP<2:0> ⁽²⁾			CNAIS<1:0> ⁽²⁾		0000
		15:0	—	—	—	I2C1MIP<2:0>			I2C1MIS<1:0>			—	—	—	I2C1SIP<2:0>			I2C1SIS<1:0>		0000
0320	IPC30	31:16	—	—	—	CNFIP<2:0>			CNFIS<1:0>			—	—	—	CNEIP<2:0>			CNEIS<1:0>		0000
		15:0	—	—	—	CNDIP<2:0>			CNDIS<1:0>			—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
0330	IPC31	31:16	—	—	—	CNKIP<2:0> ^(2,4,8)			CNKIS<1:0> ^(2,4,8)			—	—	—	CNJIP<2:0> ^(2,4)			CNJIS<1:0> ^(2,4)		0000
		15:0	—	—	—	CNHIP<2:0> ^(2,4)			CNHIS<1:0> ^(2,4)			—	—	—	CNGIP<2:0>			CNGIS<1:0>		0000
0340	IPC32	31:16	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>			—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
		15:0	—	—	—	PMPEIP<2:0>			PMPEIS<1:0>			—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
0350	IPC33	31:16	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>			—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
		15:0	—	—	—	USBDMAIP<2:0>			USBDMAIS<1:0>			—	—	—	USBIP<2:0>			USBIS<1:0>		0000
0360	IPC34	31:16	—	—	—	DMA5IP<2:0>			DMA5IS<1:0>			—	—	—	DMA4IP<2:0>			DMA4IS<1:0>		0000
		15:0	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>			—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
0370	IPC35	31:16	—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>			—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		0000
		15:0	—	—	—	DMA7IP<2:0>			DMA7IS<1:0>			—	—	—	DMA6IP<2:0>			DMA6IS<1:0>		0000
0380	IPC36	31:16	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>			—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
		15:0	—	—	—	U2EIP<2:0>			U2EIS<1:0>			—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		0000
0390	IPC37	31:16	—	—	—	CAN1IP<2:0> ⁽³⁾			CAN1IS<1:0> ⁽³⁾			—	—	—	I2C2MIP<2:0> ⁽²⁾			I2C2MIS<1:0> ⁽²⁾		0000
		15:0	—	—	—	I2C2SIP<2:0> ⁽²⁾			I2C2SIS<1:0> ⁽²⁾			—	—	—	I2C2BIP<2:0> ⁽²⁾			I2C2BIS<1:0> ⁽²⁾		0000
03A0	IPC38	31:16	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>			—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		0000
		15:0	—	—	—	ETHIP<2:0>			ETHIS<1:0>			—	—	—	CAN2IP<2:0> ⁽³⁾			CAN2IS<1:0> ⁽³⁾		0000
03B0	IPC39	31:16	—	—	—	U3TXIP<2:0>			U3TXIS<1:0>			—	—	—	U3RXIP<2:0>			U3RXIS<1:0>		0000
		15:0	—	—	—	U3EIP<2:0>			U3EIS<1:0>			—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
03C0	IPC40	31:16	—	—	—	SPI4EIP<2:0>			SPI4EIS<1:0>			—	—	—	I2C3MIP<2:0>			I2C3MIS<1:0>		0000
		15:0	—	—	—	I2C3SIP<2:0>			I2C3SIS<1:0>			—	—	—	I2C3BIP<2:0>			I2C3BIS<1:0>		0000
03D0	IPC41	31:16	—	—	—	FCEIP<2:0>			FCEIS<1:0>			—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
		15:0	—	—	—	SPI4TXIP<2:0>			SPI4TXIS<1:0>			—	—	—	SPI4RXIP<2:0>			SPI4RXIS<1:0>		0000
03E0	IPC42	31:16	—	—	—	U4RXIP<2:0>			U4RXIS<1:0>			—	—	—	U4EIP<2:0>			U4EIS<1:0>		0000
		15:0	—	—	—	SQI1IP<2:0>			SQI1IS<1:0>			—	—	—	PREIP<2:0>			PREIS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 10-10: DCHxSSA: DMA CHANNEL x SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.

Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL x DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHDSA<31:0>**: Channel Destination Start Address bits
Channel destination start address.

Note: This must be the physical address of the destination.

TABLE 12-13: PORTF REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TRISF5	TRISF4	TRISF3	—	TRISF1	TRISF0	003B
0520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	RF5	RF4	RF3	—	RF1	RF0	xxxx
0530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	LATF5	LATF4	LATF3	—	LATF1	LATF0	xxxx
0540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ODCF5	ODCF4	ODCF3	—	ODCF1	ODCF0	0000
0550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CNPUF5	CNPUF4	CNPUF3	—	CNPUF1	CNPUF0	0000
0560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CNPDF5	CNPDF4	CNPDF3	—	CNPDF1	CNPDF0	0000
0570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CNIEF5	CNIEF4	CNIEF3	—	CNIEF1	CNIEF0	0000
0590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CN STATF5	CN STATF4	CN STATF3	—	CN STATF1	CN STATF0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 12-22: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1620	RPE8R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE8R<3:0>				0000
1624	RPE9R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE9R<3:0>				0000
1640	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF0R<3:0>				0000
1644	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF1R<3:0>				0000
1648	RPF2R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF2R<3:0>				0000
164C	RPF3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF3R<3:0>				0000
1650	RPF4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF4R<3:0>				0000
1654	RPF5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF5R<3:0>				0000
1660	RPF8R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF8R<3:0>				0000
1670	RPF12R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG12R<3:0>				0000
1674	RPF13R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG0R<3:0>				0000
1680	RPG0R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1684	RPG1R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1698	RPG6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG6R<3:0>				0000
169C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG7R<3:0>				0000
16A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG8R<3:0>				0000
16A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG9R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
2: This register is not available on 64-pin and 100-pin devices.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:

1 = External clock input is synchronized

0 = External clock input is not synchronized

When TCS = 0:

This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit

1 = External clock from T1CKI pin

0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 20-3: SQ11CFG: SQI CONFIGURATION REGISTER (CONTINUED)

- bit 9 **WP:** Write Protect bit
In Single Lane or Dual Lane mode, this bit is used to drive the SQID2 pin, which can be used with devices with a write-protect pin. The meaning of the values for this bit will depend on the device to which SQID2 is connected.
- bit 8 **SERMODE:** Serial Flash Mode Select bit
1 = Hardware ignores CPHA and CPOL bit settings and sends and latches negative edge of SQI CLK
0 = Clock phase and polarity are controlled by the CPHA and CPOL bit settings
- bit 7 **RXLATCH:** RX Latch Control During TX Mode bit
1 = RX Data sent to RX FIFO when CMDINIT<1:0> (SQICON<17:16>) is set to TX
0 = RX Data is discarded when CMDINIT (SQICON<17:16>) is set to TX
- bit 6 **Unimplemented:** Read as '0'
- bit 5 **LSBF:** Data Format Select bit
1 = LSB is sent or received first
0 = MSB is sent or received first
- bit 4 **CPOL:** Clock Polarity Select bit
1 = Active-low SQICLK (SQICLK high is the Idle state)
0 = Active-high SQICLK (SQICLK low is the Idle state)
- bit 3 **CPHA:** Clock Phase Select bit
1 = SQICLK starts toggling at the start of the first data bit
0 = SQICLK starts toggling at the middle of the first data bit
- bit 2-0 **MODE<2:0>:** Mode Select bits
111 = Reserved
•
•
•
100 = Reserved
011 = XIP mode is selected (when this mode is entered, the module behaves as if executing in place (XIP), but uses the register data to control timing)
010 = DMA mode is selected
001 = CPU mode is selected (the module is controlled by the CPU in PIO mode. This mode is entered when leaving Boot or XIP mode)
000 = Reserved

Note 1: This bit must be programmed as '1'.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 22-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 7-6 **URXISEL<1:0>**: Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least one data character)
- bit 5 **ADDEN**: Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE**: Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received
- bit 3 **PERR**: Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected
- bit 2 **FERR**: Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected
- bit 1 **OERR**: Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed
- bit 0 **URXDA**: Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

- bit 3 **CS1P:** Chip Select 1 Polarity bit⁽¹⁾
 1 = Active-high (PMCS1)
 0 = Active-low (PMCS1)
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **WRSP:** Write Strobe Polarity bit
 For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
 1 = Write strobe active-high (PMWR)
 0 = Write strobe active-low (PMWR)
 For Master mode 1 (MODE<1:0> = 11):
 1 = Enable strobe active-high (PMENB)
 0 = Enable strobe active-low (PMENB)
- bit 0 **RDSP:** Read Strobe Polarity bit
 For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
 1 = Read Strobe active-high (PMRD)
 0 = Read Strobe active-low (PMRD)
 For Master mode 1 (MODE<1:0> = 11):
 1 = Read/write strobe active-high (PMRD/PMWR)
 0 = Read/write strobe active-low (PMRD/PMWR)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

PIC32MZ Embedded Connectivity (EC) Family

27.0 RANDOM NUMBER GENERATOR (RNG)

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. “Crypto Engine (CE) and Random Number Generator (RNG)”** (DS60001246), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Random Number Generator (RNG) core implements a thermal noise-based, True Random Number Generator (TRNG) and a cryptographically secure Pseudo-Random Number Generator (PRNG).

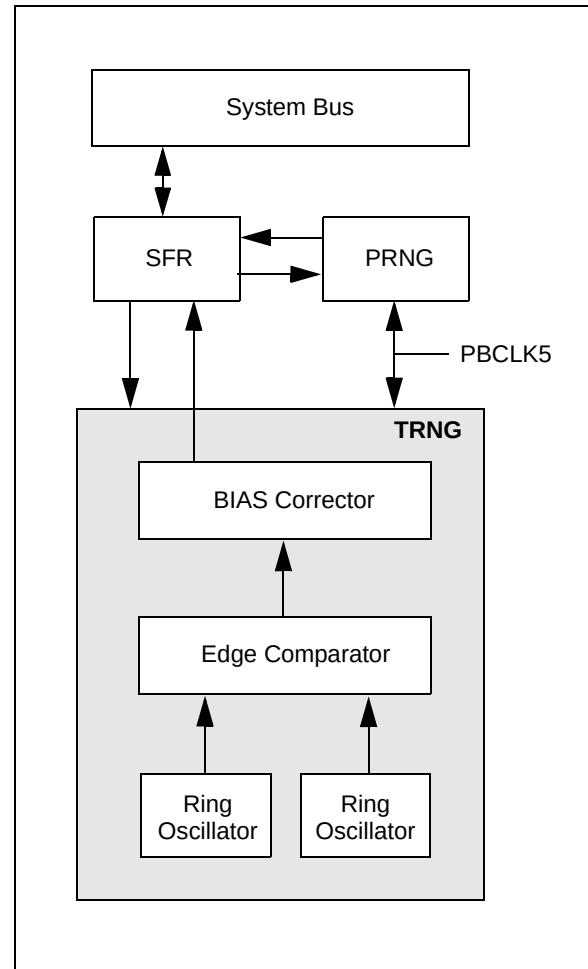
The TRNG uses multiple ring oscillators and the inherent thermal noise of integrated circuits to generate true random numbers that can initialize the PRNG.

The PRNG is a flexible LSFR, which is capable of manifesting a maximal length LFSR of up to 64-bits.

The following are some of the key features of the Random Number Generator:

- TRNG:
 - Up to 25 Mbps of random bits
 - Multi-Ring Oscillator based design
 - Built-in Bias Corrector
- PRNG:
 - LSFR-based
 - Up to 64-bit polynomial length
 - Programmable polynomial
 - TRNG can be seed value

TABLE 27-1: RANDOM NUMBER GENERATOR BLOCK DIAGRAM



PIC32MZ Embedded Connectivity (EC) Family

REGISTER 29-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4 (CONTINUED)

- bit 15 **FLTEN17**: Filter 13 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 14-13 **MSEL17<1:0>**: Filter 17 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL17<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN16**: Filter 16 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 6-5 **MSEL16<1:0>**: Filter 16 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL16<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 30-38: EMAC1SA1: ETHERNET CONTROLLER MAC STATION ADDRESS 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR4<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR3<7:0>							

Legend:

R = Readable bit

W = Writable bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR4<7:0>:** Station Address Octet 4 bits

These bits hold the fourth transmitted octet of the station address.

bit 7-0 **STNADDR3<7:0>:** Station Address Octet 3 bits

These bits hold the third transmitted octet of the station address.

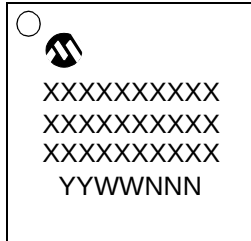
- Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.
- 2:** This register is loaded at reset from the factory preprogrammed station address.

PIC32MZ Embedded Connectivity (EC) Family

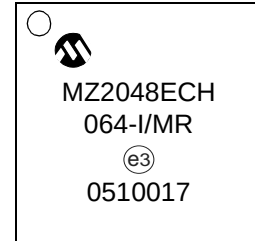
39.0 PACKAGING INFORMATION

39.1 Package Marking Information

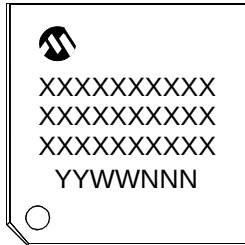
64-Lead QFN (9x9x0.9 mm)



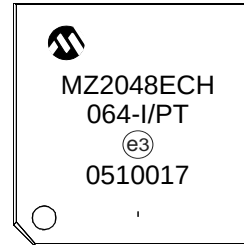
Example



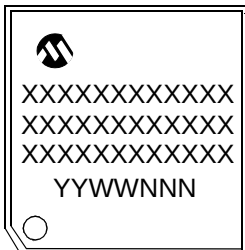
64-Lead TQFP (10x10x1 mm)



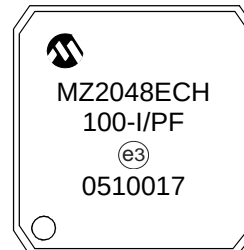
Example



100-Lead TQFP (14x14x1 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.		

PIC32MZ Embedded Connectivity (EC) Family

A.7 Interrupts and Exceptions

The key difference between Interrupt Controllers in PIC32MX5XX/6XX/7XX devices and PIC32MZ devices concerns vector spacing. Previous PIC32MX devices had fixed vector spacing, which is adjustable in set increments, and every interrupt had the same amount of space. PIC32MZ devices replace this with a variable offset spacing, where each interrupt has an offset register to determine where to begin execution.

In addition, the IFSx, IECx, and IPCx registers for old peripherals have shifted to different registers due to new peripherals. Please refer to **Section 7.0 “CPU Exceptions and Interrupt Controller”** to determine where the interrupts are now located.

Table A-8 lists differences (indicated by **Bold** type) in the registers that will affect software migration.

TABLE A-8: INTERRUPT DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
Vector Spacing	
On PIC32MX devices, the vector spacing was determined by the VS field in the CPU core. VS<4:0> (IntCtl<9:5>: CP0 Register 12, Select 1) 10000 = 512-byte vector spacing 01000 = 256-byte vector spacing 00100 = 128-byte vector spacing 00010 = 64-byte vector spacing 00001 = 32-byte vector spacing 00000 = 0-byte vector spacing	On PIC32MZ devices, the vector spacing is variable and determined by the Interrupt controller. The VOFFx<17:1> bits in the OFFx register are set to the offset from EBASE where the interrupt service routine is located. VOFFx<17:1> (OFFx<17:1>) Interrupt Vector ‘x’ Address Offset bits
Shadow Register Sets	
On PIC32MX devices, there was one shadow register set which could be used during interrupt processing. Which interrupt priority could use the shadow register set was determined by the FSRSEL field in DEVCFG3 and SS0 on INTCON. FSRSEL<2:0> (DEVCFG3<18:16>) 111 = Assign Interrupt Priority 7 to a shadow register set 110 = Assign Interrupt Priority 6 to a shadow register set • • 001 = Assign Interrupt Priority 1 to a shadow register set 000 = All interrupt priorities are assigned to a shadow register set SS0 (INTCON<16>) 1 = Single vector is presented with a shadow register set 0 = Single vector is not presented with a shadow register set	On PIC32MZ devices, there are seven shadow register sets, and each priority level can be assigned a shadow register set to use via the PRIS<3:0> bits in the PRIS register. The SS0 bit is also moved to PRIS<0>. PRIS<3:0> PRIS<y:z> 1xxx = Reserved (by default, an interrupt with a priority level of x uses Shadow Set 0) 0111 = Interrupt with a priority level of x uses Shadow Set 7 0110 = Interrupt with a priority level of x uses Shadow Set 6 • • 0001 = Interrupt with a priority level of x uses Shadow Set 1 0000 = Interrupt with a priority level of x uses Shadow Set 0 SS0 (PRIS<0>) 1 = Single vector is presented with a shadow register set 0 = Single vector is not presented with a shadow register set
Status	
PIC32MX devices, the VEC<5:0> bits show which interrupt is being serviced. VEC<5:0> (INTSTAT<5:0>) 11111-00000 = The interrupt vector that is presented to the CPU	On PIC32MZ devices, the SIRQ<7:0> bits show the IRQ number of the interrupt last serviced. SIRQ<7:0> (INTSTAT<7:0>) 11111111-00000000 = The last interrupt request number serviced by the CPU