# Microchip Technology - PIC32MZ1024ECG144T-I/PL Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | EBI/EMI, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 48x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ecg144t-i-pl |

## Device Pin Tables

### TABLE 2: PIN NAMES FOR 64-PIN DEVICES

**64-PIN QFN(4) AND TQFP (TOP VIEW)**

**PIC32MZ0512EC(E/F/K)064**
**PIC32MZ1024EC(G/H/M)064**
**PIC32MZ1024EC(E/F/K)064**
**PIC32MZ2048EC(G/H/M)064**

64 1

**QFN(4)**

64 1

**TQFP**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN17/ETXEN/RPE5/PMD5/RE5 | 33 | VBUS |
| 2 | AN16/ETXD0/PMD6/RE6 | 34 | VUSB3V3 |
| 3 | AN15/ETXD1/PMD7/RE7 | 35 | VSS |
| 4 | AN14/C1IND/RPG6/SCK2/PMA5/RG6 | 36 | D- |
| 5 | AN13/C1INC/RPG7/SDA4/PMA4/RG7 | 37 | D+ |
| 6 | AN12/C2IND/RPG8/SCL4/PMA3/RG8 | 38 | RPF3/USBID/RF3 |
| 7 | VSS | 39 | VDD |
| 8 | VDD | 40 | VSS |
| 9 | $\overline{\text{MCLR}}$ | 41 | RPF4/SDA5/PMA9/RF4 |
| 10 | AN11/C2INC/RPG9/PMA2/RG9 | 42 | RPF5/SCL5/PMA8/RF5 |
| 11 | AN45/C1INA/RPB5/RB5 | 43 | AERXD0/ETXD2/RPD9/SDA1/PMCS2/PMA15/RD9 |
| 12 | AN4/C1INB/RB4 | 44 | ECOL/RPD10/SCL1/SCK4/RD10 |
| 13 | AN3/C2INA/RPB3/RB3 | 45 | AERXCLK/AEREFCLK/ECRS/RPD11/PMCS1/PMA14/RD11 |
| 14 | AN2/C2INB/RPB2/RB2 | 46 | AERXD1/ETXD3/RPD0/RTCC/INT0/RD0 |
| 15 | PGEC1/VREF-/CVREF-/AN1/RPB1/RB1 | 47 | SOSCI/RPC13/RC13 |
| 16 | PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0 | 48 | SOSCO/RPC14/T1CK/RC14 |
| 17 | PGEC2/AN46/RPB6/RB6 | 49 | EMDIO/AEMDIO/RPD1/SCK1/RD1 |
| 18 | PGED2/AN47/RPB7/RB7 | 50 | ETXERR/AETXEN/RPD2/SDA3/RD2 |
| 19 | AVDD | 51 | AERXERR/ETXCLK/RPD3/SCL3/RD3 |
| 20 | AVss | 52 | $\overline{\text{SQICS0}}$/RPD4/PMWR/RD4 |
| 21 | AN48/RPB8/PMA10/RB8 | 53 | $\overline{\text{SQICS1}}$/RPD5/PMRD/RD5 |
| 22 | AN49/RPB9/PMA7/RB9 | 54 | VDD |
| 23 | TMS/CVREFOUT/AN5/RPB10/PMA13/RB10 | 55 | VSS |
| 24 | TDO/AN6/PMA12/RB11 | 56 | ERXD3/AETXD1/RPF0/RF0 |
| 25 | VSS | 57 | TRCLK/SQICLK/ERXD2/AETXD0/RPF1/RF1 |
| 26 | VDD | 58 | TRD0/SQID0/ERXD1/PMD0/RE0 |
| 27 | TCK/AN7/PMA11/RB12 | 59 | VSS |
| 28 | TDI/AN8/RB13 | 60 | VDD |
| 29 | AN9/RPB14/SCK3/PMA1/RB14 | 61 | TRD1/SQID1/ERXD0/PMD1/RE1 |
| 30 | AN10/EMDC/AEMDC/RPB15/OCFB/PMA0/RB15 | 62 | TRD2/SQID2/ERXDV/ECRSDV/AECRSDV/PMD2/RE2 |
| 31 | OSC1/CLKI/RC12 | 63 | TRD3/SQID3/ERXCLK/EREFCLK/RPE3/PMD3/RE3 |
| 32 | OSC2/CLKO/RC15 | 64 | AN18/ERXERR/PMD4/RE4 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select (PPS)"** for restrictions.

**2:** Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.

**4:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**TABLE 1-1: ADC1 PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-pin QFN/ TQFP | 100-pin TQFP | 124-pin VTLA | 144-pin TQFP/ LQFP | | | |
| AN0 | 16 | 25 | A18 | 36 | I | Analog | Analog Input Channels |
| AN1 | 15 | 24 | A17 | 35 | I | Analog | |
| AN2 | 14 | 23 | A16 | 34 | I | Analog | |
| AN3 | 13 | 22 | A14 | 31 | I | Analog | |
| AN4 | 12 | 21 | A13 | 26 | I | Analog | |
| AN5 | 23 | 34 | B19 | 49 | I | Analog | |
| AN6 | 24 | 35 | A24 | 50 | I | Analog | |
| AN7 | 27 | 41 | A27 | 59 | I | Analog | |
| AN8 | 28 | 42 | B23 | 60 | I | Analog | |
| AN9 | 29 | 43 | A28 | 61 | I | Analog | |
| AN10 | 30 | 44 | B24 | 62 | I | Analog | |
| AN11 | 10 | 16 | B9 | 21 | I | Analog | |
| AN12 | 6 | 12 | B7 | 16 | I | Analog | |
| AN13 | 5 | 11 | A8 | 15 | I | Analog | |
| AN14 | 4 | 10 | B6 | 14 | I | Analog | |
| AN15 | 3 | 5 | A4 | 5 | I | Analog | |
| AN16 | 2 | 4 | B2 | 4 | I | Analog | |
| AN17 | 1 | 3 | A3 | 3 | I | Analog | |
| AN18 | 64 | 100 | A67 | 144 | I | Analog | |
| AN19 | — | 9 | A7 | 13 | I | Analog | |
| AN20 | — | 8 | B5 | 12 | I | Analog | |
| AN21 | — | 7 | A6 | 11 | I | Analog | |
| AN22 | — | 6 | B3 | 6 | I | Analog | |
| AN23 | — | 1 | A2 | 1 | I | Analog | |
| AN24 | — | 17 | A11 | 22 | I | Analog | |
| AN25 | — | 18 | B10 | 23 | I | Analog | |
| AN26 | — | 19 | A12 | 24 | I | Analog | |
| AN27 | — | 28 | B15 | 39 | I | Analog | |
| AN28 | — | 29 | A20 | 40 | I | Analog | |
| AN29 | — | 38 | B21 | 56 | I | Analog | |
| AN30 | — | 39 | A26 | 57 | I | Analog | |
| AN31 | — | 40 | B22 | 58 | I | Analog | |
| AN32 | — | 47 | B27 | 69 | I | Analog | |
| AN33 | — | 48 | A32 | 70 | I | Analog | |
| AN34 | — | 2 | B1 | 2 | I | Analog | |
| AN35 | — | — | A5 | 7 | I | Analog | |

**Legend:** CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

**TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0568 | OFF010 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 056C | OFF011 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0570 | OFF012 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0574 | OFF013 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0578 | OFF014 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 057C | OFF015 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0580 | OFF016 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0584 | OFF017 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0588 | OFF018 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 058C | OFF019 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0590 | OFF020 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0594 | OFF021 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0598 | OFF022 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 059C | OFF023 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 05A0 | OFF024 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
**2:** This bit or register is not available on 64-pin devices.
**3:** This bit or register is not available on devices without a CAN module.
**4:** This bit or register is not available on 100-pin devices.
**5:** Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
**6:** Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
**7:** This bit or register is not available on devices without a Crypto module.
**8:** This bit or register is not available on 124-pin devices.

**REGISTER 11-20: USBDMAINT: USB DMA INTERRUPT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-0, HS |
| | DMA8IF | DMA7IF | DMA6IF | DMA5IF | DMA4IF | DMA3IF | DMA2IF | DMA1IF |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **DMAxIF:** DMA Channel 'x' Interrupt bit

1 = The DMA channel has an interrupt event

0 = No interrupt event

All bits are cleared on a read of the register.

**REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1 (CONTINUED)**

bit 16 **LPMXMT:** LPM Transition to the L1 State bit

When in *Device mode*:

1 = USB module will transition to the L1 state upon the receipt of the next LPM transaction. LPMEN must be set to '0b11. Both LPMXMT and LPMEN must be set in the same cycle.

0 = Maintain current state

When LPMXMT and LPMEN are set, the USB module can respond in the following ways:

- If no data is pending (all TX FIFOs are empty), the USB module will respond with an ACK. The bit will self clear and a software interrupt will be generated.
- If data is pending (data resides in at least one TX FIFO), the USB module will respond with a NYET. In this case, the bit will not self clear however a software interrupt will be generated.

When in *Host mode*:

1 = USB module will transmit an LPM transaction. This bit is self clearing, and will be immediately cleared upon receipt of any Token or three time-outs have occurred.

0 = Maintain current state

bit 15-12 **ENDPOINT<3:0>:** LPM Token Packet Endpoint bits

This is the endpoint in the token packet of the LPM transaction.

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **RMTWAK:** Remote Wake-up Enable bit

This bit is applied on a temporary basis only and is only applied to the current suspend state.

1 = Remote wake-up is enabled

0 = Remote wake-up is disabled

bit 7-4 **HIRD<3:0>:** Host Initiated Resume Duration bits

The minimum time the host will drive resume on the bus. The value in this register corresponds to an actual resume time of:

Resume Time = 50 µs + HIRD * 75 µs. The resulting range is 50 µs to 1200 µs.

bit 3-0 **LNKSTATE<3:0>:** Link State bits

This value is provided by the host to the peripheral to indicate what state the peripheral must transition to after the receipt and acceptance of a LPM transaction. The only valid value for this register is '1' for Sleep State (L1). All other values are reserved.

**REGISTER 21-2: I2CxSTAT: I$^2$C STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0, HS, HC | R-0, HS, HC | R/C-0, HS, HC | U-0 | U-0 | R/C-0, HS | R-0, HS, HC | R-0, HS, HC |
| | ACKSTAT | TRSTAT | ACKTIM | — | — | BCL | GCSTAT | ADD10 |
| 7:0 | R/C-0, HS | R/C-0, HS | R-0, HS, HC | R/C-0, HS, HC | R/C-0, HS, HC | R-0, HS, HC | R-0, HS, HC | R-0, HS, HC |
| | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |

| Legend: | HS = Hardware Set | HC = Hardware Cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | C = Clearable bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I$^2$C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I$^2$C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (Valid in I$^2$C Slave mode only)
1 = I$^2$C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I$^2$C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

## 24.1 EBI Control Registers

**TABLE 24-2: EBI REGISTER MAP**

| Virtual Address (BF8E_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1014 | EBICS0(1) | 31:16 | CSADDR<15:0> | | | | | | | | | | | | | | | | 2000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 1018 | EBICS1(2) | 31:16 | CSADDR<15:0> | | | | | | | | | | | | | | | | 1000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 101C | EBICS2(2) | 31:16 | CSADDR<15:0> | | | | | | | | | | | | | | | | 2040 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 1020 | EBICS3(2) | 31:16 | CSADDR<15:0> | | | | | | | | | | | | | | | | 1040 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 1054 | EBIMSK0(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | REGSEL<2:0> | | | MEMTYPE<2:0> | | | MEMSIZE<4:0> | | | | | 0020 |
| 1058 | EBIMSK1(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | REGSEL<2:0> | | | MEMTYPE<2:0> | | | MEMSIZE<4:0> | | | | | 0020 |
| 105C | EBIMSK2(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | REGSEL<2:0> | | | MEMTYPE<2:0> | | | MEMSIZE<4:0> | | | | | 0120 |
| 1060 | EBIMSK3(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | REGSEL<2:0> | | | MEMTYPE<2:0> | | | MEMSIZE<4:0> | | | | | 0120 |
| 1094 | EBISMT0 | 31:16 | — | — | — | — | — | RDYMODE | PAGESIZE<1:0> | | PAGEMODE | TPRC<3:0> | | | | TBTA<2:0> | | | 041C |
| | | 15:0 | TWP<5:0> | | | | | | TWR<1:0> | | TAS<1:0> | | TRC<5:0> | | | | | | 2D4B |
| 1098 | EBISMT1 | 31:16 | — | — | — | — | — | RDYMODE | PAGESIZE<1:0> | | PAGEMODE | TPRC<3:0> | | | | TBTA<2:0> | | | 041C |
| | | 15:0 | TWP<5:0> | | | | | | TWR<1:0> | | TAS<1:0> | | TRC<5:0> | | | | | | 2D4B |
| 109C | EBISMT2 | 31:16 | — | — | — | — | — | RDYMODE | PAGESIZE<1:0> | | PAGEMODE | TPRC<3:0> | | | | TBTA<2:0> | | | 041C |
| | | 15:0 | TWP<5:0> | | | | | | TWR<1:0> | | TAS<1:0> | | TRC<5:0> | | | | | | 2d$b |
| 10A0 | EBIFTRPD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | TRPD<11:0> | | | | | | | | | | | | 00C8 |
| 10A4 | EBISMCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SMDWIDTH2<2:0> | | | SMDWIDTH1<2:0> | | | SMDWIDTH0<2:0> | | | — | — | — | — | — | — | SMRP | 0201 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is not available on 64-pin devices.

**2:** This register is available on 144-pin devices only.

**REGISTER 26-9: CEHDLEN: CRYPTO ENGINE HEADER LENGTH REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HDRLEN<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **HDRLEN<7:0>:** DMA Header Length bits
For every packet, skip this length of locations and start filling the data.

**REGISTER 26-10: CETRLLEN: CRYPTO ENGINE TRAILER LENGTH REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TRLRLEN<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **TRLRLEN<7:0>:** DMA Trailer Length bits
For every packet, skip this length of locations at the end of the current packet and start putting the next packet.

## 27.1 RNG Control Registers

**TABLE 27-2: RANDOM NUMBER GENERATOR (RNG) REGISTER MAP**

| Virtual Address (BF8E_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6000 | RNGVER | 31:16 | ID<15:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | VERSION<7:0> | | | | | | | | REVISION<7:0> | | | | | | | | xxxx |
| 6004 | RNGCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | LOAD | — | CONT | PRNGEN | TRNGEN | PLEN<7:0> | | | | | | | | 0064 |
| 6008 | RNGPOLY1 | 31:16 | POLY<31:0> | | | | | | | | | | | | | | | | FFFF |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 600C | RNGPOLY2 | 31:16 | POLY<31:0> | | | | | | | | | | | | | | | | FFFF |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 6010 | RNGNUMGEN1 | 31:16 | RNG<31:0> | | | | | | | | | | | | | | | | FFFF |
| | | 15:0 | | | | | | | | | | | | | | | | | FFFF |
| 6014 | RNGNUMGEN2 | 31:16 | RNG<31:0> | | | | | | | | | | | | | | | | FFFF |
| | | 15:0 | | | | | | | | | | | | | | | | | FFFF |
| 6018 | RNGSEED1 | 31:16 | SEED<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 601C | RNGSEED2 | 31:16 | SEED<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 6020 | RNGCNT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | RCNT<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 28-13: AD1CMPn: ADC1 DIGITAL COMPARATOR REGISTER 'n' ('n' = 1, 2, 3, 4, 5 OR 6)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADCMPHI<15:8> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADCMPHI<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADCMPLO<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADCMPLO<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **ADCMPHI<15:0>:** Digital Analog Comparator High Limit Value bits

These bits store the high limit value, which is used for comparisons with the analog-to-digital conversion data. The user is responsible for formatting the data as signed or unsigned to match the data format as specified by the SHxMOD<1:0> bits for the associated S&H circuit and the FRACT bit.

bit 15-0 **ADCMPLO<15:0>:** Digital Analog Comparator Low Limit Value bits

These bits store the low limit value, which is used for comparisons with the analog-to-digital conversion data. The user is responsible for formatting the data as signed or unsigned to match the data format as specified by the SHxMOD<1:0> bits for the associated S&H circuit and the FRACT bit.

**Note:** Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

**REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | WAKFIL | — | — | — | SEG2PH<2:0>(1,4) | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SEG2PHTS(1) | SAM(2) | SEG1PH<2:0>(4) | | | PRSEG<2:0>(4) | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SJW<1:0>(3) | | BRP<5:0> | | | | | |

| Legend: | HC = Hardware Clear | S = Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | P = Programmable bit | r = Reserved bit |
| U = Unimplemented bit | -n = Bit Value at POR: (‘0’, ‘1’, x = Unknown) | | |

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as ‘0’

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

**Note 1:** SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
**2:** 3 Time bit sampling is not allowed for BRP < 2.
**3:** SJW ≤ SEG2PH.
**4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

**REGISTER 29-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)**

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 30-32: EMAC1MCMD: ETHERNET CONTROLLER MAC MII MANAGEMENT COMMAND REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | SCAN | READ |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **Unimplemented:** Read as '0'

bit 1 **SCAN:** MII Management Scan Mode bit
1 = The MII Management module will perform read cycles continuously (for example, useful for monitoring the Link Fail)
0 = Normal Operation

bit 0 **READ:** MII Management Read Command bit
1 = The MII Management module will perform a single read cycle. The read data is returned in the EMAC1MRDD register
0 = The MII Management module will perform a write cycle. The write data is taken from the EMAC1MWTD register

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

## 33.0 POWER-SAVING FEATURES

**Note:** This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This section describes power-saving features for the PIC32MZ EC devices. These devices offer various methods and modes that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

## 33.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the speed of PBCLK7, or selecting a lower power clock source (i.e., LPRC or SOSC).

In addition, the Peripheral Bus Scaling mode is available for each peripheral bus where peripherals are clocked at reduced speed by selecting a higher divider for the associated PBCLKx, or by disabling the clock completely.

## 33.2 Power-Saving with CPU Halted

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

### 33.2.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted and the associated clocks are disabled. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the peripheral bus clocks will start running and the device will enter into Idle mode.

### 33.2.2 IDLE MODE

In Idle mode, the CPU is Halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

## 36.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

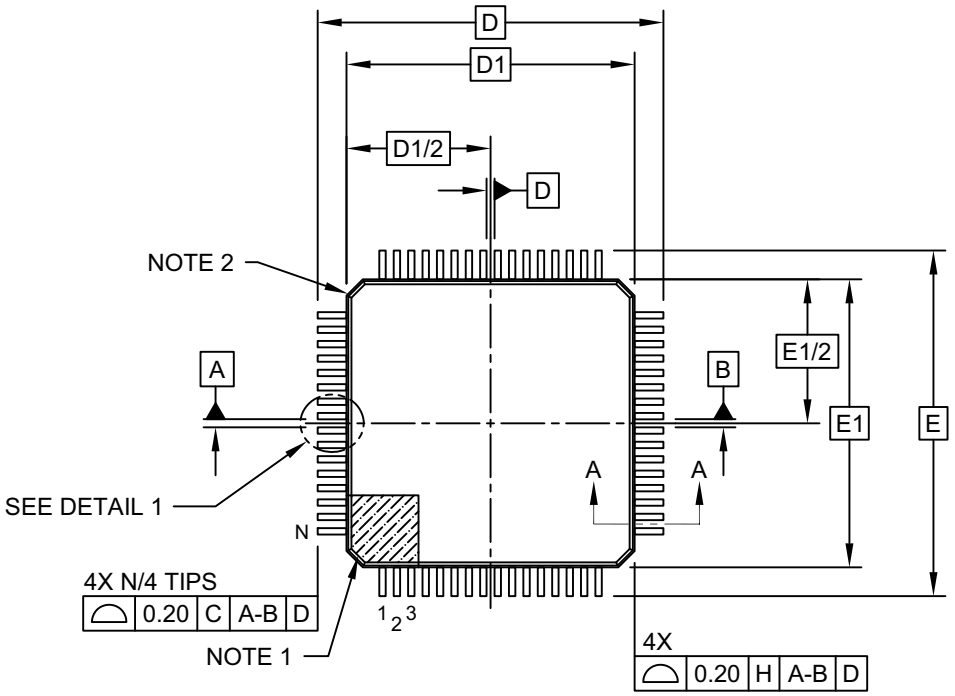
## 36.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

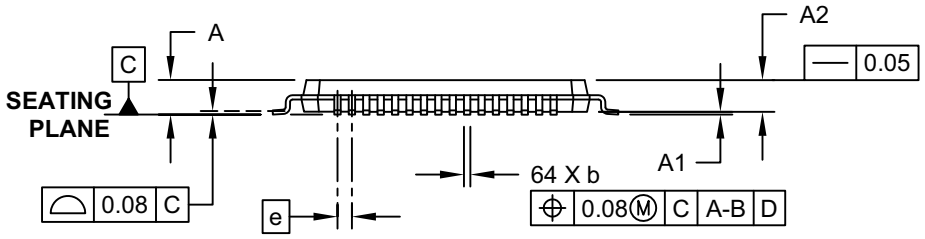
- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

**64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




TOP VIEW

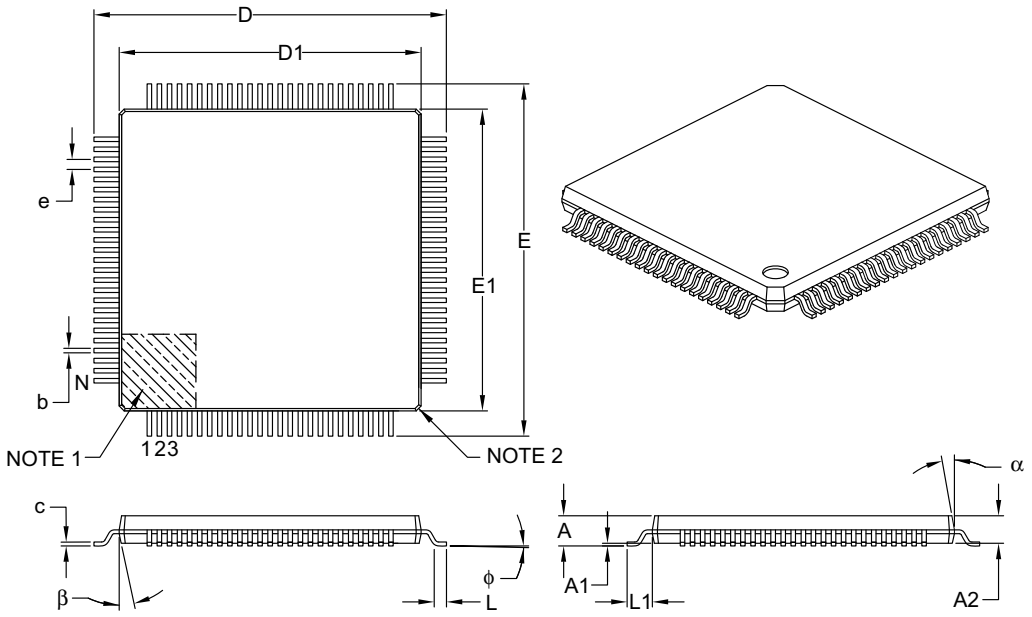



SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

### 100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.40 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 14.00 BSC | |
| Overall Length | D | | 14.00 BSC | |
| Molded Package Width | E1 | | 12.00 BSC | |
| Molded Package Length | D1 | | 12.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.13 | 0.18 | 0.23 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

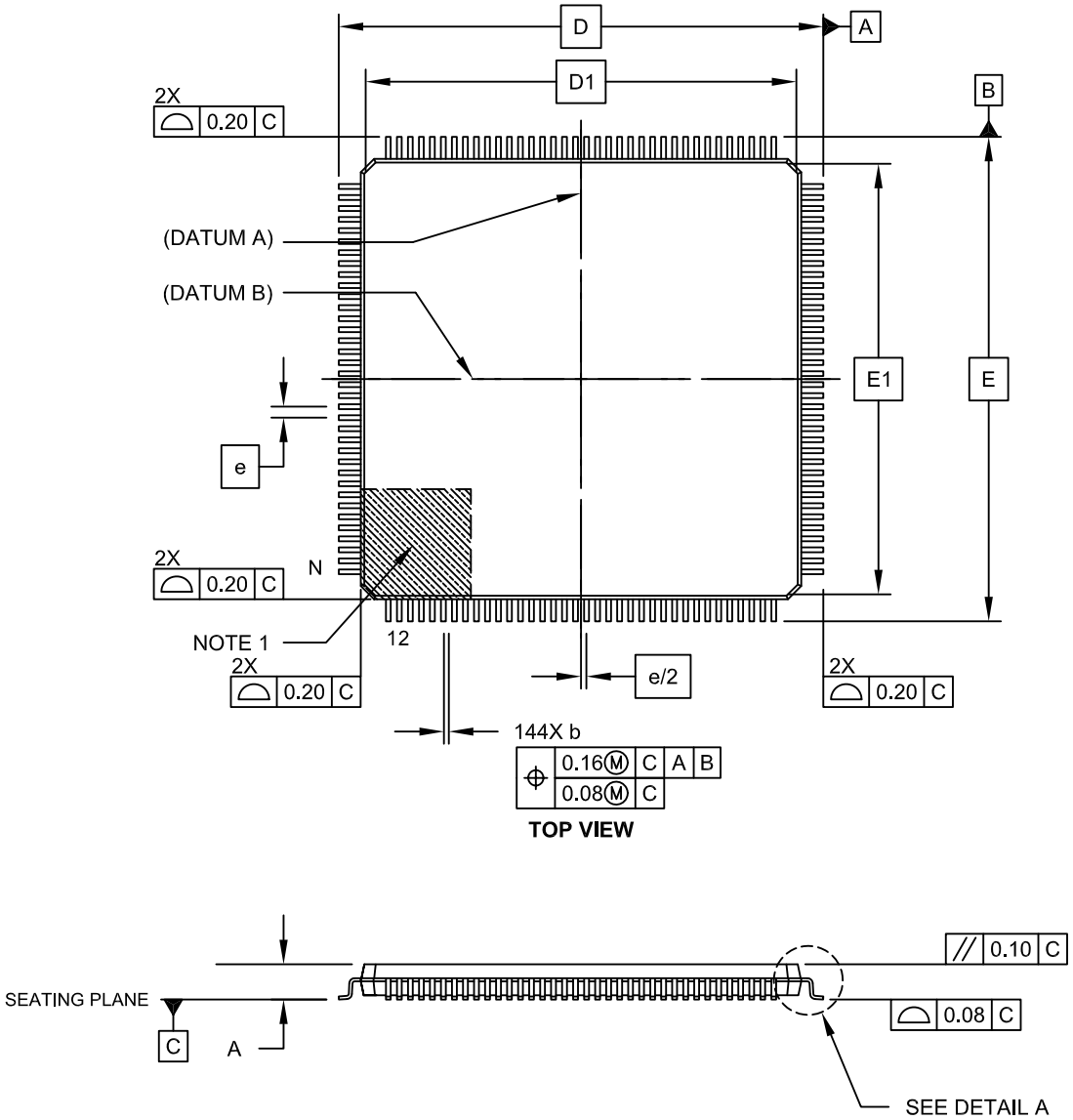
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

**144-Lead Plastic Low Profile Quad Flatpack (PL) – 20x20x1.40 mm Body, with 2.00 mm Footprint [LQFP]**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-044B Sheet 1 of 2

**TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES (CONTINUED)**

| PIC32MX5XX/6XX/7XX Feature | PIC32MZ Feature |
|---|---|
| **PLL Configuration** | |
| The FNOSC<2:0> and NOSC<2:0> bits select between POSC and FRC.<br>**FNOSC<2:0> (DEVCFG1<2:0>)**<br>**NOSC<2:0> (OSCCON<10:8>)** | Selection of which input clock (POSC or FRC) is now done through the FPLLICLK/PLLICLK bits.<br>**FPLLICLK (DEVCFG2<7>)**<br>**PLLICLK (SPLLCON<7>)** |
| On PIC32MX devices, the input frequency to the PLL had to be between 4 MHz and 5 MHz. FPLLIDIV selected how to divide the input frequency to give it the appropriate range.<br><br>FPLLIDIV<2:0> (DEVCFG2<2:0>)<br>**111 = 12x divider**<br>**110 = 10x divider**<br>101 = 6x divider<br>100 = 5x divider<br>011 = 4x divider<br>010 = 3x divider<br>001 = 2x divider<br>000 = 1x divider | On PIC32MZ devices, the input range for the PLL is wider (5 MHz to 64 MHz). The input divider values have changed, and new FPLLRNG/PLLRNG bits have been added to indicate under what range the input frequency falls.<br>FPLLIDIV<2:0> (DEVCFG2<2:0>)<br>**PLLIDIV<2:0> (SPLLCON<2:0>)**<br>**111 = Divide by 8**<br>**110 = Divide by 7**<br>101 = Divide by 6<br>100 = Divide by 5<br>011 = Divide by 4<br>010 = Divide by 3<br>001 = Divide by 2<br>000 = Divide by 1<br><br>**FPLLRNG<2:0> (DEVCFG2<6:4>)**<br>**PLLRNG<2:0> (SPLLCON<2:0>)**<br>**111 = Reserved**<br>**110 = Reserved**<br>**101 = 34-64 MHz**<br>**100 = 21-42 MHz**<br>**011 = 13-26 MHz**<br>**010 = 8-16 MHz**<br>**001 = 5-10 MHz**<br>**000 = Bypass** |
| On PIC32MX devices, the output frequency of PLL is between 60 MHz and 120 MHz. The PLL multiplier and divider bits configure the PLL for this range.<br>FPLLMUL<**2**:0> (DEVCFG2<**6:4**>)<br>PLLMULT<**2**:0> (OSCCON<18:16>)<br>**111 = 24x multiplier**<br>**110 = 21x multiplier**<br>**101 = 20x multiplier**<br>**100 = 19x multiplier**<br>**011 = 18x multiplier**<br>**010 = 17x multiplier**<br>**001 = 16x multiplier**<br>**000 = 15x multiplier**<br><br>FPLLODIV<2:0> (DEVCFG2<18:16>)<br>PLLODIV<2:0> (OSCCON<29:27>)<br>**111 = 24x multiplier**<br>**110 = 21x multiplier**<br>**101 = 20x multiplier**<br>**100 = 19x multiplier**<br>**011 = 18x multiplier**<br>**010 = 17x multiplier**<br>**001 = 16x multiplier**<br>**000 = 15x multiplier** | The PLL multiplier and divider on PIC32MZ devices have a wider range to accommodate the wider PLL specification range of 10 MHz to 200 MHz.<br>FPLLMUL**T**<**6**:0> (DEVCFG2<**14:8**>)<br>PLLMULT<**6**:0> (**SPLLCON<22:16>**)<br>**1111111 = Multiply by 128**<br>**1111110 = Multiply by 127**<br>**1111101 = Multiply by 126**<br>**1111100 = Multiply by 125**<br>•<br>•<br>•<br>**0000000 = Multiply by 1**<br><br>FPLLODIV<2:0> (DEVCFG2<18:16>)<br>PLLODIV<2:0> (**SPLLCON<26:24>**)<br>**111 = PLL Divide by 32**<br>**110 = PLL Divide by 32**<br>**101 = PLL Divide by 32**<br>**100 = PLL Divide by 16**<br>**011 = PLL Divide by 8**<br>**010 = PLL Divide by 4**<br>**001 = PLL Divide by 2**<br>**000 = PLL Divide by 2** |

## A.8 Flash Programming

The PIC32MZ family of devices incorporates a new Flash memory technology. Applications ported from PIC32MX5XX/6XX/7XX devices that take advantage of Run-time Self Programming will need to adjust the Flash programming steps to incorporate these changes.

Table A-9 lists the differences (indicated by **Bold** type) that will affect software migration.

**TABLE A-9: FLASH PROGRAMMING DIFFERENCES**

| PIC32MX5XX/6XX/7XX Feature | PIC32MZ Feature |
|---|---|
| **Program Flash Write Protection** | |
| On PIC32MX devices, the Program Flash write-protect bits are part of the Flash Configuration words (DEVCFG0).<br><br>PWP<**7**:0> (**DEVCFG0<19:12>**)<br>11111111 = Disabled<br>11111110 = 0xBD000FFF<br>11111101 = 0xBD001FFF<br>11111100 = 0xBD002FFF<br>11111011 = 0xBD003FFF<br>11111010 = 0xBD004FFF<br>11111001 = 0xBD005FFF<br>11111000 = 0xBD006FFF<br>11110111 = 0xBD007FFF<br>11110110 = 0xBD008FFF<br>11110101 = 0xBD009FFF<br>11110100 = 0xBD00AFFF<br>11110011 = 0xBD00BFFF<br>11110010 = 0xBD00CFFF<br>11110001 = 0xBD00DFFF<br>11110000 = 0xBD00EFFF<br>11101111 = 0xBD00FFFF<br>•<br>•<br>•<br>01111111 = 0xBD07FFFF | On PIC32MZ devices, the write-protect register is contained separately as the NVMPWP register. It has been expanded to 24 bits, and now represents the address below, which all Flash memory is protected. Note that the lower 14 bits are forced to zero, so that all memory locations in the page are protected.<br><br>PWP<**23**:0> (**NVMPWP<23:0>**)<br>Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>. When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected. |
| **Code Protection** | |
| On PIC32MX devices, code protection is enabled by the CP (**DEVCFG**<28>) bit. | On PIC32MZ devices, code protection is enabled by the CP (**DEVCP0**<28>) bit. |
| **Boot Flash Write Protection** | |
| On PIC32MX devices, Boot Flash write protection is enable by the **BWP (DEVCFG<24>)** bit and protects the entire Boot Flash memory. | On PIC32MZ devices, Boot Flash write protection is divided into pages and is enable by the **LBWPx** and **UBWPx** bits in the **NVMBWP** register. |
| **Low-Voltage Detect Status** | |
| LVDSTAT (NVMCON<11>)<br>1 = Low-voltage event is active<br>0 = Low-voltage event is not active | The LVDSTAT bit is not available in PIC32MZ devices. |