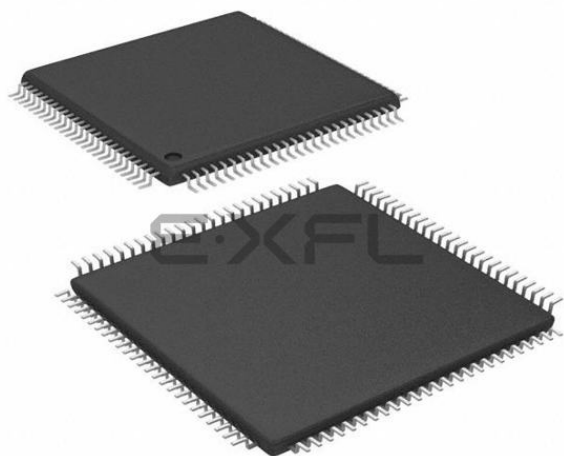




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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

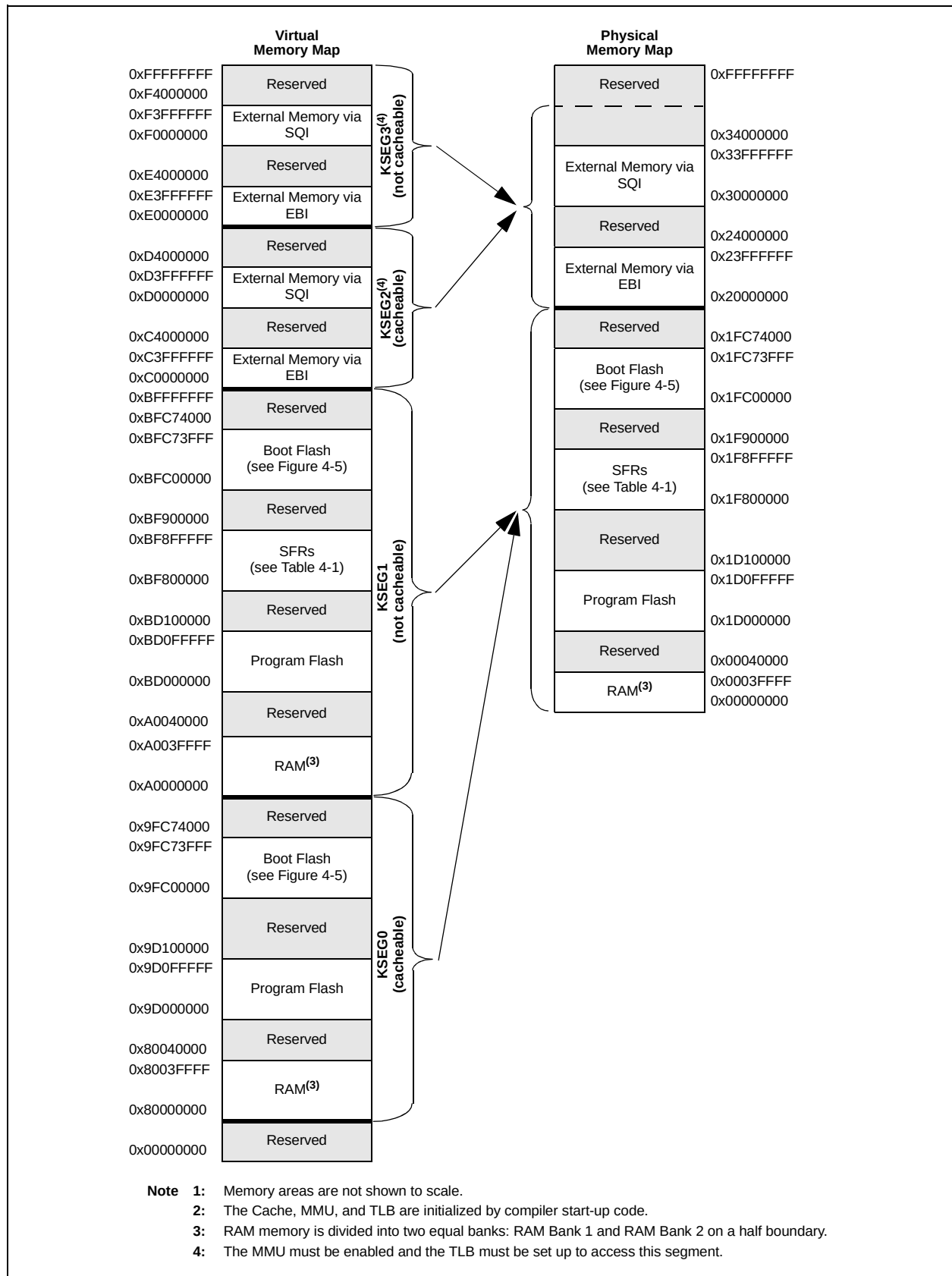
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                                   |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                            |
| Core Processor             | MIPS32® microAptiv™                                                                                                                                                               |
| Core Size                  | 32-Bit Single-Core                                                                                                                                                                |
| Speed                      | 200MHz                                                                                                                                                                            |
| Connectivity               | CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, SPI, SQI, UART/USART, USB OTG                                                                                                        |
| Peripherals                | Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT                                                                                                                      |
| Number of I/O              | 78                                                                                                                                                                                |
| Program Memory Size        | 1MB (1M x 8)                                                                                                                                                                      |
| Program Memory Type        | FLASH                                                                                                                                                                             |
| EEPROM Size                | -                                                                                                                                                                                 |
| RAM Size                   | 512K x 8                                                                                                                                                                          |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V                                                                                                                                                                       |
| Data Converters            | A/D 40x10b                                                                                                                                                                        |
| Oscillator Type            | Internal                                                                                                                                                                          |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                                 |
| Mounting Type              | Surface Mount                                                                                                                                                                     |
| Package / Case             | 100-TQFP                                                                                                                                                                          |
| Supplier Device Package    | 100-TQFP (14x14)                                                                                                                                                                  |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ech100t-i-pf">https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ech100t-i-pf</a> |

# PIC32MZ Embedded Connectivity (EC) Family

**FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 1024 KB OF PROGRAM MEMORY AND 256 KB OF RAM<sup>(1,2)</sup>**



**TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY**

| Virtual Address<br>(BFC4_#) | Register<br>Name | Bit Range | Bits                                                  |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | All Reset |
|-----------------------------|------------------|-----------|-------------------------------------------------------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|-----------|
|                             |                  |           | 31/15                                                 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 |           |
| FF40                        | ABF1DEVCFG3      | 31:0      | <b>Note:</b> See Table 34-2 for the bit descriptions. |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF44                        | ABF1DEVCFG2      | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF48                        | ABF1DEVCFG1      | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF4C                        | ABF1DEVCFG0      | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF50                        | ABF1DEVCP3       | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF54                        | ABF1DEVCP2       | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF58                        | ABF1DEVCP1       | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF5C                        | ABF1DEVCP0       | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF60                        | ABF1DEVSIGN3     | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF64                        | ABF1DEVSIGN2     | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF68                        | ABF1DEVSIGN1     | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF6C                        | ABF1DEVSIGN0     | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FF70                        | ABF1SEQ3         | 31:16     | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
|                             |                  | 15:0      | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
| FF74                        | ABF1SEQ2         | 31:16     | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
|                             |                  | 15:0      | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
| FF78                        | ABF1SEQ1         | 31:16     | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
|                             |                  | 15:0      | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
| FF7C                        | ABF1SEQ0         | 31:16     | CSEQ<15:0>                                            |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
|                             |                  | 15:0      | TSEQ<15:0>                                            |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFC0                        | BF1DEVCFG3       | 31:0      | <b>Note:</b> See Table 34-1 for the bit descriptions. |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFC4                        | BF1DEVCFG2       | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFC8                        | BF1DEVCFG1       | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFCC                        | BF1DEVCFG0       | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFD0                        | BF1DEVCP3        | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFD4                        | BF1DEVCP2        | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFD8                        | BF1DEVCP1        | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFDC                        | BF1DEVCP0        | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFE0                        | BF1DEVSIGN3      | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFE4                        | BF1DEVSIGN2      | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFE8                        | BF1DEVSIGN1      | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFEC                        | BF1DEVSIGN0      | 31:0      |                                                       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
| FFF0                        | BF1SEQ3          | 31:16     | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
|                             |                  | 15:0      | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
| FFF4                        | BF1SEQ2          | 31:16     | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
|                             |                  | 15:0      | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
| FFF8                        | BF1SEQ1          | 31:16     | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
|                             |                  | 15:0      | —                                                     | —     | —     | —     | —     | —     | —    | —    | —    | —    | —    | —    | —    | —    | —    | XXXX |           |
| FFFC                        | BF1SEQ0          | 31:16     | CSEQ<15:0>                                            |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |
|                             |                  | 15:0      | TSEQ<15:0>                                            |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      | XXXX      |

**Legend:** x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

**TABLE 4-12: SYSTEM BUS TARGET 4 REGISTER MAP**

| Virtual Address<br>(BF8E_#) | Register<br>Name | Bit Range | Bits        |       |       |       |           |       |      |             |      |      |      |      |          |            |        | All<br>Resets |
|-----------------------------|------------------|-----------|-------------|-------|-------|-------|-----------|-------|------|-------------|------|------|------|------|----------|------------|--------|---------------|
|                             |                  |           | 31/15       | 30/14 | 29/13 | 28/12 | 27/11     | 26/10 | 25/9 | 24/8        | 23/7 | 22/6 | 21/5 | 20/4 | 19/3     | 18/2       | 17/1   |               |
| 9020                        | SBT4ELOG1        | 31:16     | MULTI       | —     | —     | —     | CODE<3:0> |       |      | —           | —    | —    | —    | —    | —        | —          | —      | 0000          |
|                             |                  | 15:0      | INITID<7:0> |       |       |       |           |       |      | REGION<3:0> |      |      |      | —    | CMD<2:0> |            |        | 0000          |
| 9024                        | SBT4ELOG2        | 31:16     | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | —      | 0000          |
|                             |                  | 15:0      | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | GROUP<1:0> |        | 0000          |
| 9028                        | SBT4ECON         | 31:16     | —           | —     | —     | —     | —         | —     | ERRP | —           | —    | —    | —    | —    | —        | —          | —      | 0000          |
|                             |                  | 15:0      | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | —      | 0000          |
| 9030                        | SBT4ECLRS        | 31:16     | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | —      | 0000          |
|                             |                  | 15:0      | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | CLEAR  | 0000          |
| 9038                        | SBT4ECLRM        | 31:16     | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | —      | 0000          |
|                             |                  | 15:0      | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | CLEAR  | 0000          |
| 9040                        | SBT4REG0         | 31:16     | BASE<21:6>  |       |       |       |           |       |      |             |      |      |      |      |          |            |        | xxxx          |
|                             |                  | 15:0      | BASE<5:0>   |       |       |       |           | PRI   | —    | SIZE<4:0>   |      |      |      |      | —        | —          | —      | xxxx          |
| 9050                        | SBT4RD0          | 31:16     | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | —      | xxxx          |
|                             |                  | 15:0      | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | GROUP3   | GROUP2     | GROUP1 | GROUP0        |
| 9058                        | SBT4WR0          | 31:16     | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | —      | xxxx          |
|                             |                  | 15:0      | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | GROUP3   | GROUP2     | GROUP1 | GROUP0        |
| 9080                        | SBT4REG2         | 31:16     | BASE<21:6>  |       |       |       |           |       |      |             |      |      |      |      |          |            |        | xxxx          |
|                             |                  | 15:0      | BASE<5:0>   |       |       |       |           | PRI   | —    | SIZE<4:0>   |      |      |      |      | —        | —          | —      | xxxx          |
| 9090                        | SBT4RD2          | 31:16     | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | —      | xxxx          |
|                             |                  | 15:0      | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | GROUP3   | GROUP2     | GROUP1 | GROUP0        |
| 9098                        | SBT4WR2          | 31:16     | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | —        | —          | —      | xxxx          |
|                             |                  | 15:0      | —           | —     | —     | —     | —         | —     | —    | —           | —    | —    | —    | —    | GROUP3   | GROUP2     | GROUP1 | GROUP0        |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note:** For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

# PIC32MZ Embedded Connectivity (EC) Family

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## REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ( 'x' = 0-13 ) (CONTINUED)

- bit 7-4    **REGION<3:0>**: Requested Region Number bits  
          1111 - 0000 = Target's region that reported a permission group violation
- bit 3     **Unimplemented**: Read as '0'
- bit 2-0   **CMD<2:0>**: Transaction Command of the Requester bits  
          111 = Reserved  
          110 = Reserved  
          101 = Write (a non-posted write)  
          100 = Reserved  
          011 = Read (a locked read caused by a Read-Modify-Write transaction)  
          010 = Read  
          001 = Write  
          000 = Idle

|                                                                                           |
|-------------------------------------------------------------------------------------------|
| <b>Note:</b> Refer to Table 4-6 for the list of available targets and their descriptions. |
|-------------------------------------------------------------------------------------------|

# PIC32MZ Embedded Connectivity (EC) Family

**REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | W-0            | W-0            | W-0            | W-0            | W-0            | W-0            | W-0           | W-0           |
|           | NVMKEY<31:24>  |                |                |                |                |                |               |               |
| 23:16     | W-0            | W-0            | W-0            | W-0            | W-0            | W-0            | W-0           | W-0           |
|           | NVMKEY<23:16>  |                |                |                |                |                |               |               |
| 15:8      | W-0            | W-0            | W-0            | W-0            | W-0            | W-0            | W-0           | W-0           |
|           | NVMKEY<15:8>   |                |                |                |                |                |               |               |
| 7:0       | W-0            | W-0            | W-0            | W-0            | W-0            | W-0            | W-0           | W-0           |
|           | NVMKEY<7:0>    |                |                |                |                |                |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **NVMKEY<31:0>**: Unlock Register bits

These bits are write-only, and read as '0' on any read

**Note:** This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

**REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7                | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-------------------------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | R/W-0                         | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | NVMADDR<31:24> <sup>(1)</sup> |                |                |                |                |                |               |               |
| 23:16     | R/W-0                         | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | NVMADDR<23:16> <sup>(1)</sup> |                |                |                |                |                |               |               |
| 15:8      | R/W-0                         | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | NVMADDR<15:8> <sup>(1)</sup>  |                |                |                |                |                |               |               |
| 7:0       | R/W-0                         | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | NVMADDR<7:0> <sup>(1)</sup>   |                |                |                |                |                |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **NVMADDR<31:0>**: Flash Address bits<sup>(1)</sup>

| NVMOP<3:0> Selection | Flash Address Bits (NVMADDR<31:0>)                                                     |
|----------------------|----------------------------------------------------------------------------------------|
| Page Erase           | Address identifies the page to erase (NVMADDR<13:0> are ignored).                      |
| Row Program          | Address identifies the row to program (NVMADDR<11:0> are ignored).                     |
| Word Program         | Address identifies the word to program (NVMADDR<1:0> are ignored).                     |
| Quad Word Program    | Address identifies the quad word (128-bit) to program (NVMADDR<3:0> bits are ignored). |

**Note 1:** For all other NVMOP<3:0> bit settings, the Flash address is ignored. See the NVMCON register (Register 5-1) for additional information on these bits.

**Note:** The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

## 6.1 Reset Control Registers

**TABLE 6-1: RESETS REGISTER MAP**

| Virtual Address<br>(BF80_#) | Register<br>Name | Bit Range | Bits  |       |       |       |         |          |      |      |             |      |      |      |       |      |      |       | All Resets |
|-----------------------------|------------------|-----------|-------|-------|-------|-------|---------|----------|------|------|-------------|------|------|------|-------|------|------|-------|------------|
|                             |                  |           | 31/15 | 30/14 | 29/13 | 28/12 | 27/11   | 26/10    | 25/9 | 24/8 | 23/7        | 22/6 | 21/5 | 20/4 | 19/3  | 18/2 | 17/1 | 16/0  |            |
| 1240                        | RCON             | 31:16     | —     | —     | —     | —     | BCFGERR | BCFGFAIL | —    | —    | —           | —    | —    | —    | —     | —    | —    | —     | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —       | —        | CMR  | —    | EXTR        | SWR  | DMTO | WDTO | SLEEP | IDLE | BOR  | POR   | 0000       |
| 1250                        | RSWRST           | 31:16     | —     | —     | —     | —     | —       | —        | —    | —    | —           | —    | —    | —    | —     | —    | —    | —     | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —       | —        | —    | —    | —           | —    | —    | —    | —     | —    | —    | SWRST | 0000       |
| 1260                        | RNMICON          | 31:16     | —     | —     | —     | —     | —       | —        | DMTO | WDTO | SWNMI       | —    | —    | —    | —     | —    | CF   | WDTS  | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —       | —        | —    | —    | NMICNT<7:0> |      |      |      |       |      |      |       | 0000       |
| 1270                        | PWRCON           | 31:16     | —     | —     | —     | —     | —       | —        | —    | —    | —           | —    | —    | —    | —     | —    | —    | —     | 0000       |
|                             |                  | 15:0      | —     | —     | —     | —     | —       | —        | —    | —    | —           | —    | —    | —    | —     | —    | —    | VREGS | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)**

| Virtual Address<br>(BF81_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits         |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | All Resets |
|-----------------------------|---------------------------------|-----------|--------------|-------|----------|-------|----------|-------|------|-------------|--------|--------|--------|--------|--------|--------|------------|------|------------|
|                             |                                 |           | 31/15        | 30/14 | 29/13    | 28/12 | 27/11    | 26/10 | 25/9 | 24/8        | 23/7   | 22/6   | 21/5   | 20/4   | 19/3   | 18/2   | 17/1       | 16/0 |            |
| 1390                        | DCH4SSA                         | 31:16     | CHSSA<31:0>  |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
|                             |                                 | 15:0      |              |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 13A0                        | DCH4DSA                         | 31:16     | CHDSA<31:0>  |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
|                             |                                 | 15:0      |              |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 13B0                        | DCH4SSIZ                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHSSIZ<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 13C0                        | DCH4DSIZ                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHDSIZ<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 13D0                        | DCH4SPTR                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHSPTR<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 13E0                        | DCH4DPTR                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHDPTR<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 13F0                        | DCH4CSIZ                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHCSIZ<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 1400                        | DCH4CPTR                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHCPTR<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 1410                        | DCH4DAT                         | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHPDAT<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 1420                        | DCH5CON                         | 31:16     | CHPIGN<7:0>  |       |          |       |          |       |      |             | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHBUSY       | —     | CHPIGNEN | —     | CHPATLEN | —     | —    | CHCHNS      | CHEN   | CHAED  | CHCHN  | CHAEN  | —      | CHEDET | CHPRI<1:0> | 0000 |            |
| 1430                        | DCH5ECON                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | CHAIRQ<7:0> |        |        |        |        |        |        |            | 00FF |            |
|                             |                                 | 15:0      | CHSIRQ<7:0>  |       |          |       |          |       |      |             | CFORCE | CABORT | PATEN  | SIRQEN | AIRQEN | —      | —          | —    | FF00       |
| 1440                        | DCH5INT                         | 31:16     | —            | —     | —        | —     | —        | —     | —    | CHSDIE      | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE     | 0000 |            |
|                             |                                 | 15:0      | —            | —     | —        | —     | —        | —     | —    | CHSDIF      | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF     | 0000 |            |
| 1450                        | DCH5SSA                         | 31:16     | CHSSA<31:0>  |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
|                             |                                 | 15:0      |              |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 1460                        | DCH5DSA                         | 31:16     | CHDSA<31:0>  |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
|                             |                                 | 15:0      |              |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 1470                        | DCH5SSIZ                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHSSIZ<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 1480                        | DCH5DSIZ                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHDSIZ<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |
| 1490                        | DCH5SPTR                        | 31:16     | —            | —     | —        | —     | —        | —     | —    | —           | —      | —      | —      | —      | —      | —      | —          | 0000 |            |
|                             |                                 | 15:0      | CHSPTR<15:0> |       |          |       |          |       |      |             |        |        |        |        |        |        |            |      | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.



# PIC32MZ Embedded Connectivity (EC) Family

**REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6        | Bit 29/21/13/5 | Bit 28/20/12/4           | Bit 27/19/11/3     | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|-----------------------|----------------|--------------------------|--------------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0                   | R/W-0          | R/W-0                    | R/W-0              | U-0            | U-0           | R/W-0         |
|           | —              | —                     | BYTO<1:0>      |                          | WBO <sup>(1)</sup> | —              | —             | BITO          |
| 23:16     | U-0            | U-0                   | U-0            | U-0                      | U-0                | U-0            | U-0           | U-0           |
|           | —              | —                     | —              | —                        | —                  | —              | —             | —             |
| 15:8      | U-0            | U-0                   | U-0            | R/W-0                    | R/W-0              | R/W-0          | R/W-0         | R/W-0         |
|           | —              | —                     | —              | PLEN<4:0> <sup>(1)</sup> |                    |                |               |               |
| 7:0       | R/W-0          | R/W-0                 | R/W-0          | U-0                      | U-0                | R/W-0          | R/W-0         | R/W-0         |
|           | CRCEN          | CRCAPP <sup>(1)</sup> | CRCTYP         | —                        | —                  | CRCCH<2:0>     |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (i.e., reverse source byte order)

00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit<sup>(1)</sup>

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)

0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits<sup>(1)</sup>

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

# PIC32MZ Embedded Connectivity (EC) Family

**REGISTER 11-17: USBE0FRST: USB END-OF-FRAME/SOFT RESET CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | R/W-0         | R/W-0         |
|           | —              | —              | —              | —              | —              | —              | NRSTX         | NRST          |
| 23:16     | R/W-0          | R/W-1          | R/W-1          | R/W-1          | R/W-0          | R.W-0          | R/W-1         | R/W-0         |
|           | LSEOF<7:0>     |                |                |                |                |                |               |               |
| 15:8      | R/W-0          | R/W-1          | R/W-1          | R/W-1          | R/W-0          | R.W-1          | R/W-1         | R/W-1         |
|           | FSEOF<7:0>     |                |                |                |                |                |               |               |
| 7:0       | R/W-1          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R.W-0          | R/W-0         | R/W-0         |
|           | HSEOF<7:0>     |                |                |                |                |                |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **NRSTX:** Reset of XCLK Domain bit

1 = Reset the XCLK domain, which is clock recovered from the received data by the PHY

0 = Normal operation

bit 24 **NRST:** Reset of CLK Domain bit

1 = Reset the CLK domain, which is clock recovered from the peripheral bus

0 = Normal operation

bit 23-16 **LSEOF<7:0>:** Low-Speed EOF bits

These bits set the Low-Speed transaction in units of 1.067  $\mu$ s (default setting is 121.6  $\mu$ s) prior to the EOF to stop new transactions from beginning.

bit 15-8 **FSEOF<7:0>:** Full-Speed EOF bits

These bits set the Full-Speed transaction in units of 533.3  $\mu$ s (default setting is 63.46  $\mu$ s) prior to the EOF to stop new transactions from beginning.

bit 7-0 **HSEOF<7:0>:** Hi-Speed EOF bits

These bits set the Hi-Speed transaction in units of 133.3  $\mu$ s (default setting is 17.07  $\mu$ s) prior to the EOF to stop new transactions from beginning.

**TABLE 12-5: PORTC REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY**

| Virtual Address<br>(BF86_#) | Register<br>Name(s) | Bit Range | Bits      |           |           |           |       |       |      |      |      |      |      |          |          |          |          |      | All<br>Resets |
|-----------------------------|---------------------|-----------|-----------|-----------|-----------|-----------|-------|-------|------|------|------|------|------|----------|----------|----------|----------|------|---------------|
|                             |                     |           | 31/15     | 30/14     | 29/13     | 28/12     | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4     | 19/3     | 18/2     | 17/1     | 16/0 |               |
| 0200                        | ANSEL               | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | ANSC4    | ANSC3    | ANSC2    | ANSC1    | —    | 001E          |
| 0210                        | TRISC               | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | TRISC15   | TRISC14   | TRISC13   | TRISC12   | —     | —     | —    | —    | —    | —    | —    | TRISC4   | TRISC3   | TRISC2   | TRISC1   | —    | F01E          |
| 0220                        | PORTC               | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | RC15      | RC14      | RC13      | RC12      | —     | —     | —    | —    | —    | —    | —    | RC4      | RC3      | RC2      | RC1      | —    | xxxx          |
| 0230                        | LATC                | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | LATC15    | LATC14    | LATC13    | LATC12    | —     | —     | —    | —    | —    | —    | —    | LATC4    | LATC3    | LATC2    | LATC1    | —    | xxxx          |
| 0240                        | ODCC                | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | ODCC15    | ODCC14    | ODCC13    | ODCC12    | —     | —     | —    | —    | —    | —    | —    | ODCC4    | ODCC3    | ODCC2    | ODCC1    | —    | 0000          |
| 0250                        | CNPUC               | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | CNPUC15   | CNPUC14   | CNPUC13   | CNPUC12   | —     | —     | —    | —    | —    | —    | —    | CNPUC4   | CNPUC3   | CNPUC2   | CNPUC1   | —    | 0000          |
| 0260                        | CNPDC               | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | CNPDC15   | CNPDC14   | CNPDC13   | CNPDC12   | —     | —     | —    | —    | —    | —    | —    | CNPDC4   | CNPDC3   | CNPDC2   | CNPDC1   | —    | 0000          |
| 0270                        | CNCONC              | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | ON        | —         | SIDL      | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
| 0280                        | CNENC               | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | CNIEC15   | CNIEC14   | CNIEC13   | CNIEC12   | —     | —     | —    | —    | —    | —    | —    | CNIEC4   | CNIEC3   | CNIEC2   | CNIEC1   | —    | 0000          |
| 0290                        | CNSTATC             | 31:16     | —         | —         | —         | —         | —     | —     | —    | —    | —    | —    | —    | —        | —        | —        | —        | —    | 0000          |
|                             |                     | 15:0      | CNSTATC15 | CNSTATC14 | CNSTATC13 | CNSTATC12 | —     | —     | —    | —    | —    | —    | —    | CNSTATC4 | CNSTATC3 | CNSTATC2 | CNSTATC1 | —    | 0000          |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

# 19.1 SPI Control Registers

**TABLE 19-1: SPI1 THROUGH SPI6 REGISTER MAP**

| Virtual Address<br>(BF82_#) | Register<br>Name(1) | Bit Range | Bits          |         |        |               |              |              |        |          |         |        |        |               |              |      |              |        | All Resets |
|-----------------------------|---------------------|-----------|---------------|---------|--------|---------------|--------------|--------------|--------|----------|---------|--------|--------|---------------|--------------|------|--------------|--------|------------|
|                             |                     |           | 31/15         | 30/14   | 29/13  | 28/12         | 27/11        | 26/10        | 25/9   | 24/8     | 23/7    | 22/6   | 21/5   | 20/4          | 19/3         | 18/2 | 17/1         | 16/0   |            |
| 1000                        | SPI1CON             | 31:16     | FRMEN         | FRMSYNC | FRMPOL | MSSSEN        | FRMSYPW      | FRMCNT<2:0>  |        |          | MCLKSEL | —      | —      | —             | —            | —    | SPIFE        | ENHBUF | 0000       |
|                             |                     | 15:0      | ON            | —       | SIDL   | DISSDO        | MODE32       | MODE16       | SMP    | CKE      | SSEN    | CKP    | MSTEN  | DISSDI        | STXISEL<1:0> |      | SRXISEL<1:0> |        | 0000       |
| 1010                        | SPI1STAT            | 31:16     | —             | —       | —      | RXBUFELM<4:0> |              |              |        |          | —       | —      | —      | TXBUFELM<4:0> |              |      |              |        | 0000       |
|                             |                     | 15:0      | —             | —       | —      | FRMERR        | SPIBUSY      | —            | —      | SPITUR   | SRMT    | SPIROV | SPIRBE | —             | SPITBE       | —    | SPITBF       | SPIRBF | 0008       |
| 1020                        | SPI1BUF             | 31:16     | DATA<31:0>    |         |        |               |              |              |        |          |         |        |        |               |              |      |              |        | 0000       |
|                             |                     | 15:0      |               |         |        |               |              |              |        |          |         |        |        |               |              |      |              |        | 0000       |
| 1030                        | SPI1BRG             | 31:16     | —             | —       | —      | —             | —            | —            | —      | —        | —       | —      | —      | —             | —            | —    | —            | —      | 0000       |
|                             |                     | 15:0      | —             | —       | —      | BRG<12:0>     |              |              |        |          |         |        |        |               |              |      |              |        | 0000       |
| 1040                        | SPI1CON2            | 31:16     | —             | —       | —      | —             | —            | —            | —      | —        | —       | —      | —      | —             | —            | —    | —            | —      | 0000       |
|                             |                     | 15:0      | SPI<br>SGNEXT | —       | —      | FRM<br>ERREN  | SPI<br>ROVEN | SPI<br>TUREN | IGNROV | IGNTUR   | AUDEN   | —      | —      | —             | AUD<br>MONO  | —    | AUDMOD<1:0>  |        | 0000       |
| 1200                        | SPI2CON             | 31:16     | FRMEN         | FRMSYNC | FRMPOL | MSSSEN        | FRMSYPW      | FRMCNT<2:0>  |        |          | MCLKSEL | —      | —      | —             | —            | —    | SPIFE        | ENHBUF | 0000       |
|                             |                     | 15:0      | ON            | —       | SIDL   | DISSDO        | MODE32       | MODE16       | SMP    | CKE      | SSEN    | CKP    | MSTEN  | DISSDI        | STXISEL<1:0> |      | SRXISEL<1:0> |        | 0000       |
| 1210                        | SPI2STAT            | 31:16     | —             | —       | —      | RXBUFELM<4:0> |              |              |        |          | —       | —      | —      | TXBUFELM<4:0> |              |      |              |        | 0000       |
|                             |                     | 15:0      | —             | —       | —      | FRMERR        | SPIBUSY      | —            | —      | SPITUR   | SRMT    | SPIROV | SPIRBE | —             | SPITBE       | —    | SPITBF       | SPIRBF | 0008       |
| 1220                        | SPI2BUF             | 31:16     | DATA<31:0>    |         |        |               |              |              |        |          |         |        |        |               |              |      |              |        | 0000       |
|                             |                     | 15:0      |               |         |        |               |              |              |        |          |         |        |        |               |              |      |              |        | 0000       |
| 1230                        | SPI2BRG             | 31:16     | —             | —       | —      | —             | —            | —            | —      | —        | —       | —      | —      | —             | —            | —    | —            | —      | 0000       |
|                             |                     | 15:0      | —             | —       | —      | —             | —            | —            | —      | BRG<8:0> |         |        |        |               |              |      |              |        |            |
| 1240                        | SPI2CON2            | 31:16     | —             | —       | —      | —             | —            | —            | —      | —        | —       | —      | —      | —             | —            | —    | —            | —      | 0000       |
|                             |                     | 15:0      | SPI<br>SGNEXT | —       | —      | FRM<br>ERREN  | SPI<br>ROVEN | SPI<br>TUREN | IGNROV | IGNTUR   | AUDEN   | —      | —      | —             | AUD<br>MONO  | —    | AUDMOD<1:0>  |        | 0000       |
| 1400                        | SPI3CON             | 31:16     | FRMEN         | FRMSYNC | FRMPOL | MSSSEN        | FRMSYPW      | FRMCNT<2:0>  |        |          | MCLKSEL | —      | —      | —             | —            | —    | SPIFE        | ENHBUF | 0000       |
|                             |                     | 15:0      | ON            | —       | SIDL   | DISSDO        | MODE32       | MODE16       | SMP    | CKE      | SSEN    | CKP    | MSTEN  | DISSDI        | STXISEL<1:0> |      | SRXISEL<1:0> |        | 0000       |
| 1410                        | SPI3STAT            | 31:16     | —             | —       | —      | RXBUFELM<4:0> |              |              |        |          | —       | —      | —      | TXBUFELM<4:0> |              |      |              |        | 0000       |
|                             |                     | 15:0      | —             | —       | —      | FRMERR        | SPIBUSY      | —            | —      | SPITUR   | SRMT    | SPIROV | SPIRBE | —             | SPITBE       | —    | SPITBF       | SPIRBF | 0008       |
| 1420                        | SPI3BUF             | 31:16     | DATA<31:0>    |         |        |               |              |              |        |          |         |        |        |               |              |      |              |        | 0000       |
|                             |                     | 15:0      |               |         |        |               |              |              |        |          |         |        |        |               |              |      |              |        | 0000       |
| 1430                        | SPI3BRG             | 31:16     | —             | —       | —      | —             | —            | —            | —      | —        | —       | —      | —      | —             | —            | —    | —            | —      | 0000       |
|                             |                     | 15:0      | —             | —       | —      | —             | —            | —            | —      | BRG<8:0> |         |        |        |               |              |      |              |        |            |
| 1440                        | SPI3CON2            | 31:16     | —             | —       | —      | —             | —            | —            | —      | —        | —       | —      | —      | —             | —            | —    | —            | —      | 0000       |
|                             |                     | 15:0      | SPI<br>SGNEXT | —       | —      | FRM<br>ERREN  | SPI<br>ROVEN | SPI<br>TUREN | IGNROV | IGNTUR   | AUDEN   | —      | —      | —             | AUD<br>MONO  | —    | AUDMOD<1:0>  |        | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

# PIC32MZ Embedded Connectivity (EC) Family

**REGISTER 20-8: SQI1INTEN: SQI INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | R/W-0          | R/W-0         | R/W-0         |
|           | —              | —              | —              | —              | —              | PKTCOMPIE      | BDDONEIE      | CONTHRIE      |
| 7:0       | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | CONEMPTYIE     | CONFULLIE      | RXTHRIE        | RXFULLIE       | RXEMPTYIE      | TXTHRIE        | TXFULLIE      | TXEMPTYIE     |

|                   |                                    |
|-------------------|------------------------------------|
| <b>Legend:</b>    | HS = Hardware Set                  |
| R = Readable bit  | W = Writable bit                   |
| -n = Value at POR | U = Unimplemented bit, read as '0' |
|                   | '1' = Bit is set                   |
|                   | '0' = Bit is cleared               |
|                   | x = Bit is unknown                 |

bit 31-11 **Unimplemented:** Read as '0'

bit 10 **PKTCOMPIE:** DMA Buffer Descriptor Packet Complete Interrupt Enable bit

1 = Interrupts are enabled  
0 = Interrupts are not enabled

bit 9 **BDDONEIE:** DMA Buffer Descriptor Done Interrupt Enable bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 8 **CONTHRIE:** Control Buffer Threshold Interrupt Enable bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 7 **CONEMPTYIE:** Control Buffer Empty Interrupt bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 6 **CONFULLIE:** Control Buffer Full Interrupt Enable bit

This bit enables an interrupt when the receive FIFO buffer is full.  
1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 5 **RXTHRIE:** Receive Buffer Threshold Interrupt Enable bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 4 **RXFULLIE:** Receive Buffer Full Interrupt Enable bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 3 **RXEMPTYIE:** Receive Buffer Empty Interrupt Enable bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 2 **TXTHRIE:** Transmit Threshold Interrupt Enable bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 1 **TXFULLIE:** Transmit Buffer Full Interrupt Enable bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

bit 0 **TXEMPTYIE:** Transmit Buffer Empty Interrupt Enable bit

1 = Interrupt is enabled  
0 = Interrupt is disabled

# PIC32MZ Embedded Connectivity (EC) Family

## REGISTER 20-22: SQI1INTSEN: SQI INTERRUPT SIGNAL ENABLE REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | R/W-0          | R/W-0         | R/W-0         |
|           | —              | —              | —              | —              | —              | PKT DONEISE    | BD DONEISE    | CON THRISE    |
| 7:0       | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | CON EMPTYISE   | CON FULLISE    | RX THRISE      | RX FULLISE     | RX EMPTYISE    | TX THRISE      | TX FULLISE    | TX EMPTYISE   |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10 **PKTDONEISE:** Receive Error Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 9 **BDDONEISE:** Transmit Error Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 8 **CONTHRISE:** Control Buffer Threshold Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 7 **CONEMPTYISE:** Control Buffer Empty Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 6 **CONFULLISE:** Control Buffer Full Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 5 **RXTHRISE:** Receive Buffer Threshold Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 4 **RXFULLISE:** Receive Buffer Full Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 3 **RXEMPTYISE:** Receive Buffer Empty Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 2 **TXTHRISE:** Transmit Buffer Threshold Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 1 **TXFULLISE:** Transmit Buffer Full Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

bit 0 **TXEMPTYISE:** Transmit Buffer Empty Interrupt Signal Enable bit

1 = Interrupt signal is enabled

0 = Interrupt signal is disabled

## 21.1 I<sup>2</sup>C Control Registers

**TABLE 21-1: I2C1 THROUGH I2C5 REGISTER MAP**

| Virtual Address<br>(BF82_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits    |        |        |        |        |       |        |       |       |                              |       |       |       |       |      |      | All Resets |
|-----------------------------|---------------------------------|-----------|---------|--------|--------|--------|--------|-------|--------|-------|-------|------------------------------|-------|-------|-------|-------|------|------|------------|
|                             |                                 |           | 31/15   | 30/14  | 29/13  | 28/12  | 27/11  | 26/10 | 25/9   | 24/8  | 23/7  | 22/6                         | 21/5  | 20/4  | 19/3  | 18/2  | 17/1 | 16/0 |            |
| 0000                        | I2C1CON                         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | PCIE                         | SCIE  | BOEN  | SDAHT | SBCDE | AHEN | DHEN | 0000       |
|                             |                                 | 15:0      | ON      | —      | SIDL   | SCLREL | STRICT | A10M  | DISSLW | SMEN  | GCEN  | STREN                        | ACKDT | ACKEN | RCEN  | PEN   | RSEN | SEN  | 1000       |
| 0010                        | I2C1STAT                        | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | ACKSTAT | TRSTAT | ACKTIM | —      | —      | BCL   | GCSTAT | ADD10 | IWCOL | I2COV                        | D/A   | P     | S     | R/W   | RBF  | TBF  | 0000       |
| 0020                        | I2C1ADD                         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Address Register             |       |       |       |       |      |      | 0000       |
| 0030                        | I2C1MSK                         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Address Mask Register        |       |       |       |       |      |      | 0000       |
| 0040                        | I2C1BRG                         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Baud Rate Generator Register |       |       |       |       |      |      | 0000       |
| 0050                        | I2C1TRN                         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Transmit Register            |       |       |       |       |      |      | 0000       |
| 0060                        | I2C1RCV                         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Receive Register             |       |       |       |       |      |      | 0000       |
| 0200                        | I2C2CON <sup>(2)</sup>          | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | PCIE                         | SCIE  | BOEN  | SDAHT | SBCDE | AHEN | DHEN | 0000       |
|                             |                                 | 15:0      | ON      | —      | SIDL   | SCLREL | STRICT | A10M  | DISSLW | SMEN  | GCEN  | STREN                        | ACKDT | ACKEN | RCEN  | PEN   | RSEN | SEN  | 1000       |
| 0210                        | I2C2STAT <sup>(2)</sup>         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | ACKSTAT | TRSTAT | ACKTIM | —      | —      | BCL   | GCSTAT | ADD10 | IWCOL | I2COV                        | D/A   | P     | S     | R/W   | RBF  | TBF  | 0000       |
| 0220                        | I2C2ADD <sup>(2)</sup>          | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Address Register             |       |       |       |       |      |      | 0000       |
| 0230                        | I2C2MSK <sup>(2)</sup>          | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Address Mask Register        |       |       |       |       |      |      | 0000       |
| 0240                        | I2C2BRG <sup>(2)</sup>          | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Baud Rate Generator Register |       |       |       |       |      |      | 0000       |
| 0250                        | I2C2TRN <sup>(2)</sup>          | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Transmit Register            |       |       |       |       |      |      | 0000       |
| 0260                        | I2C2RCV <sup>(2)</sup>          | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Receive Register             |       |       |       |       |      |      | 0000       |
| 0400                        | I2C3CON                         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | PCIE                         | SCIE  | BOEN  | SDAHT | SBCDE | AHEN | DHEN | 0000       |
|                             |                                 | 15:0      | ON      | —      | SIDL   | SCLREL | STRICT | A10M  | DISSLW | SMEN  | GCEN  | STREN                        | ACKDT | ACKEN | RCEN  | PEN   | RSEN | SEN  | 1000       |
| 0410                        | I2C3STAT                        | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | ACKSTAT | TRSTAT | ACKTIM | —      | —      | BCL   | GCSTAT | ADD10 | IWCOL | I2COV                        | D/A   | P     | S     | R/W   | RBF  | TBF  | 0000       |
| 0420                        | I2C3ADD                         | 31:16     | —       | —      | —      | —      | —      | —     | —      | —     | —     | —                            | —     | —     | —     | —     | —    | —    | 0000       |
|                             |                                 | 15:0      | —       | —      | —      | —      | —      | —     | —      | —     | —     | Address Register             |       |       |       |       |      |      | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

**2:** This register is not available on 64-pin devices.

# PIC32MZ Embedded Connectivity (EC) Family

## 24.0 EXTERNAL BUS INTERFACE (EBI)

**Note:** This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 47. “External Bus Interface (EBI)”** (DS60001245), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The External Bus Interface (EBI) module provides a high-speed, convenient way to interface external parallel memory devices to the PIC32MZ EC family device.

With the EBI module, it is possible to connect asynchronous SRAM and NOR Flash devices, as well as non-memory devices such as camera sensors and LCDs.

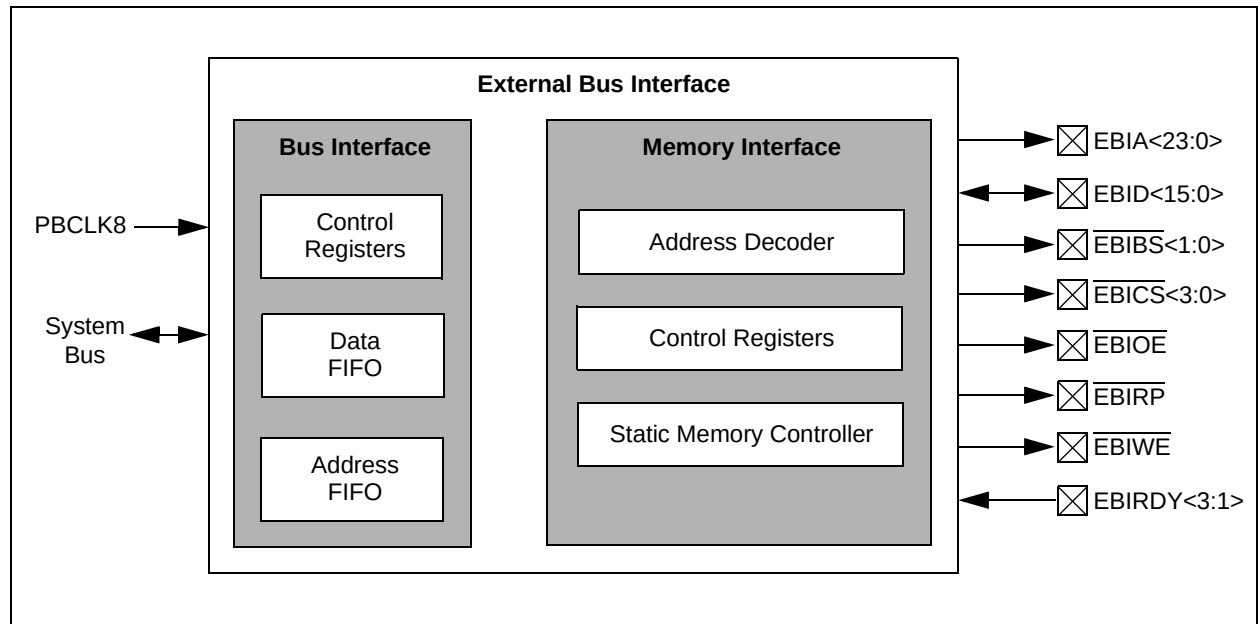
The features of the EBI module depend on the pin count of the PIC32MZ EC device, as shown in Table 24-1.

TABLE 24-1: EBI MODULE FEATURES

| Feature                   | Number of Device Pins |     |     |
|---------------------------|-----------------------|-----|-----|
|                           | 100                   | 124 | 144 |
| Async SRAM                | Y                     | Y   | Y   |
| Async NOR Flash           | Y                     | Y   | Y   |
| Available address lines   | 20                    | 20  | 24  |
| 8-bit data bus support    | Y                     | Y   | Y   |
| 16-bit data bus support   | Y                     | Y   | Y   |
| Available Chip Selects    | 1                     | 1   | 4   |
| Timing mode sets          | 3                     | 3   | 3   |
| 8-bit R/W from 16-bit bus | N                     | N   | Y   |
| Non-memory device         | Y                     | Y   | Y   |
| LCD                       | Y                     | Y   | Y   |

**Note:** Once the EBI module is configured, external devices will be memory mapped and can be access from KSEG2 memory space (see Figure 4-1 through Figure 4-4 in **Section 4.0 “Memory Organization”** for more information). The MMU must be enabled and the TLB must be set up to access this memory (see **Section 50. “CPU for Devices with MIPS32® microAptiv™ and M-Class Cores”** (DS60001192) in the *“PIC32 Family Reference Manual”* for more information).

FIGURE 24-1: EBI SYSTEM BLOCK DIAGRAM





# PIC32MZ Embedded Connectivity (EC) Family

## REGISTER 24-3: EBISMTx: EXTERNAL BUS INTERFACE STATIC MEMORY TIMING REGISTER ('x' = 0-2)

| Bit Range | Bit 31/23/15/7          | Bit 30/22/14/6           | Bit 29/21/13/5          | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2           | Bit 25/17/9/1           | Bit 24/16/8/0 |
|-----------|-------------------------|--------------------------|-------------------------|----------------|----------------|--------------------------|-------------------------|---------------|
| 31:24     | U-0                     | U-0                      | U-0                     | U-0            | U-0            | R/W-1                    | R/W-0                   | R/W-0         |
|           | —                       | —                        | —                       | —              | —              | RDYMODE                  | PAGESIZE<1:0>           |               |
| 23:16     | R/W-0                   | R/W-0                    | R/W-0                   | R/W-1          | R/W-1          | R/W-1                    | R/W-0                   | R/W-0         |
|           | PAGEMODE                | TPRC<3:0> <sup>(1)</sup> |                         |                |                | TBTA<2:0> <sup>(1)</sup> |                         |               |
| 15:8      | R/W-0                   | R/W-0                    | R/W-1                   | R/W-0          | R/W-1          | R/W-1                    | R/W-0                   | R/W-1         |
|           | TWP<5:0> <sup>(1)</sup> |                          |                         |                |                |                          | TWR<1:0> <sup>(1)</sup> |               |
| 7:0       | R/W-0                   | R/W-1                    | R/W-0                   | R/W-0          | R/W-1          | R/W-0                    | R/W-1                   | R/W-1         |
|           | TAS<1:0> <sup>(1)</sup> |                          | TRC<5:0> <sup>(1)</sup> |                |                |                          |                         |               |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **RDYMODE:** Data Ready Device Select bit

The device associated with register set 'x' is a data-ready device, and will use the EBIRDYx pin.

1 = EBIRDYx input is used

0 = EBIRDYx input is not used

bit 25-24 **PAGESIZE<1:0>:** Page Size for Page Mode Device bits

11 = 32-word page

10 = 16-word page

01 = 8-word page

00 = 4-word page

bit 23 **PAGEMODE:** Memory Device Page Mode Support bit

1 = Device supports Page mode

0 = Device does not support Page mode

bit 22-19 **TPRC<3:0>:** Page Mode Read Cycle Time bits<sup>(1)</sup>

Read cycle time is TPRC + 1 clock cycle.

bit 18-16 **TBTA<2:0>:** Data Bus Turnaround Time bits<sup>(1)</sup>

Clock cycles (0-7) for static memory between read-to-write, write-to-read, and read-to-read when Chip Select changes.

bit 15-10 **TWP<5:0>:** Write Pulse Width bits<sup>(1)</sup>

Write pulse width is TWP + 1 clock cycle.

bit 9-8 **TWR<1:0>:** Write Address/Data Hold Time bits<sup>(1)</sup>

Number of clock cycles to hold address or data on the bus.

bit 7-6 **TAS<1:0>:** Write Address Setup Time bits<sup>(1)</sup>

Clock cycles for address setup time. A value of '0' is only valid in the case of SSRAM.

bit 5-0 **TRC<5:0>:** Read Cycle Time bits<sup>(1)</sup>

Read cycle time is TRC + 1 clock cycle.

**Note 1:** Please refer to **Section 47. "External Bus Interface (EBI)"** (DS60001245) in the *"PIC32 Family Reference Manual"* for the EBI timing diagrams and additional information.

# PIC32MZ Embedded Connectivity (EC) Family

## REGISTER 30-27: EMAC1CLRT: ETHERNET CONTROLLER MAC COLLISION WINDOW/RETRY LIMIT REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | R/W-1          | R/W-1          | R/W-0          | R/W-1          | R/W-1         | R/W-1         |
|           | —              | —              | CWINDOW<5:0>   |                |                |                |               |               |
| 7:0       | U-0            | U-0            | U-0            | U-0            | R/W-1          | R/W-1          | R/W-1         | R/W-1         |
|           | —              | —              | —              | —              | RETX<3:0>      |                |               |               |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13-8 **CWINDOW<5:0>:** Collision Window bits

This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RETX<3:0>:** Retransmission Maximum bits

This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts (attemptLimit) to be 0xF (15d). Its default is '0xF'.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**TABLE 34-2: ADEVCFG: ALTERNATE DEVICE CONFIGURATION WORD SUMMARY**

| Virtual Address<br>(BFC0_#) | Register<br>Name | Bit Range | Bits         |               |         |          |         |       |                |              |         |               |         |              |             |               |            |            | All Resets |      |
|-----------------------------|------------------|-----------|--------------|---------------|---------|----------|---------|-------|----------------|--------------|---------|---------------|---------|--------------|-------------|---------------|------------|------------|------------|------|
|                             |                  |           | 31/15        | 30/14         | 29/13   | 28/12    | 27/11   | 26/10 | 25/9           | 24/8         | 23/7    | 22/6          | 21/5    | 20/4         | 19/3        | 18/2          | 17/1       | 16/0       |            |      |
| FF40                        | ADEVCFG3         | 31:16     | —            | FUSBIDIO      | IOL1WAY | PMDL1WAY | PGL1WAY | —     | FETHIO         | FMIEN        | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | USERID<15:0> |               |         |          |         |       |                |              |         |               |         |              |             |               |            |            | xxxx       |      |
| FF44                        | ADEVCFG2         | 31:16     | —            | UPLLFSEL      | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | FPLL0DIV<2:0> |            |            | xxxx       |      |
|                             |                  | 15:0      | —            | FPLLMULT<6:0> |         |          |         |       |                |              | FPLLICK | FPLL0RNG<2:0> |         |              | —           | FPLL0DIV<2:0> |            |            | xxxx       |      |
| FF48                        | ADEVCFG1         | 31:16     | FDMTEN       | DMTCNT<4:0>   |         |          |         |       | FWDTWINSZ<1:0> |              | FWDTEN  | WINDIS        | WDTSPGM | WDTPS<4:0>   |             |               |            |            |            | xxxx |
|                             |                  | 15:0      | FCKSM<1:0>   |               | —       | —        | —       | —     | OSCI0FNC       | POSCMOD<1:0> |         | IESO          | FSOSCEN | DMTINTV<2:0> |             |               | FNOSC<2:0> |            | xxxx       |      |
| FF4C                        | ADEVCFG0         | 31:16     | —            | EJTAGBEN      | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | DBGPER<2:0>   |         |          |         | —     | FSLEEP         | FECCCON<1:0> |         | —             | BOOTISA | TRCEN        | ICESEL<1:0> |               | JTAGEN     | DEBUG<1:0> |            | xxxx |
| FF50                        | ADEVCP3          | 31:16     | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
| FF54                        | ADEVCP2          | 31:16     | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
| FF58                        | ADEVCP1          | 31:16     | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
| FF5C                        | ADEVCP0          | 31:16     | —            | —             | —       | CP       | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
| FF60                        | ADEVSIGN3        | 31:16     | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
| FF64                        | ADEVSIGN2        | 31:16     | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
| FF68                        | ADEVSIGN1        | 31:16     | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
| FF6C                        | ADEVSIGN0        | 31:16     | 0            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |
|                             |                  | 15:0      | —            | —             | —       | —        | —       | —     | —              | —            | —       | —             | —       | —            | —           | —             | —          | —          | xxxx       |      |

**Legend:** x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

# PIC32MZ Embedded Connectivity (EC) Family

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## 36.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for  
Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICKit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,  
Evaluation Kits and Starter Kits
- Third-party development tools

## 36.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

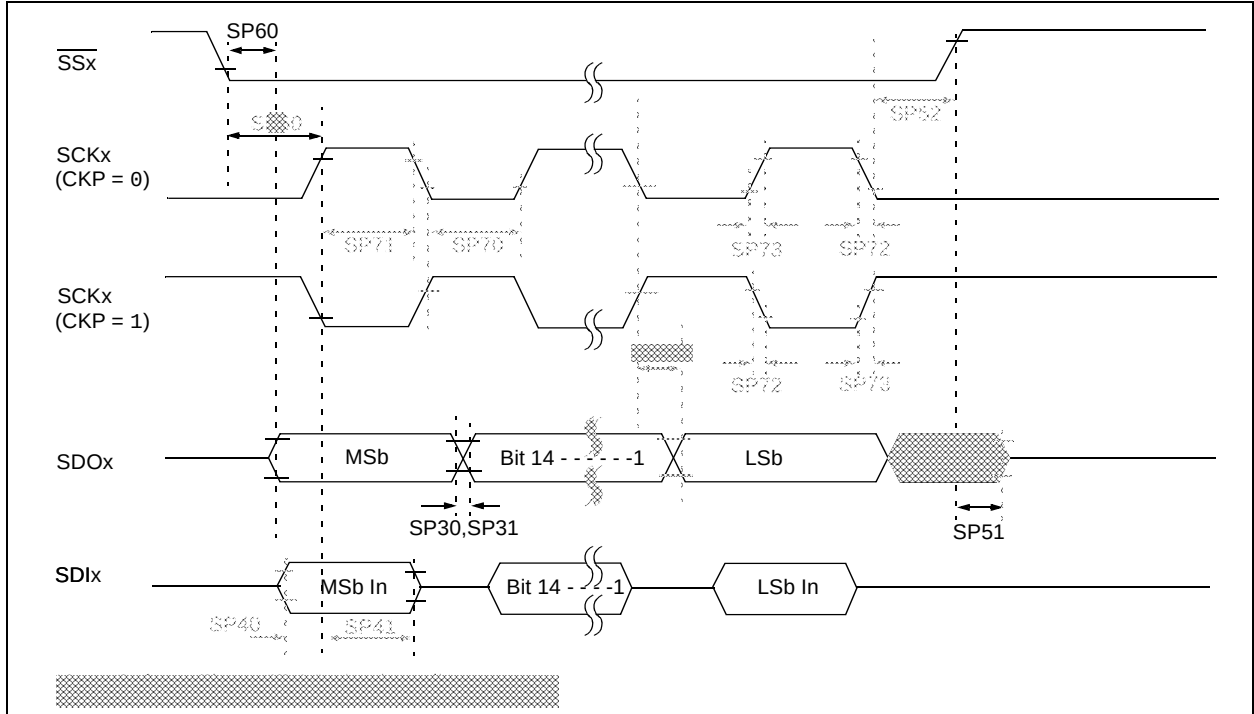
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

# PIC32MZ Embedded Connectivity (EC) Family

**FIGURE 37-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**



**TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS |                       |                                              | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial |                     |      |       |                    |
|--------------------|-----------------------|----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|-------|--------------------|
| Param. No.         | Symbol                | Characteristics <sup>(1)</sup>               | Min.                                                                                                                                | Typ. <sup>(2)</sup> | Max. | Units | Conditions         |
| SP70               | TscL                  | SCKx Input Low Time ( <b>Note 3</b> )        | Tsck/2                                                                                                                              | —                   | —    | ns    | —                  |
| SP71               | Tsch                  | SCKx Input High Time ( <b>Note 3</b> )       | Tsck/2                                                                                                                              | —                   | —    | ns    | —                  |
| SP72               | TscF                  | SCKx Input Fall Time                         | —                                                                                                                                   | —                   | 10   | ns    | —                  |
| SP73               | TscR                  | SCKx Input Rise Time                         | —                                                                                                                                   | —                   | 10   | ns    | —                  |
| SP30               | Tdof                  | SDOx Data Output Fall Time ( <b>Note 4</b> ) | —                                                                                                                                   | —                   | —    | ns    | See parameter DO32 |
| SP31               | Tdor                  | SDOx Data Output Rise Time ( <b>Note 4</b> ) | —                                                                                                                                   | —                   | —    | ns    | See parameter DO31 |
| SP35               | Tsch2doV,<br>TscL2doV | SDOx Data Output Valid after SCKx Edge       | —                                                                                                                                   | —                   | 10   | ns    | VDD > 2.7V         |
|                    |                       |                                              | —                                                                                                                                   | —                   | 15   | ns    | VDD < 2.7V         |
| SP40               | TdiV2sch,<br>TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge   | 0                                                                                                                                   | —                   | —    | ns    | —                  |
| SP41               | Tsch2diL,<br>TscL2diL | Hold Time of SDIx Data Input to SCKx Edge    | 7                                                                                                                                   | —                   | —    | ns    | —                  |
| SP50               | Tssl2sch,<br>Tssl2scL | SSx ↓ to SCKx ↓ or SCKx ↑ Input              | 88                                                                                                                                  | —                   | —    | ns    | —                  |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 20 ns.

**4:** Assumes 10 pF load on all SPIx pins.