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Details

Product Status	Obsolete
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	98
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ech124-i-tl

PIC32MZ Embedded Connectivity (EC) Family

TABLE 3-3: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0	Index	Index into the TLB array (microAptiv MPU only).
1	Random	Randomly generated index into the TLB array (microAptiv MPU only).
2	EntryLo0	Low-order portion of the TLB entry for even-numbered virtual pages (microAptiv MPU only).
3	EntryLo1	Low-order portion of the TLB entry for odd-numbered virtual pages (microAptiv MPU only).
4	Context/ UserLocal	Pointer to the page table entry in memory (microAptiv MPU only). User information that can be written by privileged software and read via the RDHWR instruction.
5	PageMask/ PageGrain	PageMask controls the variable page sizes in TLB entries. PageGrain enables support of 1 KB pages in the TLB (microAptiv MPU only).
6	Wired	Controls the number of fixed (i.e., wired) TLB entries (microAptiv MPU only).
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-privileged mode.
8	BadVAddr	Reports the address for the most recent address-related exception.
9	Count	Processor cycle count.
10	EntryHi	High-order portion of the TLB entry (microAptiv MPU only).
11	Compare	Core timer interrupt control.
12	Status	Processor status and control.
	IntCtl	Interrupt control of vector spacing.
	SRSCtl	Shadow register set control.
	SRSMap	Shadow register mapping control.
	View_IPL	Allows the Priority Level to be read/written without extracting or inserting that bit from/to the Status register.
	SRSMap2	Contains two 4-bit fields that provide the mapping from a vector number to the shadow set number to use when servicing such an interrupt.
13	Cause	Describes the cause of the last exception.
	NestedExc	Contains the error and exception level status bit values that existed prior to the current exception.
	View_RIPL	Enables read access to the RIPL bit that is available in the Cause register.
14	EPC	Program counter at last exception.
	NestedEPC	Contains the exception program counter that existed prior to the current exception.
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	LLAddr	Load link address (microAptiv MPU only).
18	WatchLo	Low-order watchpoint address (microAptiv MPU only).
19	WatchHi	High-order watchpoint address (microAptiv MPU only).
20-22	Reserved	Reserved in the PIC32 core.

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The System Bus arbitration scheme implements a non-programmable, Least Recently Served (LRS) priority, which provides Quality Of Service (QOS) for most initiators. However, some initiators can use Fixed High Priority (HIGH) arbitration to guarantee their access to data.

The arbitration scheme for the available initiators is shown in Table 4-5.

TABLE 4-5: INITIATOR ID AND QOS

Name	ID	QOS
CPU	1	LRS ⁽¹⁾
CPU	2	HIGH ^(1,2)
DMA Read	3	LRS ⁽¹⁾
DMA Read	4	HIGH ^(1,2)
DMA Write	5	LRS ⁽¹⁾
DMA Write	6	HIGH ^(1,2)
USB	7	LRS
Ethernet Read	8	LRS
Ethernet Write	9	LRS
CAN1	10	LRS
CAN2	11	LRS
SQI1	12	LRS
Flash Controller	13	HIGH ⁽²⁾
Crypto	14	LRS

Note 1: When accessing SRAM, the DMAPRI bit (CFGCON<25>) and the CPUPRI bit (CFGCON<24>) provide arbitration control for the DMA and CPU (when servicing an interrupt (i.e., EXL = 1)), respectively, by selecting the use of LRS or HIGH. When using HIGH, the DMA and CPU get arbitration preference over all initiators using LRS.

- 2:** Using HIGH arbitration can have serious negative effects on other initiators. Therefore, it is recommended to not enable this type of arbitration for an initiator that uses significant system bandwidth. HIGH arbitration is intended to be used for low bandwidth applications that require low latency, such as LCC graphics applications.

4.3 Permission Access and System Bus Registers

The System Bus on PIC32MZ EC family of microcontrollers provides access control capabilities for the transaction initiators on the System Bus.

The System Bus divides the entire memory space into fourteen target regions and permits access to each target by initiators via permission groups. Four Permission Groups (0 through 3) can be assigned to each initiator. Each permission group is independent of the others and can have exclusive or shared access to a region.

Using the CFGPG register (see Register 34-10 in **Section 34.0 “Special Features”**), Boot firmware can assign a permission group to each initiator, which can make requests on the System Bus.

The available targets and their regions, as well as the associated control registers to assign protection, are described and listed in Table 4-6.

Register 4-2 through Register 4-10 are used for setting and controlling access permission groups and regions.

To change these registers, they must be unlocked in hardware. The register lock is controlled by the PGLOCK Configuration bit (CFGCON<11>). Setting PGLOCK prevents writes to the control registers; clearing PGLOCK allows writes.

To set or clear the PGLOCK bit, an unlock sequence must be executed. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the “PIC32 Family Reference Manual” for details.

6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1240	RCON	31:16	—	—	—	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	—	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR	0000
1250	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
1260	RNMICON	31:16	—	—	—	—	—	—	DMTO	WDTO	SWNMI	—	—	—	—	—	CF	WDTS	0000
		15:0	—	—	—	—	—	—	—	—	NMICNT<7:0>								0000
1270	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VREGS	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81 #)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05A4	OFF025	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05A8	OFF026	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05AC	OFF027	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05B0	OFF028	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05B4	OFF029	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05B8	OFF030	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05BC	OFF031	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05C0	OFF032	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05C4	OFF033	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05C8	OFF034	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05CC	OFF035	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05D0	OFF036	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05D4	OFF037	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05D8	OFF038	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
05DC	OFF039	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
 - 2: This bit or register is not available on 64-pin devices.
 - 3: This bit or register is not available on devices without a CAN module.
 - 4: This bit or register is not available on 100-pin devices.
 - 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
 - 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
 - 7: This bit or register is not available on devices without a Crypto module.
 - 8: This bit or register is not available on 124-pin devices.

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REGISTER 9-2: PRESTAT: PREFETCH MODULE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
	—	—	—	—	PFMDDED	PFMSEC	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PFMSECCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

HS = Hardware Set

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **PFMDDED:** Flash Double-bit Error Detected (DED) Status bit

This bit is set in hardware and can only be cleared (i.e., set to '0') in software.

1 = A DED error has occurred

0 = A DED error has not occurred

bit 26 **PFMSEC:** Flash Single-bit Error Corrected (SEC) Status bit

1 = A SEC error occurred when PFMSECCNT<7:0> was equal to '0'

0 = A SEC error has not occurred

bit 25-8 **Unimplemented:** Read as '0'

bit 7-0 **PFMSECCNT<7:0>:** Flash SEC Count bits

11111111 - 00000000 = SEC count

This field decrements by one each time an SEC error occurs. It will hold at zero on the two-hundred and fifty-sixth error. When an SEC error occurs, when PFMSECCNT = 0, the PFMSEC status bit is set. If PFMSECEN is also set, an interrupt is generated.

Note: These bits count all SEC errors and are not limited to SEC errors on unique addresses.

PIC32MZ Embedded Connectivity (EC) Family

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Direct Memory Access (DMA) Controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the device such as SPI, UART, PMP, etc., or memory itself.

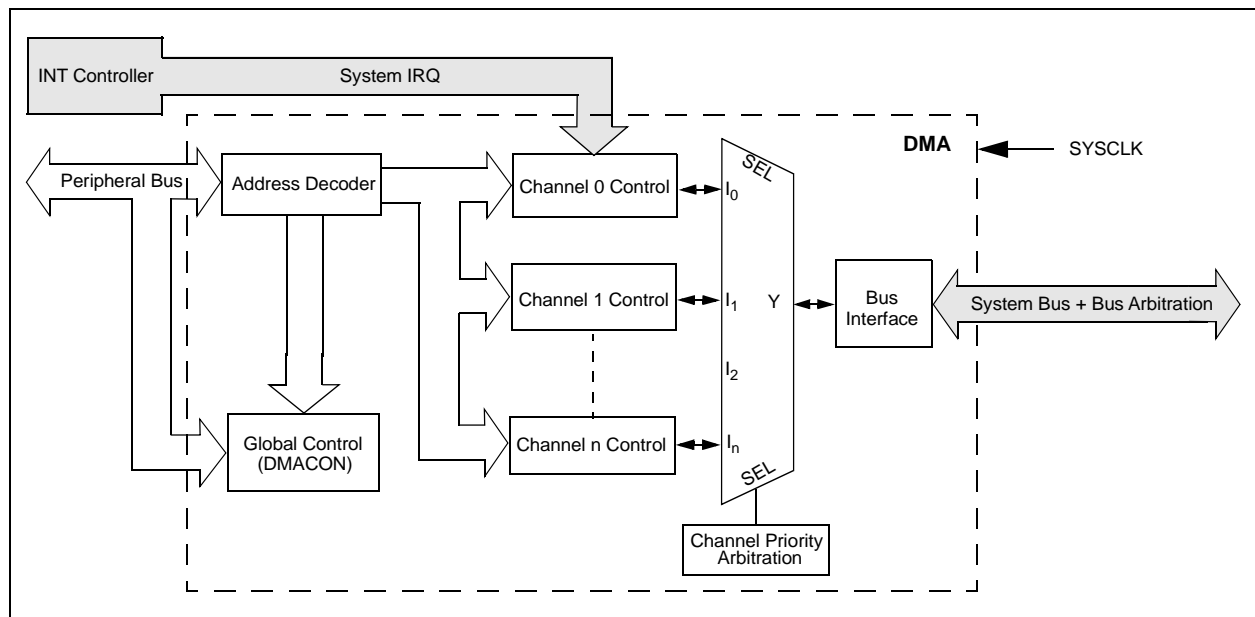
Note: To avoid cache coherency problems on devices with L1 cache, DMA buffers must only be allocated or accessed from the KSEG1 segment.

Following are some of the key features of the DMA Controller module:

- Eight identical channels, each featuring:
 - Auto-increment source and destination address registers
 - Source and destination pointers
 - Memory to memory and memory to peripheral transfers

- Automatic word-size detection:
 - Transfer granularity, down to byte level
 - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- Flexible DMA requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Up to 2-byte Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA debug support features:
 - Most recent error address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- CRC Generation module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



PIC32MZ Embedded Connectivity (EC) Family

REGISTER 10-8: DCHxECON: DMA CHANNEL x EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0> ⁽¹⁾							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0> ⁽¹⁾							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits⁽¹⁾

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•
•
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits⁽¹⁾

11111111 = Interrupt 255 will initiate a DMA transfer

•
•
•

00000001 = Interrupt 1 will initiate a DMA transfer

00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See Table 7-2: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

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REGISTER 22-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 7-6 **URXISEL<1:0>**: Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least one data character)
- bit 5 **ADDEN**: Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE**: Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received
- bit 3 **PERR**: Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected
- bit 2 **FERR**: Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected
- bit 1 **OERR**: Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed
- bit 0 **URXDA**: Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

PIC32MZ Embedded Connectivity (EC) Family

25.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

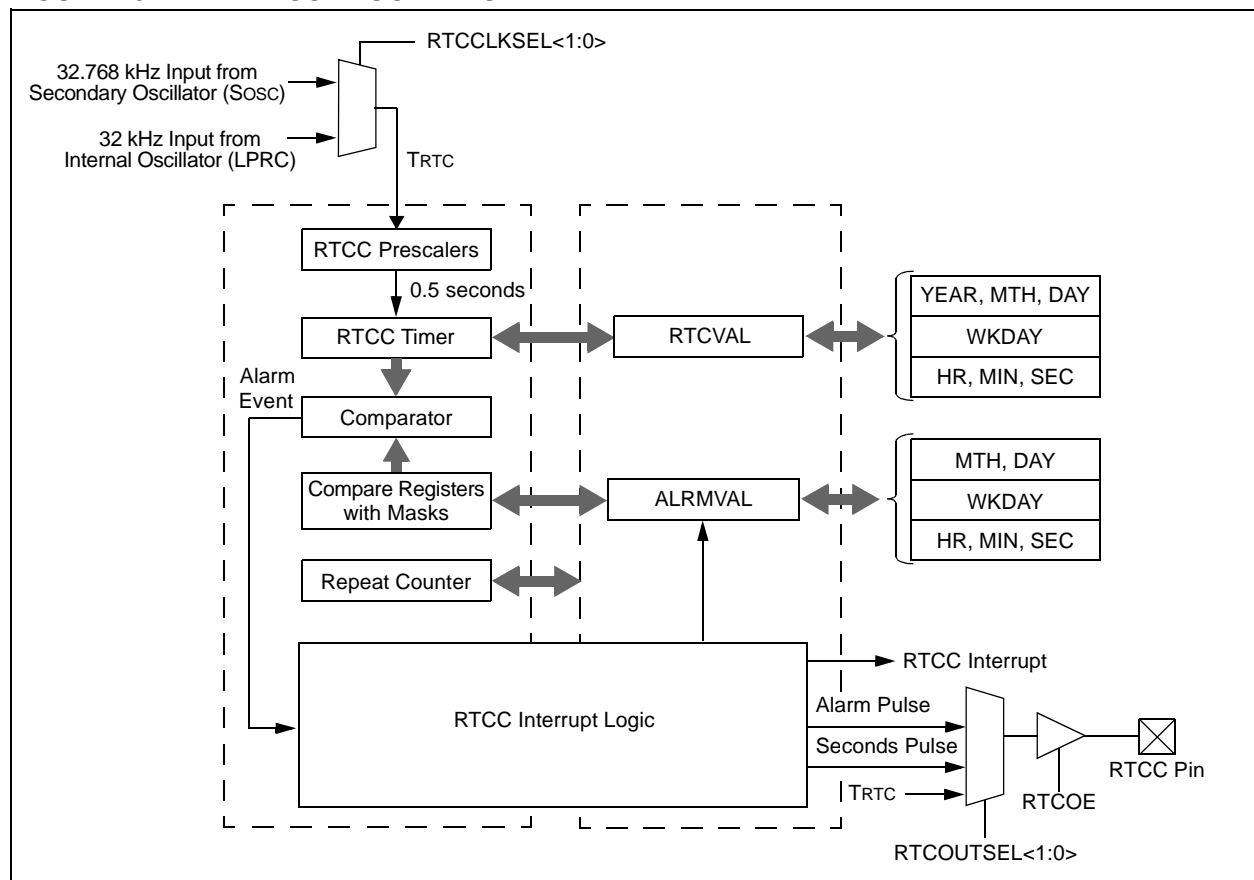
Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are key features of the RTCC module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ± 0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

FIGURE 25-1: RTCC BLOCK DIAGRAM



PIC32MZ Embedded Connectivity (EC) Family

REGISTER 30-3: ETHTXST: ETHERNET CONTROLLER TX PACKET DESCRIPTOR START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXSTADDR<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXSTADDR<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXSTADDR<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
TXSTADDR<7:2>							—	—

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-2 **TXSTADDR<31:2>**: Starting Address of First Transmit Descriptor bits

This register should not be written while any transmit, receive or DMA operations are in progress.

This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented**: Read as '0'

Note 1: This register is only used for TX operations.

2: This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

REGISTER 30-4: ETHRXST: ETHERNET CONTROLLER RX PACKET DESCRIPTOR START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RXSTADDR<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RXSTADDR<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RXSTADDR<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
RXSTADDR<7:2>							—	—

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-2 **RXSTADDR<31:2>**: Starting Address of First Receive Descriptor bits

This register should not be written while any transmit, receive or DMA operations are in progress.

This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented**: Read as '0'

Note 1: This register is only used for RX operations.

2: This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

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REGISTER 30-16: ETHRXOVFLOW: ETHERNET CONTROLLER RECEIVE OVERFLOW STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVFLWCNT<15:0>:** Dropped Receive Frames Count bits

Increment counter for frames accepted by the RX filter and subsequently dropped due to internal receive error (RXFIFO overrun). This event also sets the RXOVFLW bit (ETHIRQ<0>) interrupt flag.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

31.1 Comparator Control Registers

TABLE 31-1: COMPARATOR REGISTER MAP

Virtual Address (BF84_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>	—	—	CREF	—	—	CCH<1:0>	—	00C3
C010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>	—	—	CREF	—	—	CCH<1:0>	—	00C3
C060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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REGISTER 32-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	CVROE	CVRR	CVRSS	CVR<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit

1 = Module is enabled

Setting this bit does not affect other bits in the register.

0 = Module is disabled and does not consume current.

Clearing this bit does not affect the other bits in the register.

bit 14-7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** CVREFOUT Enable bit

1 = Voltage level is output on CVREFOUT pin

0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit

1 = 0 to 0.625 CVRSRC, with CVRSRC/24 step size

0 = 0.25 CVRSRC to 0.719 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit

1 = Comparator voltage reference source, $CVRSRC = (VREF+) - (VREF-)$

0 = Comparator voltage reference source, $CVRSRC = AVDD - AVSS$

bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \leq CVR<3:0> \leq 15$ bits

When CVRR = 1:

$CVREF = (CVR<3:0>/24) \cdot (CVRSRC)$

When CVRR = 0:

$CVREF = 1/4 \cdot (CVRSRC) + (CVR<3:0>/32) \cdot (CVRSRC)$

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REGISTER 34-13: DEVSNx: DEVICE SERIAL NUMBER REGISTER 'x' ('x' = 0, 1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	SN<31:24>							
23:16	R	R	R	R	R	R	R	R
	SN<23:16>							
15:8	R	R	R	R	R	R	R	R
	SN<15:8>							
7:0	R	R	R	R	R	R	R	R
	SN<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **SN<31:0>**: Device Unique Serial Number bits

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-10: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

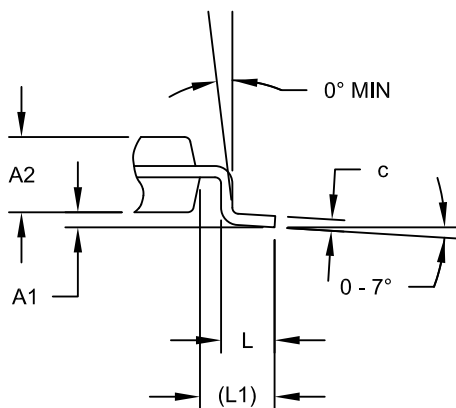
DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DI60a	I _{ICL}	Input Low Injection Current	0	—	-5 ^(2,5)	mA	This parameter applies to all pins, with the exception of RB10. Maximum I _{ICH} current for this exception is 0 mA.
DI60b	I _{ICH}	Input High Injection Current	0	—	+5 ^(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, OSC1, OSC2, SOSC1, SOSCO, D+, D-, and RB10. Maximum I _{ICH} current for these exceptions is 0 mA.
DI60c	ΣI _{ICT}	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁶⁾	—	+20 ⁽⁶⁾	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (I _{ICL} + I _{ICH}) ≤ ΣI _{ICT}

- Note 1:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** V_{IL} source < (V_{SS} - 0.3). Characterized but not tested.
- 3:** V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- 4:** Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- 5:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., V_{IH} Source > (V_{DD} + 0.3) or V_{IL} source < (V_{SS} - 0.3)).
- 6:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, I_{ICL} = (((V_{SS} - 0.3) - V_{IL} source) / R_S). If **Note 3**, I_{ICH} = ((I_{ICH} source - (V_{DD} + 0.3)) / R_S). R_S = Resistance between input source voltage and device pin. If (V_{SS} - 0.3) ≤ V_{SOURCE} ≤ (V_{DD} + 0.3), injection current = 0.

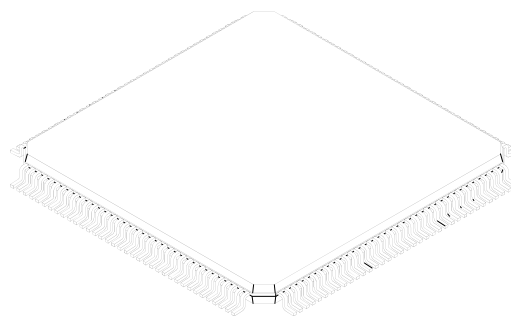
PIC32MZ Embedded Connectivity (EC) Family

144-Lead Plastic Thin Quad Flatpack (PH) - 16x16x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



DETAIL A



Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	144		
Lead Pitch	e	0.40 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Overall Width	D	18.00 BSC		
Overall Length	E	18.00 BSC		
Molded Body Width	D1	16.00 BSC		
Molded Body Length	E1	16.00 BSC		
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.13	-	0.23

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-155B Sheet 2 of 2

PIC32MZ Embedded Connectivity (EC) Family

A.7 Interrupts and Exceptions

The key difference between Interrupt Controllers in PIC32MX5XX/6XX/7XX devices and PIC32MZ devices concerns vector spacing. Previous PIC32MX devices had fixed vector spacing, which is adjustable in set increments, and every interrupt had the same amount of space. PIC32MZ devices replace this with a variable offset spacing, where each interrupt has an offset register to determine where to begin execution.

In addition, the IFSx, IECx, and IPCx registers for old peripherals have shifted to different registers due to new peripherals. Please refer to **Section 7.0 “CPU Exceptions and Interrupt Controller”** to determine where the interrupts are now located.

Table A-8 lists differences (indicated by **Bold** type) in the registers that will affect software migration.

TABLE A-8: INTERRUPT DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
Vector Spacing	
On PIC32MX devices, the vector spacing was determined by the VS field in the CPU core.	On PIC32MZ devices, the vector spacing is variable and determined by the Interrupt controller. The VOFFx<17:1> bits in the OFFx register are set to the offset from EBASE where the interrupt service routine is located.
VS<4:0> (IntCtl<9:5>: CP0 Register 12, Select 1) 10000 = 512-byte vector spacing 01000 = 256-byte vector spacing 00100 = 128-byte vector spacing 00010 = 64-byte vector spacing 00001 = 32-byte vector spacing 00000 = 0-byte vector spacing	VOFFx<17:1> (OFFx<17:1>) Interrupt Vector ‘x’ Address Offset bits
Shadow Register Sets	
On PIC32MX devices, there was one shadow register set which could be used during interrupt processing. Which interrupt priority could use the shadow register set was determined by the FSRSEL field in DEVCFG3 and SS0 on INTCON.	On PIC32MZ devices, there are seven shadow register sets, and each priority level can be assigned a shadow register set to use via the PRISSEL<3:0> bits in the PRIS register. The SS0 bit is also moved to PRIS<0>.
FSRSEL<2:0> (DEVCFG3<18:16>) 111 = Assign Interrupt Priority 7 to a shadow register set 110 = Assign Interrupt Priority 6 to a shadow register set • • • 001 = Assign Interrupt Priority 1 to a shadow register set 000 = All interrupt priorities are assigned to a shadow register set	PRISSEL<3:0> PRIS<y:z> 1xxx = Reserved (by default, an interrupt with a priority level of x uses Shadow Set 0) 0111 = Interrupt with a priority level of x uses Shadow Set 7 0110 = Interrupt with a priority level of x uses Shadow Set 6 • • • 0001 = Interrupt with a priority level of x uses Shadow Set 1 0000 = Interrupt with a priority level of x uses Shadow Set 0
SS0 (INTCON<16>) 1 = Single vector is presented with a shadow register set 0 = Single vector is not presented with a shadow register set	SS0 (PRIS<0>) 1 = Single vector is presented with a shadow register set 0 = Single vector is not presented with a shadow register set
Status	
PIC32MX devices, the VEC<5:0> bits show which interrupt is being serviced.	On PIC32MZ devices, the SIRQ<7:0> bits show the IRQ number of the interrupt last serviced.
VEC<5:0> (INTSTAT<5:0>) 11111-00000 = The interrupt vector that is presented to the CPU	SIRQ<7:0> (INTSTAT<7:0>) 11111111-00000000 = The last interrupt request number serviced by the CPU

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TABLE A-9: FLASH PROGRAMMING DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
Flash Programming	
<p>NVMOP<3:0> (NVMCON<3:0>)</p> <p>1111 = Reserved</p> <p>•</p> <p>•</p> <p>•</p> <p>0111 = Reserved</p> <p>0110 = No operation</p> <p>0101 = Program Flash (PFM) erase operation</p> <p>0100 = Page erase operation</p> <p>0011 = Row program operation</p> <p>0010 = No operation</p> <p>0001 = Word program operation</p> <p>0000 = No operation</p>	<p>The op codes for programming the Flash memory have been changed to accommodate the new quad-word programming and dual-panel features. The row size has changed to 2 KB (512 IW) from 128 IW. The page size has changed to 16 KB (4K IW) from 4 KB (1K IW). Note that the NVMOP register is now protected, and requires the WREN bit be set to enable modification.</p> <p>NVMOP<3:0> (NVMCON<3:0>)</p> <p>1111 = Reserved</p> <p>•</p> <p>•</p> <p>•</p> <p>1000 = Reserved</p> <p>0111 = Program erase operation</p> <p>0110 = Upper program Flash memory erase operation</p> <p>0101 = Lower program Flash memory erase operation</p> <p>0100 = Page erase operation</p> <p>0011 = Row program operation</p> <p>0010 = Quad Word (128-bit) program operation</p> <p>0001 = Word program operation</p> <p>0000 = No operation</p>
PIC32MX devices feature a single NVMDATA register for word programming.	On PIC32MZ devices, to support quad word programming, the NVMDATA register has been expanded to four words.
NVMDATA	NVMDATAx, where 'x' = 0 through 3
Flash Endurance and Retention	
PIC32MX devices support Flash endurance and retention of up to 20K E/W cycles and 20 years.	On PIC32MZ devices, ECC must be enabled to support the same endurance and retention as PIC32MX devices.
Configuration Words	
On PIC32MX devices, Configuration Words can be programmed with Word or Row program operation.	On PIC32MZ devices, all Configuration Words must be programmed with Quad Word operation.
Configuration Words Reserved Bit	
On PIC32MX devices, the DEVCFG0<15> bit is Reserved and must be programmed to '0'.	On PIC32MZ devices, this bit is DEVSIGN0<31> .

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APPENDIX B: REVISION HISTORY

Revision A (February 2013)

This is the initial released version of the document.

Revision B (November 2013)

Throughout the document, references to Microchip documentation numbers have been updated to reflect a new 8-digit numbering scheme now in use by Microchip. For example, DS61191 is now DS60001191.

The revision includes the following major changes, which are referenced by their respective chapter in Table B-1.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE B-1: MAJOR SECTION UPDATES

Section Name	Update Description
“32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog”	All Family Feature tables were updated (see Table 1 and Table 2). The device part numbers were updated in all pin tables (see Table 3 through Table 6).
1.0 “Device Overview”	Updated the Pinout I/O Descriptions for 64-pin QFN/TQFP devices for SPI5 and SPI6 (see Table 1-9).
2.0 “Guidelines for Getting Started with 32-bit Microcontrollers”	Updated the $\overline{\text{MCLR}}$ Pin Connections example (see Figure 2-2). Removed the Termination Resistor diagram (formerly Figure 2-4).
4.0 “Memory Organization”	Updated the Boot and Alias Memory Map (see Figure 4-5). Updated the Boot Flash 1 and Boot Flash 2 Sequence and Configuration Words Summaries (see Table 4-2 and Table 4-3, respectively). Added the Watchdog Timer (WDT) to Target 5 in the Initiators to Targets Access Association and System Bus Targets and Associated Protection Registers (see Table 4-4 and Table 4-6, respectively). In addition, the reset values in Note 1 of Table 4-6 were updated. The CODE<3:0> bit value definitions and the default POR values for the CMD<2:0> bits were updated (see Register 4-3). The default POR value for the GROUP3 bit was updated (see Register 4-9 and Register 4-10).
5.0 “Flash Program Memory”	The All Resets value for the lower 16 bits of the NVMBWP register was updated (see Table 5-1).
6.0 “Resets”	The Brown-out Reset block was removed from the Configuration Mismatch Reset (CMR) in the System Reset Block Diagram (see Figure 6-1). Removed the EXT bit from RNMICON register in the Resets Register Map (see Table 6-1).
7.0 “CPU Exceptions and Interrupt Controller”	Note 2 and Note 3 were added to Interrupt IRQ, Vector and Bit Location (see Table 7-2). Notes 4, 5, and 6 were added to the Interrupt Register Map (see Table 7-3).
9.0 “Prefetch Module”	Updated the bit value definitions for the PFMWS<2:0> bits (see Register 9-1).
10.0 “Direct Memory Access (DMA) Controller”	The CHPDAT bits were updated to <15:0> in the DCHxDAT registers (see Table 10-3).
20.0 “Serial Quad Interface (SQI)”	The SQI1CMDTHR, SQI1INTTHR, SQI1BDTXDSTAT, and SQI1BDRXDSTAT registers were updated (see Table 20-1, Register 20-6, Register 20-7, Register 20-19, and Register 20-20).

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Revision C (July 2014)

The following global updates were incorporated throughout the data sheet:

- All instances of OSCI and OSCO in the pin tables were changed to: OSC1 and OSC2, respectively
- V-Temp Operating Conditions: 180 MHz, $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ were added
- Operating Conditions voltage range was changed to 2.3V to 3.6V

In addition, the following major updates were made, which are referenced by their respective chapter in Table B-3:

TABLE B-3: MAJOR SECTION UPDATES

Section Name	Update Description
26.0 “Crypto Engine”	Updated the Crypto Engine Buffer Descriptors (see Table 26-3). Updated the Security Association Control Word Structure (see Figure 26-10).
28.0 “Pipelined Analog-to-Digital Converter (ADC)”	Added 28.1 “ADC Configuration Requirements” .
37.0 “Electrical Characteristics”	Updated the DC Temperature and Voltage Specifications (see Table 37-4). Updated parameter DC20 and DC21 in the Operating Current Specifications (see Table 37-6). Updated parameter DC30a and DC31a in the Idle Current Specifications (see Table 37-7). Updated the Power-Down Current Specifications (see Table 37-8). Updated the I/O Pin Input Specifications (see Table 37-9). Updated the System Timing Requirements (see Table 37-17). Updated the Internal FRC Accuracy Specifications (see Table 37-19). Updated the Internal LPRC Accuracy Specifications (see Table 37-20). Updated the Internal BFRC Accuracy Specifications (see Table 37-21). Updated the SQI Timing Requirements (see Table 37-33). Updated the ADC1 Module Specifications (see Table 37-37). Updated the Analog-to-Digital Conversion Timing Requirements (see Table 37-38). Updated the USB OTG Specification: USB322 (see Table 37-43).