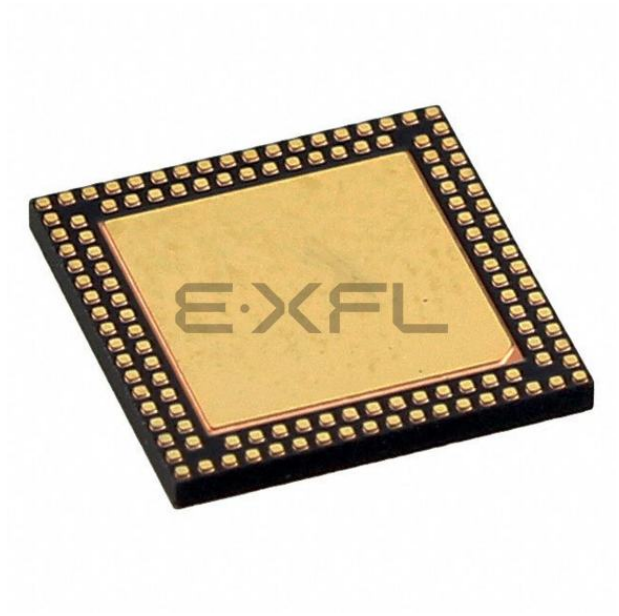

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	98
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ech124t-i-tl

TABLE 3-3: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0	Index	Index into the TLB array (microAptiv MPU only).
1	Random	Randomly generated index into the TLB array (microAptiv MPU only).
2	EntryLo0	Low-order portion of the TLB entry for even-numbered virtual pages (microAptiv MPU only).
3	EntryLo1	Low-order portion of the TLB entry for odd-numbered virtual pages (microAptiv MPU only).
4	Context/ UserLocal	Pointer to the page table entry in memory (microAptiv MPU only). User information that can be written by privileged software and read via the RDHWR instruction.
5	PageMask/ PageGrain	PageMask controls the variable page sizes in TLB entries. PageGrain enables support of 1 KB pages in the TLB (microAptiv MPU only).
6	Wired	Controls the number of fixed (i.e., wired) TLB entries (microAptiv MPU only).
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-privileged mode.
8	BadVAddr	Reports the address for the most recent address-related exception.
9	Count	Processor cycle count.
10	EntryHi	High-order portion of the TLB entry (microAptiv MPU only).
11	Compare	Core timer interrupt control.
12	Status	Processor status and control.
	IntCtl	Interrupt control of vector spacing.
	SRSCtl	Shadow register set control.
	SRSMap	Shadow register mapping control.
	View_IPL	Allows the Priority Level to be read/written without extracting or inserting that bit from/to the Status register.
	SRSMAP2	Contains two 4-bit fields that provide the mapping from a vector number to the shadow set number to use when servicing such an interrupt.
13	Cause	Describes the cause of the last exception.
	NestedExc	Contains the error and exception level status bit values that existed prior to the current exception.
	View_RIPL	Enables read access to the RIPL bit that is available in the Cause register.
14	EPC	Program counter at last exception.
	NestedEPC	Contains the exception program counter that existed prior to the current exception.
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	LLAddr	Load link address (microAptiv MPU only).
18	WatchLo	Low-order watchpoint address (microAptiv MPU only).
19	WatchHi	High-order watchpoint address (microAptiv MPU only).
20-22	Reserved	Reserved in the PIC32 core.

REGISTER 4-9: SBTxRDy: SYSTEM BUS TARGET 'x' REGION 'y' READ PERMISSIONS REGISTER ('x' = 0-13; 'y' = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **Group3:** Group3 Read Permissions bits
- 1 = Privilege Group 3 has read permission
- 0 = Privilege Group 3 does not have read permission

bit 2 **Group2:** Group2 Read Permissions bits
- 1 = Privilege Group 2 has read permission
- 0 = Privilege Group 2 does not have read permission

bit 1 **Group1:** Group1 Read Permissions bits
- 1 = Privilege Group 1 has read permission
- 0 = Privilege Group 1 does not have read permission

bit 0 **Group0:** Group0 Read Permissions bits
- 1 = Privilege Group 0 has read permission
- 0 = Privilege Group 0 does not have read permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MZ EC devices contain an internal Flash program memory for executing user code, which includes the following features:

- Two Flash banks for live update support
- Dual boot support
- Write protection for program and boot Flash
- ECC support

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip website.

Note: In PIC32MZ EC devices, the Flash page size is 16 KB (4096 IW) and the row size is 2 KB (512 IW).

REGISTER 6-4: PWRCON: POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	VREGS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **VREGS:** Voltage Regulator Stand-by Enable bit
1 = Voltage regulator will remain active during Sleep
0 = Voltage regulator will go to Stand-by mode during Sleep

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
12A0	DCH3CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
12B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
12C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
12D0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
12E0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
12F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1360	DCH4CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1370	DCH4ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1380	DCH4INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 11-2: USBCSR1: USB CONTROL STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	U-0
	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-17 **EP7TXIE:EP1TXIE:** Endpoint 'n' Transmit Interrupt Enable bits
1 = Endpoint Transmit interrupt events are enabled
0 = Endpoint Transmit interrupt events are not enabled

bit 16 **EP0IE:** Endpoint 0 Interrupt Enable bit
1 = Endpoint 0 interrupt events are enabled
0 = Endpoint 0 interrupt events are not enabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7-1 **EP7RXIF:EP1RXIF:** Endpoint 'n' RX Interrupt bit
1 = Endpoint has a receive event to be serviced
0 = No interrupt event

bit 0 **Unimplemented:** Read as '0'

REGISTER 11-16: USBINFO: USB INFORMATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	VPLEN<7:0>							
23:16	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	WTCON<3:0>				WTID<3:0>			
15:8	R-1	R-0	R-0	R-0	R-1	R-1	R-0	R-0
	DMACHANS<3:0>				RAMBITS<3:0>			
7:0	R-0	R-1	R-1	R-1	R-0	R-1	R-1	R-1
	RXENDPTS<3:0>				TXENDPTS<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **VPLEN<7:0>:** VBUS pulsing charge length bits

Sets the duration of the VBUS pulsing charge in units of 546.1 µs. (The default setting corresponds to 32.77 ms.)

bit 23-20 **WTCON<3:0>:** Connect/Disconnect filter control bits

Sets the wait to be applied to allow for the connect/disconnect filter in units of 533.3 ns. The default setting corresponds to 2.667 µs.

bit 19-6 **WTID<3:0>:** ID delay valid control bits

Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. The default setting corresponds to 52.43ms.

bit 15-12 **DMACHANS<3:0>:** DMA Channels bits

These read-only bits provide the number of DMA channels in the USB module. For the PIC32MZ EC family, this number is 8.

bit 11-8 **RAMBITS<3:0>:** RAM address bus width bits

These read-only bits provide the width of the RAM address bus. For the PIC32MZ EC family, this number is 12.

bit 7-4 **RXENDPTS<3:0>:** Included RX Endpoints bits

This read-only register gives the number of RX endpoints in the design. For the PIC32MZ EC family, this number is 7.

bit 3-0 **TXENDPTS<3:0>:** Included TX Endpoints bits

These read-only bits provide the number of TX endpoints in the design. For the PIC32MZ EC family, this number is 7.

TABLE 12-19: PORTJ REGISTER MAP FOR 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	ANSELJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ANSJ11	—	ANSJ9	ANSJ8	—	—	—	—	—	—	—	—	0B00
0810	TRISJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISJ15	TRISJ14	TRISJ13	TRISJ12	TRISJ11	TRISJ10	TRISJ9	TRISJ8	TRISJ7	TRISJ6	TRISJ5	TRISJ4	TRISJ3	TRISJ2	TRISJ1	TRISJ0	FFFF
0820	PORTJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RJ15	RJ14	RJ13	RJ12	RJ11	RJ10	RJ9	RJ8	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	xxxx
0830	LATJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATJ15	LATJ14	LATJ13	LATJ12	LATJ11	LATJ10	LATJ9	LATJ8	LATJ7	LATJ6	LATJ5	LATJ4	LATJ3	LATJ2	LATJ1	LATJ0	xxxx
0840	ODCJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCJ15	ODCJ14	ODCJ13	ODCJ12	ODCJ11	ODCJ10	ODCJ9	ODCJ18	ODCJ7	ODCJ6	ODCJ5	ODCJ4	ODCJ3	ODCJ2	ODCJ1	ODCJ0	0000
0850	CNPUJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUJ15	CNPUJ14	CNPUJ13	CNPUJ12	CNPUJ11	CNPUJ10	CNPUJ9	CNPUJ8	CNPUJ7	CNPUJ6	CNPUJ5	CNPUJ4	CNPUJ3	CNPUJ2	CNPUJ1	CNPUJ0	0000
0860	CNPDJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDJ15	CNPDJ14	CNPDJ13	CNPDJ12	CNPDJ11	CNPDJ10	CNPDJ9	CNPDJ8	CNPDJ7	CNPDJ6	CNPDJ5	CNPDJ4	CNPDJ3	CNPDJ2	CNPDJ1	CNPDJ0	0000
0870	CNCONJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0880	CNENJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEJ15	CNIEJ14	CNIEJ13	CNIEJ12	CNIEJ11	CNIEJ10	CNIEJ9	CNIEJ8	CNIEJ7	CNIEJ6	CNIEJ5	CNIEJ4	CNIEJ3	CNIEJ2	CNIEJ1	CNIEJ0	0000
0890	CNSTATJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATJ15	CN STATJ14	CN STATJ13	CN STATJ12	CN STATJ11	CN STATJ10	CN STATJ9	CN STATJ8	CN STATJ7	CN STATJ6	CN STATJ5	CN STATJ4	CN STATJ3	CN STATJ2	CN STATJ1	CN STATJ0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

TABLE 12-22: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1620	RPE8R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE8R<3:0>				0000
1624	RPE9R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE9R<3:0>				0000
1640	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF0R<3:0>				0000
1644	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF1R<3:0>				0000
1648	RPF2R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF2R<3:0>				0000
164C	RPF3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF3R<3:0>				0000
1650	RPF4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF4R<3:0>				0000
1654	RPF5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF5R<3:0>				0000
1660	RPF8R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF8R<3:0>				0000
1670	RPF12R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG12R<3:0>				0000
1674	RPF13R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG0R<3:0>				0000
1680	RPG0R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1684	RPG1R(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1698	RPG6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG6R<3:0>				0000
169C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG7R<3:0>				0000
16A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG8R<3:0>				0000
16A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG9R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on 64-pin and 100-pin devices.

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9) (CONTINUED)

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(1)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

REGISTER 15-1: DMTCON: DEADMAN TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Deadman Timer Module Enable bit(1)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is disabled

bit 13-0 **Unimplemented:** Read as '0'

Note 1: This bit only has control when FDMTEN (DEVCFG1<3>) = 0.

REGISTER 15-2: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP1<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STEP1<7:0>:** Preclear Enable bits
01000000 = Enables the Deadman Timer Preclear (Step 1)
All other write patterns = Set BAD1 flag.
These bits are cleared when a DMT reset event occurs. STEP1<7:0> is also cleared if the STEP2<7:0> bits are loaded with the correct value in the correct sequence.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 15-7: DMTPSINTV: POST STATUS CONFIGURE DMT INTERVAL STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-y	R-y	R-y
	PSINTV<7:0>							

Legend:		y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **PSINTV<31:0>:** DMT Window Interval Configuration Status bits
This is always the value of the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.

17.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

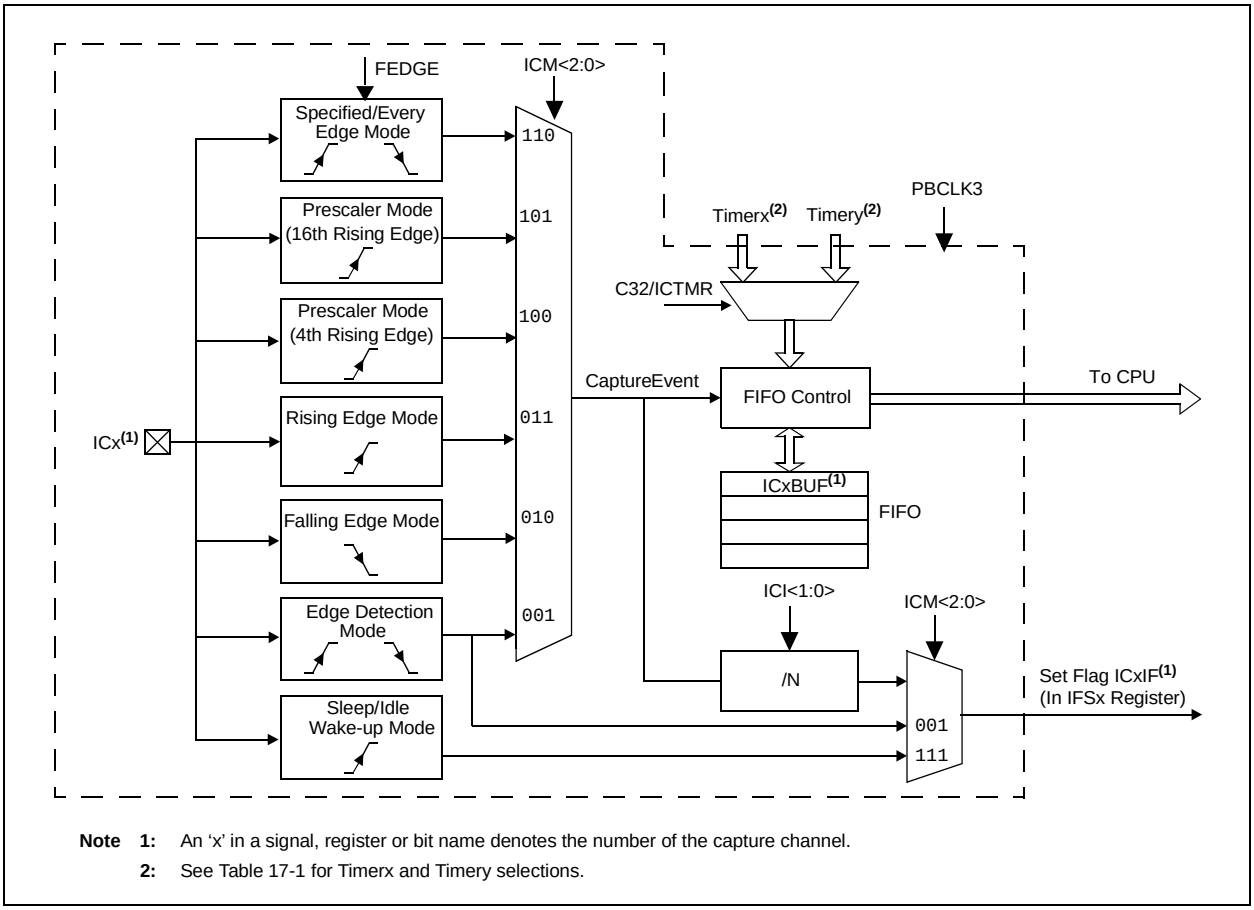
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

2: See Table 17-1 for Timerx and Timery selections.

26.1 Crypto Engine Control Registers

TABLE 26-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>				START	ACTIVE	0000
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>								0000
5024	CETRLLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRLRLEN<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 28-13: AD1CMPn: ADC1 DIGITAL COMPARATOR REGISTER 'n' ('n' = 1, 2, 3, 4, 5 OR 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPHI<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPHI<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPLO<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPLO<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **ADCMPHI<15:0>:** Digital Analog Comparator High Limit Value bits

These bits store the high limit value, which is used for comparisons with the analog-to-digital conversion data. The user is responsible for formatting the data as signed or unsigned to match the data format as specified by the SHxMOD<1:0> bits for the associated S&H circuit and the FRACT bit.

bit 15-0 **ADCMPLO<15:0>:** Digital Analog Comparator Low Limit Value bits

These bits store the low limit value, which is used for comparisons with the analog-to-digital conversion data. The user is responsible for formatting the data as signed or unsigned to match the data format as specified by the SHxMOD<1:0> bits for the associated S&H circuit and the FRACT bit.

Note: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

29.0 CONTROLLER AREA NETWORK (CAN)

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

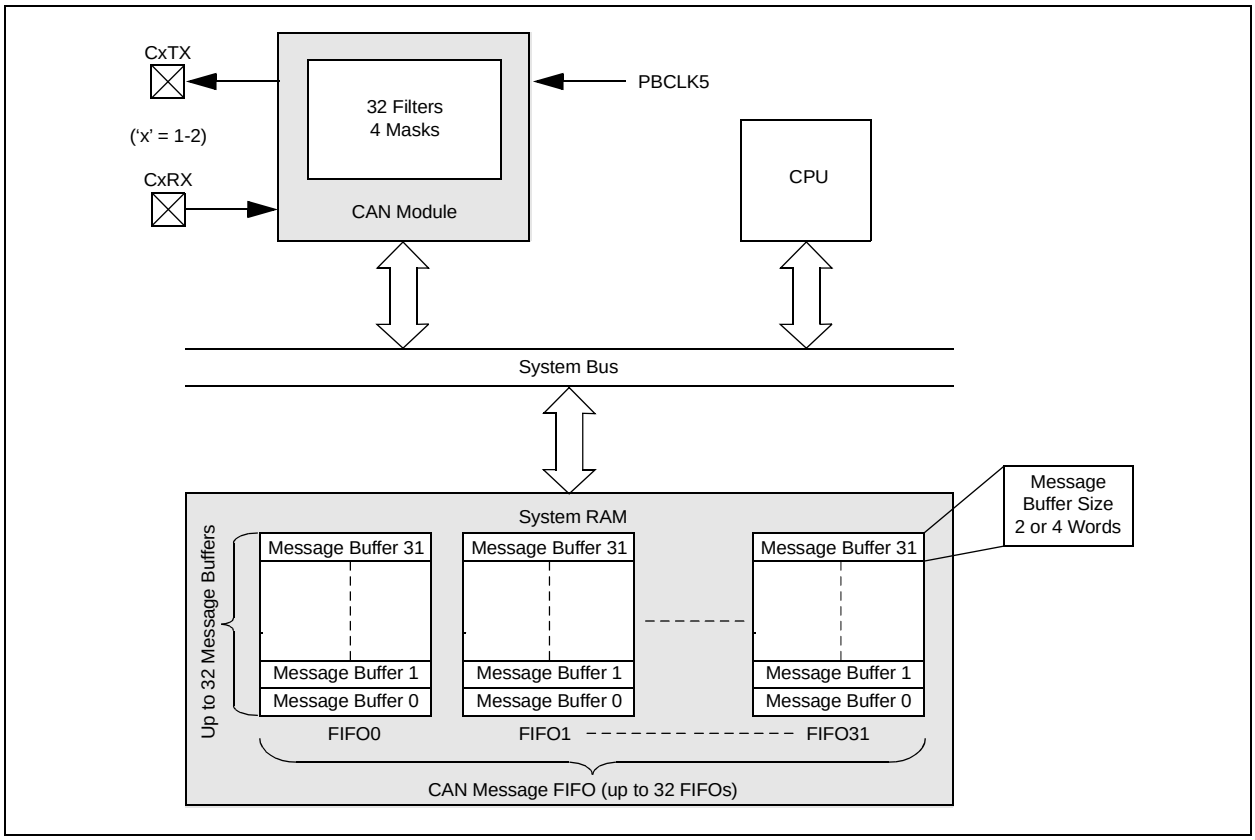
The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
  - 32 message FIFOs
  - Each FIFO can have up to 32 messages for a total of 1024 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 32 acceptance filters for message filtering
  - Four acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
- Additional Features:
  - Loopback, Listen All Messages and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus master on the PIC32 System Bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 29-1 illustrates the general structure of the CAN module.

Note: To avoid cache coherency problems on devices with L1 cache, CAN buffers must only be allocated or accessed from the KSEG1 segment.

FIGURE 29-1: PIC32 CAN MODULE BLOCK DIAGRAM



REGISTER 30-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	TXBUSE(1)	RXBUSE(2)	—	—	—	EWMARK(2)	FWMARK(2)
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONE(2)	PKTPEND(2)	RXACT(2)	—	TXDONE(1)	TXABORT(1)	RXBUFNA(2)	RXOVFLW(2)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSE:** Transmit BVCI Bus Error Interrupt bit(1)

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the TX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 13 **RXBUSE:** Receive BVCI Bus Error Interrupt bit(2)

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the RX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARK:** Empty Watermark Interrupt bit(2)

1 = Empty Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a '0' or a '1' has no effect.

bit 8 **FWMARK:** Full Watermark Interrupt bit(2)

1 = Full Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

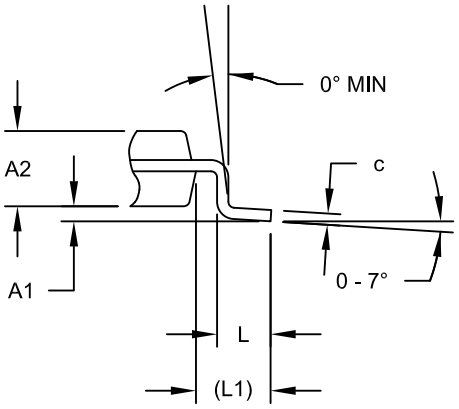
Note 1: This bit is only used for TX operations.
2: This bit is only used for RX operations.

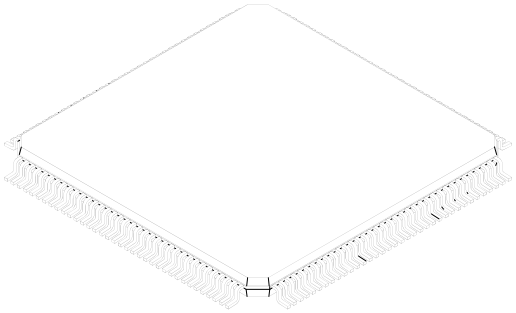
Note: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

NOTES:

144-Lead Plastic Thin Quad Flatpack (PH) - 16x16x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		144	
Lead Pitch	e		0.40 BSC	
Overall Height	A	-	-	1.20
Molded PackageThickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Overall Width	D		18.00 BSC	
Overall Length	E		18.00 BSC	
Molded Body Width	D1		16.00 BSC	
Molded Body Length	E1		16.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.13	-	0.23

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-155B Sheet 2 of 2

TABLE B-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
28.0 "12-bit Pipelined Analog-to-Digital Converter (ADC)"	Figure 28-1, Figure 28-2, and Figure 28-3 were updated. Register names were updated in the ADC Register Map (see Table 28-1). The OVRSAM<2:0> bit values were updated (see Register 28-14).
34.0 "Special Features"	The DEVCFG3/ADEVCFG3 register was updated (see Register 34-6).
37.0 "Electrical Characteristics"	Various electrical specifications were updated, including: • The minimum value for parameter DC10 (V_{DD}) in the DC Temperature and Voltage Specifications was updated (see Table 37-4). • The minimum and maximum values for parameter BO10 (V_{BOR}) were updated in the BOR Electrical Characteristics (see Table 37-4). • Updated the third and fourth bullet list items in Note 2 in DC Characteristics: Operating Current (I_{DD}) (see Table 37-6). • Updated the third and fourth bullet list items in Note 1 in DC Characteristics: Idle Current (I_{IDLE}) (see Table 37-7). • Updated the third and fourth bullet list items in Note 1in DC Characteristics: Power-Down Current (I_{PD}) (see Table 37-8). • Added Note 6 and updated parameters DI20, DI28a, DI28b, DI30, and DI31 in DC Characteristics: I/O Pin Input Specifications (see Table 37-9). • Added DC Characteristics: I/O Pin Input Injection Current Specifications (see Table 37-10). • Added parameter DO50 to Capacitive Loading Requirements on Output Pins (see Table 37-15). • Note 3 was added and the Conditions were updated for parameter OS42 in the External Clock Timing Requirements (see Table 37-16). • Updated the Minimum value for parameter OS51 (F_{SYS}) in the System Timing Requirements (see Table 37-17). • Added parameter OS54a and updated the Maximum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 37-18). • The Internal Backup FRC (BFRC) Accuracy specification was added (see Table 37-21). • The SQI Input and Output Timing Characteristics diagram were updated (see Figure 37-14 and Figure 37-15). • The SQI Timing Requirements were updated (see Table 37-33). • Parameter AD13 was removed (see Table 37-37). • The Min. and Max. values for parameter TS12 and the Conditions for parameter TS13 and TS14 in the Temperature Sensor Specifications were updated (see Table 36-39).
38.0 "AC and DC Characteristics Graphs"	Updated Typical Temperature Sensor Voltage (see Figure 38-7).
Appendix A: "Migrating from PIC32MX5XX/6XX/7XX to PIC32MZ"	New appendix for migrating to PIC32MZ devices was added.