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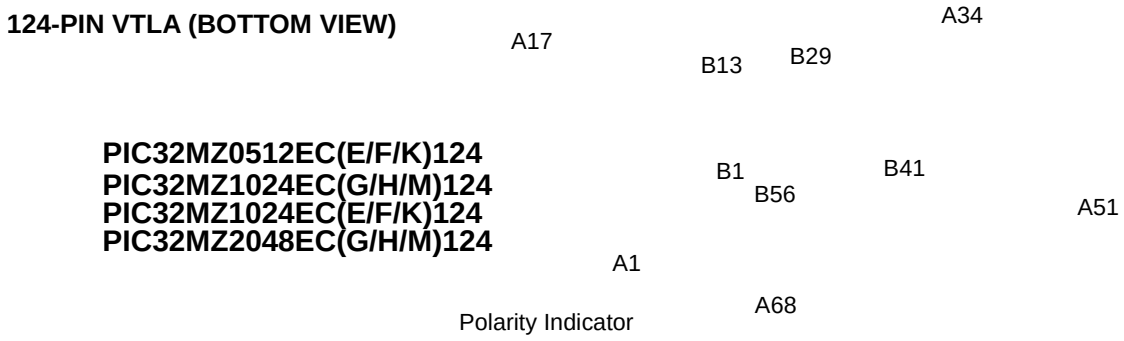
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ech144-i-ph

TABLE 4: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)



Package Pin #	Full Pin Name	Package Pin #	Full Pin Name
B1	EBIA5/AN34/PMA5/RA5	B29	VSS
B2	EBID6/AN16/PMD6/RE6	B30	D+
B3	EBIA6/AN22/RPC1/PMA6/RC1	B31	RPF2/SDA3/RF2
B4	AN36/ETXD1/RJ9	B32	ERXD0/RH8
B5	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	B33	ECOL/RH10
B6	AN14/C1IND/RPG6/SCK2/RG6	B34	EBIRDY1/SDA2/RA3
B7	EBIA3/AN12/C2IND/RPG8/SCL4/PMA3/RG8	B35	VDD
B8	VDD	B36	EBIA9/RPF4/SDA5/PMA9/RF4
B9	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	B37	RPA14/SCL1/RA14
B10	AN25/RPE8/RE8	B38	EBIA15/RPD9/PMCS2/PMA15/RD9
B11	AN45/C1INA/RPB5/RB5	B39	EMDC/RPD11/RD11
B12	AN37/ERXCLK/EREFCLK/RJ11	B40	ERXDV/ECRSDV/RH13
B13	VSS	B41	SOSCI/RPC13/RC13
B14	PGEC2/AN46/RPB6/RB6	B42	EBID14/RPD2/PMD14/RD2
B15	VREF-/CVREF-/AN27/RA9	B43	EBID12/RPD12/PMD12/RD12
B16	AVDD	B44	ETXERR/RJ0
B17	AN38/ETXD2/RH0	B45	EBIRDY3/RJ2
B18	EBIA10/AN48/RPB8/PMA10/RB8	B46	$\overline{\text{SQICS1}}$/RPD5/RD5
B19	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	B47	ETXCLK/RPD7/RD7
B20	VSS	B48	VSS
B21	TCK/EBIA19/AN29/RA1	B49	EBID10/RPF1/PMD10/RF1
B22	TDO/EBIA17/AN31/RPF12/RF12	B50	EBID8/RPG0/PMD8/RG0
B23	AN8/RB13	B51	TRD3/SQID3/RA7
B24	EBIA0/AN10/RPB15/OCFB/PMA0/RB15	B52	EBID0/PMD0/RE0
B25	VDD	B53	VDD
B26	AN41/ERXD1/RH5	B54	TRD2/SQID2/RG14
B27	AN32/AETXD0/RPD14/RD14	B55	TRD0/SQID0/RG13
B28	OSC1/CLKI/RC12	B56	EBID3/RPE3/PMD3/RE3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

NOTES:

REGISTER 5-7: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

bit 4 **UBWP4:** Upper Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF enabled
0 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF disabled

bit 3 **UBWP3:** Upper Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF enabled
0 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF disabled

bit 2 **UBWP2:** Upper Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF enabled
0 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF disabled

bit 1 **UBWP1:** Upper Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF enabled
0 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF disabled

bit 0 **UBWP0:** Upper Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF enabled
0 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF disabled

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

10.1 DMA Control Registers

TABLE 10-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
1010	DMASTAT	31:16	RDWR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	DMACH<2:0>			0000
1020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

TABLE 10-2: DMA CRC REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
1040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
1050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 10-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHPDAT<15:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All other modes:
Unused.

TABLE 12-8: PORTD REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD15	ANSD14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	—	—	—	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FE3F
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	—	—	—	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	—	—	—	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	—	—	—	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	—	—	—	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	—	—	—	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	—	—	—	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	—	—	—	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

16.0 WATCHDOG TIMER (WDT)

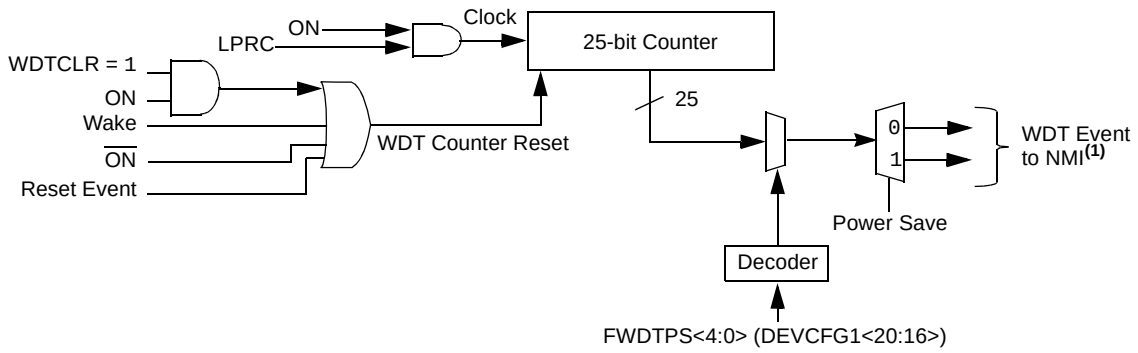
Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

When enabled, the Watchdog Timer (WDT) operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 16-1: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: Refer to **Section 6.0 "Resets"** for more information.

REGISTER 20-3: SQI1CFG: SQI CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	SQIEN	—	—	—	—	—	CSEN<1:0>	
23:16	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0, HC
	—	—	DATAEN<1:0>		—	—	—	RESET
15:8	U-0	r-0	r-0	R/W-0	r-0	R/W-0	R/W-0	R/W-0
	—	—	—	BURSTEN(1)	—	HOLD	WP	SERMODE
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXLATCH	—	LSBF	CPOL	CPHA	MODE<2:0>		

Legend:	HC = Hardware Cleared	r = Reserved	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **SQIEN:** SQI Enable bit
1 = SQI module is enabled
0 = SQI module is disabled

bit 30-26 **Unimplemented:** Read as '0'

bit 25-24 **CSEN<1:0>:** Chip Select Output Enable bits
11 = Chip Select 0 and Chip Select 1 are used
10 = Chip Select 1 is used (Chip Select 0 is not used)
01 = Chip Select 0 is used (Chip Select 1 is not used)
00 = Chip Select 0 and Chip Select 1 are not used

bit 23-22 **Unimplemented:** Read as '0'

bit 21-20 **DATAEN<1:0>:** Data Output Enable bits
11 = Reserved
10 = SQID3-SQID0 outputs are enabled
01 = SQID1 and SQID0 data outputs are enabled
00 = SQID0 data output is enabled

bit 19-17 **Unimplemented:** Read as '0'

bit 16 **RESET:** Software Reset Select bit
This bit is automatically cleared by the SQI module. All of the internal state machines and FIFO pointers are reset by this reset pulse.
1 = A reset pulse is generated
0 = A reset pulse is not generated

bit 15 **Unimplemented:** Read as '0'

bit 14-13 **Reserved:** Must be programmed as '0'

bit 12 **BURSTEN:** Burst Configuration bit(1)
1 = Burst is enabled
0 = Burst is not enabled

bit 11 **Reserved:** Must be programmed as '0'

bit 10 **HOLD:** Hold bit
In Single Lane or Dual Lane mode, this bit is used to drive the SQID3 pin, which can be used for devices with a HOLD input pin. The meaning of the values for this bit will depend on the device to which SQID3 is connected.

Note 1: This bit must be programmed as '1'.

NOTES:

REGISTER 25-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	HR10<1:0>		HR01<3:0>			
23:16	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	MIN10<2:0>			MIN01<3:0>			
15:8	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	SEC10<2:0>			SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **HR10<1:0>:** Binary Coded Decimal value of hours bits, tens digit; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, ones digit; contains a value from 0 to 9

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MIN10<2:0>:** Binary Coded Decimal value of minutes bits, tens digit; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, ones digit; contains a value from 0 to 9

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SEC10<2:0>:** Binary Coded Decimal value of seconds bits, tens digit; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, ones digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

27.1 RNG Control Registers

TABLE 27-2: RANDOM NUMBER GENERATOR (RNG) REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	RNGVER	31:16	ID<15:0>																xxxx
		15:0	VERSION<7:0>								REVISION<7:0>								xxxx
6004	RNGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	LOAD	—	CONT	PRNGEN	TRNGEN	PLEN<7:0>								0064
6008	RNGPOLY1	31:16	POLY<31:0>																FFFF
		15:0																	0000
600C	RNGPOLY2	31:16	POLY<31:0>																FFFF
		15:0																	0000
6010	RNGNUMGEN1	31:16	RNG<31:0>																FFFF
		15:0																	FFFF
6014	RNGNUMGEN2	31:16	RNG<31:0>																FFFF
		15:0																	FFFF
6018	RNGSEED1	31:16	SEED<31:0>																0000
		15:0																	0000
601C	RNGSEED2	31:16	SEED<31:0>																0000
		15:0																	0000
6020	RNGCNT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RCNT<6:0>							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 27-5: RNGSEEDx: TRUE RANDOM NUMBER GENERATOR SEED REGISTER 'x' ('x' = 1 OR 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SEED<31:0>:** TRNG MSb/LSb Value bits (RNGSEED1 = LSb, RNGSEED2 = MSb)

REGISTER 27-6: RNGCNT: TRUE RANDOM NUMBER GENERATOR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **RCNT<6:0>:** Number of Valid TRNG MSB 32 bits

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B104	AD1DATA19	31:16	ADC Output Register 19 <31:16>																0000
		15:0	ADC Output Register 19<15:0>																0000
B108	AD1DATA20	31:16	ADC Output Register 20 <31:16>																0000
		15:0	ADC Output Register 20<15:0>																0000
B10C	AD1DATA21	31:16	ADC Output Register 21 <31:16>																0000
		15:0	ADC Output Register 21 <15:0>																0000
B110	AD1DATA22	31:16	ADC Output Register 22 <31:16>																0000
		15:0	ADC Output Register 22<15:0>																0000
B114	AD1DATA23	31:16	ADC Output Register 23 <31:16>																0000
		15:0	ADC Output Register 23<15:0>																0000
B118	AD1DATA24	31:16	ADC Output Register 24 <31:16>																0000
		15:0	ADC Output Register 24<15:0>																0000
B11C	AD1DATA25	31:16	ADC Output Register 25 <31:16>																0000
		15:0	ADC Output Register 25 <15:0>																0000
B120	AD1DATA26	31:16	ADC Output Register 26 <31:16>																0000
		15:0	ADC Output Register 26<15:0>																0000
B124	AD1DATA27	31:16	ADC Output Register 27 <31:16>																0000
		15:0	ADC Output Register 27<15:0>																0000
B128	AD1DATA28	31:16	ADC Output Register 28 <31:16>																0000
		15:0	ADC Output Register 28<15:0>																0000
B12C	AD1DATA29	31:16	ADC Output Register 29 <31:16>																0000
		15:0	ADC Output Register 29 <15:0>																0000
B130	AD1DATA30	31:16	ADC Output Register 30 <31:16>																0000
		15:0	ADC Output Register 30<15:0>																0000
B134	AD1DATA31	31:16	ADC Output Register 31 <31:16>																0000
		15:0	ADC Output Register 31 <15:0>																0000
B138	AD1DATA32	31:16	ADC Output Register 32 <31:16>																0000
		15:0	ADC Output Register 32 <15:0>																0000
B13C	AD1DATA33	31:16	ADC Output Register 33 <31:16>																0000
		15:0	ADC Output Register 33 <15:0>																0000
B140	AD1DATA34	31:16	ADC Output Register 34 <31:16>																0000
		15:0	ADC Output Register 34 <15:0>																0000
B144	AD1DATA35	31:16	ADC Output Register 35 <31:16>																0000
		15:0	ADC Output Register 35 <15:0>																0000
B148	AD1DATA36	31:16	ADC Output Register 36 <31:16>																0000
		15:0	ADC Output Register 36 <15:0>																0000
B14C	AD1DATA37	31:16	ADC Output Register 37 <31:16>																0000
		15:0	ADC Output Register 37 <15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 28-5: AD1GIRQEN1: ADC1 GLOBAL INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN31	AGIEN30	AGIEN29	AGIEN28	AGIEN27	AGIEN26	AGIEN25	AGIEN24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN23	AGIEN22	AGIEN21	AGIEN20	AGIEN19	AGIEN18	AGIEN17	AGIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **AGIENx:** Global ADC Interrupt Enable bits ('x' = 0-31)

1 = A data ready event (transition from 0 to 1 of the ARDYx bit) will generate a Global ADC interrupt
0 = No global interrupt is generated on a data ready event

The Global ADC Interrupt is enabled by setting a bit in the IECx registers (refer to **Section 7.0 "CPU Exceptions and Interrupt Controller"** for details).

Note 1: The enable bits do not affect assertion of the individual interrupt output. Interrupts generated for individual ARDY events are enabled in the IECx register.

2: AGIENx = ANx, where 'x' = 0-31.

REGISTER 30-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits

Increment count for frames that were successfully transmitted after there was more than one collision.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

34.2 Registers

TABLE 34-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FFC0	DEVCFG3	31:16	—	FUSBIDIO	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN	—	—	—	—	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
FFC4	DEVCFG2	31:16	—	UPLLFSEL	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
FFC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
FFCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>		—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
FFD0	DEVCP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD4	DEVCP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD8	DEVCP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFDC	DEVCP0	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE0	DEVSIGN3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE4	DEVSIGN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE8	DEVSIGN1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFEC	DEVSIGN0	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

REGISTER 34-1: DEVSIGN0/ADEVSIGN0: DEVICE SIGNATURE WORD 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '0'

bit 30-0 **Reserved:** Write as '1'

Note:	The DEVSIGN1 through DEVSIGN3 and ADEVSIGN1 through ADEVSIGN3 registers are used for Quad Word programming operation when programming the DEVSIGN0/ADESIGN0 registers, and do not contain any valid information.

REGISTER 34-2: DEVCP0/ADEVCP0: DEVICE CODE-PROTECT 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	R/P	r-1	r-1	r-1	r-1
	—	—	—	CP	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Reserved:** Write as '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection is disabled
0 = Protection is enabled

bit 27-0 **Reserved:** Write as '1'

Note:	The DEVCP1 through DEVCP3 and ADEVCP1 through ADEVCP3 registers are used for Quad Word programming operation when programming the DEVCP0/ADEVCP0 registers, and do not contain any valid information.

36.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

36.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

36.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

36.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

36.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
Fail-Safe Clock Monitor (FSCM)	
On PIC32MX devices, the internal FRC became the clock source on a failure of the clock source.	On PIC32MZ devices, a separate internal Backup FRC (BFRC) becomes the clock source upon a failure at the clock source.
On PIC32MX devices, a clock failure resulted in the triggering of a specific interrupt when the switchover was complete. **FSCM generates an interrupt.**	On PIC32MZ devices, a NMI is triggered instead, and must be handled by the NMI routine. **FSCM generates a NMI.**
FCKSM<1:0> (DEVCFG1<15:14>) **1x = Clock switching is disabled, FSCM is disabled** 01 = Clock switching is enabled, FSCM is disabled **00 = Clock switching is enabled, FSCM is enabled**	The definitions of the FCKSM<1:0> bits has changed on PIC32MZ devices. FCKSM<1:0> (DEVCFG1<15:14>) **11 = Clock switching is enabled and clock monitoring is enabled** **10 = Clock switching is disabled and clock monitoring is enabled** 01 = Clock switching is enabled and clock monitoring is disabled **00 = Clock switching is disabled and clock monitoring is disabled**
On PIC32MX devices, the CF (OSCCON<3>) bit indicates a clock failure. Writing to this bit initiates a FSCM event.	On PIC32MZ devices, the CF (OSCCON<3>) bit has the same functionality as that of PIC32MX device; however, an additional CF(RNMICON<1>) bit is available to indicate a NMI event. Writing to this bit causes a NMI event, but not a FSCM event.
On PIC32MX devices, the CLKLOCK (OSCCON<7>) bit is controlled by the FSCM. CLKLOCK (OSCCON<7>) **If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):** 1 = Clock and PLL selections are locked 0 = Clock and PLL selections are not locked and may be modified **If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):** **Clock and PLL selections are never locked and may be modified.**	On PIC32MZ devices, the CLKLOCK (OSCCON<7>) bit is not impacted by the FSCM. CLKLOCK (OSCCON<7>) 1 = Clock and PLL selections are locked 0 = Clock and PLL selections are not locked and may be modified

Table A-2 illustrates the difference in code setup of the respective parts for maximum speed using an external 24 MHz crystal.

TABLE A-2: CODE DIFFERENCES FOR MAXIMUM SPEED USING AN EXTERNAL 24 MHz CRYSTAL

PIC32MX5XX/6XX/7XX at 80 MHz	PIC32MZ at 200 MHz

`#include <xc.h>`
 	
`#pragma config POSCMOD = HS`
`#pragma config FNOSC = PRIPLL`
 	
`#pragma config FPLLIDIV = DIV_6`
 	
`#pragma config FPLLMUL = MUL_20`
`#pragma config FPLLODIV = DIV_1`
 	
`#define SYSFREQ (80000000L)`
	`#include <xc.h>`
	
	`#pragma config POSCMOD = HS`
	`#pragma config FNOSC = SPLL`
	`#pragma config FPLLICLK = PLL_POSC`
	`#pragma config FPLLIDIV = DIV_3`
	`#pragma config FPLLRNG = RANGE_5_10_MHZ`
	`#pragma config FPLLMULT = MUL_50`
	`#pragma config FPLLODIV = DIV_2`
	
	`#define SYSFREQ (200000000L)`

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