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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ech144-i-pl

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-1: ADC1 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
AN0	16	25	A18	36	I	Analog	Analog Input Channels
AN1	15	24	A17	35	I	Analog	
AN2	14	23	A16	34	I	Analog	
AN3	13	22	A14	31	I	Analog	
AN4	12	21	A13	26	I	Analog	
AN5	23	34	B19	49	I	Analog	
AN6	24	35	A24	50	I	Analog	
AN7	27	41	A27	59	I	Analog	
AN8	28	42	B23	60	I	Analog	
AN9	29	43	A28	61	I	Analog	
AN10	30	44	B24	62	I	Analog	
AN11	10	16	B9	21	I	Analog	
AN12	6	12	B7	16	I	Analog	
AN13	5	11	A8	15	I	Analog	
AN14	4	10	B6	14	I	Analog	
AN15	3	5	A4	5	I	Analog	
AN16	2	4	B2	4	I	Analog	
AN17	1	3	A3	3	I	Analog	
AN18	64	100	A67	144	I	Analog	
AN19	—	9	A7	13	I	Analog	
AN20	—	8	B5	12	I	Analog	
AN21	—	7	A6	11	I	Analog	
AN22	—	6	B3	6	I	Analog	
AN23	—	1	A2	1	I	Analog	
AN24	—	17	A11	22	I	Analog	
AN25	—	18	B10	23	I	Analog	
AN26	—	19	A12	24	I	Analog	
AN27	—	28	B15	39	I	Analog	
AN28	—	29	A20	40	I	Analog	
AN29	—	38	B21	56	I	Analog	
AN30	—	39	A26	57	I	Analog	
AN31	—	40	B22	58	I	Analog	
AN32	—	47	B27	69	I	Analog	
AN33	—	48	A32	70	I	Analog	
AN34	—	2	B1	2	I	Analog	
AN35	—	—	A5	7	I	Analog	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFCA_#)	Register Name	Bit Range	Bits																All Reset
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF1DEVCFG3	31:0	Note: See Table 34-2 for the bit descriptions.																XXXX
FF44	ABF1DEVCFG2	31:0																	XXXX
FF48	ABF1DEVCFG1	31:0																	XXXX
FF4C	ABF1DEVCFG0	31:0																	XXXX
FF50	ABF1DEVCP3	31:0																	XXXX
FF54	ABF1DEVCP2	31:0																	XXXX
FF58	ABF1DEVCP1	31:0																	XXXX
FF5C	ABF1DEVCP0	31:0																	XXXX
FF60	ABF1DEVSIGN3	31:0																	XXXX
FF64	ABF1DEVSIGN2	31:0																	XXXX
FF68	ABF1DEVSIGN1	31:0																	XXXX
FF6C	ABF1DEVSIGN0	31:0																	XXXX
FF70	ABF1SEQ3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
FF74	ABF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
FF78	ABF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
FF7C	ABF1SEQ0	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX
FFC0	BF1DEVCFG3	31:0	Note: See Table 34-1 for the bit descriptions.																XXXX
FFC4	BF1DEVCFG2	31:0																	XXXX
FFC8	BF1DEVCFG1	31:0																	XXXX
FFCC	BF1DEVCFG0	31:0																	XXXX
FFD0	BF1DEVCP3	31:0																	XXXX
FFD4	BF1DEVCP2	31:0																	XXXX
FFD8	BF1DEVCP1	31:0																	XXXX
FFDC	BF1DEVCP0	31:0																	XXXX
FFE0	BF1DEVSIGN3	31:0																	XXXX
FFE4	BF1DEVSIGN2	31:0																	XXXX
FFE8	BF1DEVSIGN1	31:0																	XXXX
FFEC	BF1DEVSIGN0	31:0																	XXXX
FFF0	BF1SEQ3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
FFF4	BF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
FFF8	BF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
FFFC	BF1SEQ0	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 4-7: SYSTEM BUS REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
0510	SBFLAG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	T13PGV	T12PGV	T11PGV	T10PGV	T9PGV	T8PGV	T7PGV	T6PGV	T5PGV	T4PGV	T3PGV	T2PGV	T1PGV	T0PGV

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: SYSTEM BUS TARGET 0 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
8020	SBT0ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000
8024	SBT0ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8028	SBT0ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8030	SBT0ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8038	SBT0ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8040	SBT0REG0	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—
8050	SBT0RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8058	SBT0WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8060	SBT0REG1	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—
8070	SBT0RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8078	SBT0WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Parallel Master Port Error	_PMP_ERROR_VECTOR	129	OFF129<17:1>	IFS4<1>	IEC4<1>	IPC32<12:10>	IPC32<9:8>	Yes
Comparator 1 Interrupt	_COMPARATOR_1_VECTOR	130	OFF130<17:1>	IFS4<2>	IEC4<2>	IPC32<20:18>	IPC32<17:16>	No
Comparator 2 Interrupt	_COMPARATOR_2_VECTOR	131	OFF131<17:1>	IFS4<3>	IEC4<3>	IPC32<28:26>	IPC32<25:24>	No
USB General Event	_USB1_VECTOR	132	OFF132<17:1>	IFS4<4>	IEC4<4>	IPC33<4:2>	IPC33<1:0>	Yes
USB DMA Event	_USB1_DMA_VECTOR	133	OFF133<17:1>	IFS4<5>	IEC4<5>	IPC33<12:10>	IPC33<9:8>	Yes
DMA Channel 0	_DMA0_VECTOR	134	OFF134<17:1>	IFS4<6>	IEC4<6>	IPC33<20:18>	IPC33<17:16>	No
DMA Channel 1	_DMA1_VECTOR	135	OFF135<17:1>	IFS4<7>	IEC4<7>	IPC33<28:26>	IPC33<25:24>	No
DMA Channel 2	_DMA2_VECTOR	136	OFF136<17:1>	IFS4<8>	IEC4<8>	IPC34<4:2>	IPC34<1:0>	No
DMA Channel 3	_DMA3_VECTOR	137	OFF137<17:1>	IFS4<9>	IEC4<9>	IPC34<12:10>	IPC34<9:8>	No
DMA Channel 4	_DMA4_VECTOR	138	OFF138<17:1>	IFS4<10>	IEC4<10>	IPC34<20:18>	IPC34<17:16>	No
DMA Channel 5	_DMA5_VECTOR	139	OFF139<17:1>	IFS4<11>	IEC4<11>	IPC34<28:26>	IPC34<25:24>	No
DMA Channel 6	_DMA6_VECTOR	140	OFF140<17:1>	IFS4<12>	IEC4<12>	IPC35<4:2>	IPC35<1:0>	No
DMA Channel 7	_DMA7_VECTOR	141	OFF141<17:1>	IFS4<13>	IEC4<13>	IPC35<12:10>	IPC35<9:8>	No
SPI2 Fault	_SPI2_FAULT_VECTOR	142	OFF142<17:1>	IFS4<14>	IEC4<14>	IPC35<20:18>	IPC35<17:16>	Yes
SPI2 Receive Done	_SPI2_RX_VECTOR	143	OFF143<17:1>	IFS4<15>	IEC4<15>	IPC35<28:26>	IPC35<25:24>	Yes
SPI2 Transfer Done	_SPI2_TX_VECTOR	144	OFF144<17:1>	IFS4<16>	IEC4<16>	IPC36<4:2>	IPC36<1:0>	Yes
UART2 Fault	_UART2_FAULT_VECTOR	145	OFF145<17:1>	IFS4<17>	IEC4<17>	IPC36<12:10>	IPC36<9:8>	Yes
UART2 Receive Done	_UART2_RX_VECTOR	146	OFF146<17:1>	IFS4<18>	IEC4<18>	IPC36<20:18>	IPC36<17:16>	Yes
UART2 Transfer Done	_UART2_TX_VECTOR	147	OFF147<17:1>	IFS4<19>	IEC4<19>	IPC36<28:26>	IPC36<25:24>	Yes
I2C2 Bus Collision Event ⁽²⁾	_I2C2_BUS_VECTOR	148	OFF148<17:1>	IFS4<20>	IEC4<20>	IPC37<4:2>	IPC37<1:0>	Yes
I2C2 Slave Event ⁽²⁾	_I2C2_SLAVE_VECTOR	149	OFF149<17:1>	IFS4<21>	IEC4<21>	IPC37<12:10>	IPC37<9:8>	Yes
I2C2 Master Event ⁽²⁾	_I2C2_MASTER_VECTOR	150	OFF150<17:1>	IFS4<22>	IEC4<22>	IPC37<20:18>	IPC37<17:16>	Yes
Control Area Network 1	_CAN1_VECTOR	151	OFF151<17:1>	IFS4<23>	IEC4<23>	IPC37<28:26>	IPC37<25:24>	Yes
Control Area Network 2	_CAN2_VECTOR	152	OFF152<17:1>	IFS4<24>	IEC4<24>	IPC38<4:2>	IPC38<1:0>	Yes
Ethernet Interrupt	_ETHERNET_VECTOR	153	OFF153<17:1>	IFS4<25>	IEC4<25>	IPC38<12:10>	IPC38<9:8>	Yes
SPI3 Fault	_SPI3_FAULT_VECTOR	154	OFF154<17:1>	IFS4<26>	IEC4<26>	IPC38<20:18>	IPC38<17:16>	Yes
SPI3 Receive Done	_SPI3_RX_VECTOR	155	OFF155<17:1>	IFS4<27>	IEC4<27>	IPC38<28:26>	IPC38<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EC Family Features"** for the list of available peripherals.

Note 2: This interrupt source is not available on 64-pin devices.

Note 3: This interrupt source is not available on 100-pin devices.

Note 4: This interrupt source is not available on 124-pin devices.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
I2C5 Slave Event	_I2C5_SLAVE_VECTOR	183	OFF183<17:1>	IFS5<23>	IEC5<23>	IPC45<28:26>	IPC45<25:24>	Yes
I2C5 Master Event	_I2C5_MASTER_VECTOR	184	OFF184<17:1>	IFS5<24>	IEC5<24>	IPC46<4:2>	IPC46<1:0>	Yes
SPI6 Fault ⁽²⁾	_SPI6_FAULT_VECTOR	185	OFF185<17:1>	IFS5<25>	IEC5<25>	IPC46<12:10>	IPC46<9:8>	Yes
SPI6 Receive Done ⁽²⁾	_SPI6_RX_VECTOR	186	OFF186<17:1>	IFS5<26>	IEC5<26>	IPC46<20:18>	IPC46<17:16>	Yes
SPI6 Transfer Done ⁽²⁾	_SPI6_TX_VECTOR	187	OFF187<17:1>	IFS5<27>	IEC5<27>	IPC46<28:26>	IPC46<25:24>	Yes
UART6 Fault	_UART6_FAULT_VECTOR	188	OFF188<17:1>	IFS5<28>	IEC5<28>	IPC47<4:2>	IPC47<1:0>	Yes
UART6 Receive Done	_UART6_RX_VECTOR	189	OFF189<17:1>	IFS5<29>	IEC5<29>	IPC47<12:10>	IPC47<9:8>	Yes
UART6 Transfer Done	_UART6_TX_VECTOR	190	OFF190<17:1>	IFS5<30>	IEC5<30>	IPC47<20:18>	IPC47<17:16>	Yes
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EC Family Features”** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

8.2 Oscillator Control Registers

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1200	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			DRMEN	SOSCRDY	—	—	—	—	—	—	0000
		15:0	—	COSC<2:0>				—	NOSC<2:0>			CLKLOCK	ULOCK	SLOCK	SLPEN	CF	—	SOSCEN	OSWEN
1210	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	TUN<5:0>							
1220	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>							01xx
		15:0	—	—	—	—	—	PLLDIV<2:0>			PLLICK	—	—	—	—	PLLRANGE<2:0>			0x0x
1280	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	—	ROSEL<3:0>			
1290	REFO1TRIM	31:16	ROTRIM<8:0>															0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12A0	REFO2CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	—	ROSEL<3:0>			
12B0	REFO2TRIM	31:16	ROTRIM<8:0>															0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12C0	REFO3CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	—	ROSEL<3:0>			
12D0	REFO3TRIM	31:16	ROTRIM<8:0>															0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12E0	REFO4CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	—	ROSEL<3:0>			
12F0	REFO4TRIM	31:16	ROTRIM<8:0>															0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1300	PB1DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1310	PB2DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1320	PB3DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1330	PB4DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1340	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1360	PB7DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1370	PB8DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER (CONTINUED)

- bit 4 **CHAEN:** Channel Automatic Enable bit
 1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
 0 = Channel is disabled on block transfer complete
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **CHEDET:** Channel Event Detected bit
 1 = An event has been detected
 0 = No events have been detected
- bit 1-0 **CHPRI<1:0>:** Channel Priority bits
 11 = Channel has priority 3 (highest)
 10 = Channel has priority 2
 01 = Channel has priority 1
 00 = Channel has priority 0

- Note 1:** The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).
- 2:** When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-2: USBCSR1: USB CONTROL STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	U-0
	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-17 **EP7TXIE:EP1TXIE:** Endpoint 'n' Transmit Interrupt Enable bits

1 = Endpoint Transmit interrupt events are enabled

0 = Endpoint Transmit interrupt events are not enabled

bit 16 **EP0IE:** Endpoint 0 Interrupt Enable bit

1 = Endpoint 0 interrupt events are enabled

0 = Endpoint 0 interrupt events are not enabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7-1 **EP7RXIF:EP1RXIF:** Endpoint 'n' RX Interrupt bit

1 = Endpoint has a receive event to be serviced

0 = No interrupt event

bit 0 **Unimplemented:** Read as '0'

PIC32MZ Embedded Connectivity (EC) Family

TABLE 12-2: OUTPUT PIN SELECTION

RPN Port Pin	RPNR SFR	RPNR bits	RPNR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect 0001 = U3TX 0010 = U4RTS 0011 = Reserved 0100 = Reserved 0101 = SDO1 0110 = SDO2 0111 = SDO3 1000 = Reserved 1001 = SDO5 ⁽¹⁾ 1010 = SS6 ⁽¹⁾ 1011 = OC3 1100 = OC6 1101 = REFCLKO4 1110 = C2OUT 1111 = C1TX ⁽³⁾
RPG8	RPG8R	RPG8R<3:0>	
RPF4	RPF4R	RPF4R<3:0>	
RPD10	RPD10R	RPD10R<3:0>	
RPF1	RPF1R	RPF1R<3:0>	
RPB9	RPB9R	RPB9R<3:0>	
RPB10	RPB10R	RPB10R<3:0>	
RPC14	RPC14R	RPC14R<3:0>	
RPB5	RPB5R	RPB5R<3:0>	
RPC1 ⁽¹⁾	RPC1R ⁽¹⁾	RPC1R<3:0> ⁽¹⁾	
RPD14 ⁽¹⁾	RPD14R ⁽¹⁾	RPD14R<3:0> ⁽¹⁾	
RPG1 ⁽¹⁾	RPG1R ⁽¹⁾	RPG1R<3:0> ⁽¹⁾	
RPA14 ⁽¹⁾	RPA14R ⁽¹⁾	RPA14R<3:0> ⁽¹⁾	
RPD6 ⁽²⁾	RPD6R ⁽²⁾	RPD6R<3:0> ⁽²⁾	
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect 0001 = U1TX 0010 = U2RTS 0011 = U5TX 0100 = U6RTS 0101 = SDO1 0110 = SDO2 0111 = SDO3 1000 = SDO4 1001 = SDO5 ⁽¹⁾ 1010 = Reserved 1011 = OC4 1100 = OC7 1101 = Reserved 1110 = Reserved 1111 = REFCLKO1
RPG7	RPG7R	RPG7R<3:0>	
RPF5	RPF5R	RPF5R<3:0>	
RPD11	RPD11R	RPD11R<3:0>	
RPF0	RPF0R	RPF0R<3:0>	
RPB1	RPB1R	RPB1R<3:0>	
RPE5	RPE5R	RPE5R<3:0>	
RPC13	RPC13R	RPC13R<3:0>	
RPB3	RPB3R	RPB3R<3:0>	
RPC4 ⁽¹⁾	RPC4R ⁽¹⁾	RPC4R<3:0> ⁽¹⁾	
RPD15 ⁽¹⁾	RPD15R ⁽¹⁾	RPD15R<3:0> ⁽¹⁾	
RPG0 ⁽¹⁾	RPG0R ⁽¹⁾	RPG0R<3:0> ⁽¹⁾	
RPA15 ⁽¹⁾	RPA15R ⁽¹⁾	RPA15R<3:0> ⁽¹⁾	
RPD7 ⁽²⁾	RPD7R ⁽²⁾	RPD7R<3:0> ⁽²⁾	
RPD9	RPD9R	RPD9R<3:0>	0000 = No Connect 0001 = U3RTS 0010 = U4TX 0011 = Reserved 0100 = U6TX 0101 = SS1 0110 = Reserved 0111 = SS3 1000 = SS4 1001 = SS5 ⁽¹⁾ 1010 = SDO6 ⁽¹⁾ 1011 = OC5 1100 = OC8 1101 = Reserved 1110 = C1OUT 1111 = REFCLKO3
RPG6	RPG6R	RPG6R<3:0>	
RPB8	RPB8R	RPB8R<3:0>	
RPB15	RPB15R	RPB15R<3:0>	
RPD4	RPD4R	RPD4R<3:0>	
RPB0	RPB0R	RPB0R<3:0>	
RPE3	RPE3R	RPE3R<3:0>	
RPB7	RPB7R	RPB7R<3:0>	
RPF12 ⁽¹⁾	RPF12R ⁽¹⁾	RPF12R<3:0> ⁽¹⁾	
RPD12 ⁽¹⁾	RPD12R ⁽¹⁾	RPD12R<3:0> ⁽¹⁾	
RPF8 ⁽¹⁾	RPF8R ⁽¹⁾	RPF8R<3:0> ⁽¹⁾	
RPC3 ⁽¹⁾	RPC3R ⁽¹⁾	RPC3R<3:0> ⁽¹⁾	
RPE9 ⁽¹⁾	RPE9R ⁽¹⁾	RPE9R<3:0> ⁽¹⁾	

Note 1: This selection is not available on 64-pin devices.

Note 2: This selection is not available on 64-pin or 100-pin devices.

Note 3: This selection is not available on devices without a CAN module.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 5 **MSTEN**: Master Mode Enable bit
 1 = Master mode
 0 = Slave mode
- bit 4 **DISSDI**: Disable SDI bit⁽⁴⁾
 1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
 0 = SDI pin is controlled by the SPI module
- bit 3-2 **STXISEL<1:0>**: SPI Transmit Buffer Empty Interrupt Mode bits
 11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
 10 = Interrupt is generated when the buffer is empty by one-half or more
 01 = Interrupt is generated when the buffer is completely empty
 00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
- bit 1-0 **SRXISEL<1:0>**: SPI Receive Buffer Full Interrupt Mode bits
 11 = Interrupt is generated when the buffer is full
 10 = Interrupt is generated when the buffer is full by one-half or more
 01 = Interrupt is generated when the buffer is not empty
 00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

- Note 1:** This bit can only be written when the ON bit = 0. Refer to **Section 37.0 “Electrical Characteristics”** for maximum clock frequency requirements.
- 2:** This bit is not used in the Framed SPI mode. The user should program this bit to ‘0’ for the Framed SPI mode (FRMEN = 1).
- 3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to ‘1’, regardless of the actual value of the CKP bit.
- 4:** This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.3 “Peripheral Pin Select (PPS)”** for more information).

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 19-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	R-0	R-0	R-0	R-0	R-0
	RXBUFELM<4:0>							
23:16	U-0 —	U-0 —	U-0 —	R-0	R-0	R-0	R-0	R-0
	TXBUFELM<4:0>							
15:8	U-0 —	U-0 —	U-0 —	R/C-0, HS FRMERR	R-0 SPIBUSY	U-0 —	U-0 —	R-0 SPITUR
7:0	R-0 SRMT	R/W-0 SPIROV	R-0 SPIRBE	U-0 —	R-1 SPITBE	U-0 —	R-0 SPITBF	R-0 SPIRBF

Legend:	C = Clearable bit	HS = Set in hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR:** SPI Frame Error status bit

1 = Frame error detected

0 = No Frame error detected

This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPI Activity Status bit

1 = SPI peripheral is currently busy with some transactions

0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit

1 = Transmit buffer has encountered an underrun condition

0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)

1 = When SPI module shift register is empty

0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit

1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.

0 = No overflow has occurred

This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)

1 = RX FIFO is empty (CRPTR = SWPTR)

0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

PIC32MZ Embedded Connectivity (EC) Family

NOTES:

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 26-2: CECON: CRYPTO ENGINE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0, HC	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN

Legend:

R = Readable bit

W = Writable bit

HC = Hardware Cleared

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6 **SWRST:** Software Reset bit

1 = Initiate a software reset of the Crypto Engine

0 = Normal operation

bit 5 **SWAPEN:** I/O Swap Enable bit

1 = Input data is byte swapped when read by dedicated DMA

0 = Input data is not byte swapped when read by dedicated DMA

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **BDPCHST:** Buffer Descriptor Processor (BDP) Fetch Enable bit

This bit should be enabled only after all DMA descriptor programming is completed.

1 = BDP descriptor fetch is enabled

0 = BDP descriptor fetch is disabled

bit 1 **BDPPLEN:** Buffer Descriptor Processor Poll Enable bit

This bit should be enabled only after all DMA descriptor programming is completed.

1 = Poll for descriptor until valid bit is set

0 = Do not poll

bit 0 **DMAEN:** DMA Enable bit

1 = Crypto Engine DMA is enabled

0 = Crypto Engine DMA is disabled

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 28-6: AD1GIRQEN2: ADC1 GLOBAL INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	AGIEN44	AGIEN43	AGIEN42	AGIEN41	AGIEN40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN39	AGIEN38	AGIEN37	AGIEN36	AGIEN35	AGIEN34	AGIEN33	AGIEN32

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **AGIENx:** Global ADC Interrupt Enable bits ('x' = 32-44)

1 = A data ready event (transition from 0 to 1 of the ARDYx bit) will generate a Global ADC interrupt

0 = No global interrupt is generated on a data ready event

Note 1: The enable bits do not affect assertion of the individual interrupt output. Interrupts generated for individual ARDYx events are enabled in the IECx register.

2: AGIENx = ANx, where 'x' = 32-42, AGIEN43 = IVREF, and AGIEN44 = IVTEMP.

TABLE 33-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0040	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CVRMD	—	—	—	—	—	—	—	—	—	—	—	AD1MD	0000
0050	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP2MD	CMP1MD	0000
0060	PMD3	31:16	—	—	—	—	—	—	—	OC9MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
		15:0	—	—	—	—	—	—	—	IC9MD	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
0070	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	T9MD	T8MD	T7MD	T6MD	T5MD	T4MD	T3MD	T2MD	T1MD	0000
0080	PMD5	31:16	—	—	CAN2MD	CAN1MD	—	—	—	USBMD	—	—	—	I2C5MD	I2C4MD	I2C3MD	I2C2MD	I2C1MD	0000
		15:0	—	—	SPI6MD	SPI5MD	SPI4MD	SPI3MD	SPI2MD	SPI1MD	—	—	U6MD	U5MD	U4MD	U3MD	U2MD	U1MD	0000
0090	PMD6	31:16	—	—	—	ETHMD	—	—	—	—	SQ1MD	—	—	—	—	—	EB1MD	PMPMD	0000
		15:0	—	—	—	—	REFO4MD	REFO3MD	REFO2MD	REFO1MD	—	—	—	—	—	—	—	RTCCMD	0000
00A0	PMD7	31:16	—	—	—	—	—	—	—	—	—	CRYPTMD	—	RNGMD	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	DMAMD	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

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REGISTER 34-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMA PRI ⁽¹⁾	CPUPRI ⁽¹⁾
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	ICACLK ⁽¹⁾	OCACLK ⁽¹⁾
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	IOLOCK ⁽¹⁾	PMDLOCK ⁽¹⁾	PGLOCK ⁽¹⁾	—	—	USBSEN ⁽¹⁾
7:0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	U-0	R/W-1
	—	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DMA PRI:** DMA Read and DMA Write Arbitration Priority to SRAM bit⁽¹⁾

1 = DMA gets High Priority access to SRAM

0 = DMA uses Least Recently Serviced Arbitration (same as other initiators)

bit 24 **CPUPRI:** CPU Arbitration Priority to SRAM When Servicing an Interrupt bit⁽¹⁾

1 = CPU gets High Priority access to SRAM

0 = CPU uses Least Recently Serviced Arbitration (same as other initiators)

bit 23-18 **Unimplemented:** Read as '0'

bit 17 **ICACLK:** Input Capture Alternate Clock Selection bit⁽¹⁾

1 = Input Capture modules use an alternative Timer pair as their timebase clock

0 = All Input Capture modules use Timer2/3 as their timebase clock

bit 16 **OCACLK:** Output Compare Alternate Clock Selection bit⁽¹⁾

1 = Output Compare modules use an alternative Timer pair as their timebase clock

0 = All Output Compare modules use Timer2/3 as their timebase clock

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit⁽¹⁾

1 = Peripheral Pin Select is locked. Writes to PPS registers are not allowed

0 = Peripheral Pin Select is not locked. Writes to PPS registers are allowed

bit 12 **PMDLOCK:** Peripheral Module Disable bit⁽¹⁾

1 = Peripheral module is locked. Writes to PMD registers are not allowed

0 = Peripheral module is not locked. Writes to PMD registers are allowed

bit 11 **PGLOCK:** Permission Group Lock bit⁽¹⁾

1 = Permission Group registers are locked. Writes to PG registers are not allowed

0 = Permission Group registers are not locked. Writes to PG registers are allowed

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **USBSEN:** USB Suspend Sleep Enable bit⁽¹⁾

Enables features for USB PHY clock shutdown in Sleep mode.

1 = USB PHY clock is shut down when Sleep mode is active

0 = USB PHY clock continues to run when Sleep is active

bit 7-6 **Unimplemented:** Read as '0'

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions ⁽¹⁾
DO10	VOL	Output Low Voltage I/O Pins 4x Sink Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	0.4	V	$I_{OL} \leq 10 \text{ mA}$, $V_{DD} = 3.3\text{V}$
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA0-RA2, RA4, RA5 RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	0.4	V	$I_{OL} \leq 15 \text{ mA}$, $V_{DD} = 3.3\text{V}$
		Output Low Voltage I/O Pins: 12x Sink Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	0.4	V	$I_{OL} \leq 20 \text{ mA}$, $V_{DD} = 3.3\text{V}$

Note 1: Parameters are characterized, but not tested.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-14: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Comments
D300	VIOFF	Input Offset Voltage	—	± 10	—	mV	AVDD = VDD, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0	—	VDD	V	AVDD = VDD, AVSS = VSS (Note 2)
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	Max VICM = (VDD - 1)V (Note 2)
D303	TRESP	Response Time	—	150	—	ns	AVDD = VDD, AVSS = VSS (Notes 1,2)
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	μs	Comparator module is configured before setting the comparator ON bit (Note 2)
D305	IVREF	Internal Voltage Reference	1.194	1.2	1.206	V	—

Note 1: Response time measured with one comparator input at $(VDD - 1.5)/2$, while the other input transitions from VSS to VDD.

2: These parameters are characterized but not tested.

3: The Comparator module is functional at $V_{BORMIN} < VDD < VDDMIN$, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

TABLE 37-15: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Comments
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	—	—	10	μs	See Note 1
D313	DACREFH	CVREF Input Voltage Reference Range	AVSS	—	AVDD	V	CVRSRC with CVRSS = 0
			VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	$0.625 \times \text{DACREFH}$	V	0 to $0.625 \times \text{DACREFH}$ with $\text{DACREFH}/24$ step size
			$0.25 \times \text{DACREFH}$	—	$0.719 \times \text{DACREFH}$	V	$0.25 \times \text{DACREFH}$ to $0.719 \times \text{DACREFH}$ with $\text{DACREFH}/32$ step size
D315	DACRES	Resolution	—	—	$\text{DACREFH}/24$		CVRCON<CVRR> = 1
			—	—	$\text{DACREFH}/32$		CVRCON<CVRR> = 0
D316	DACACC	Absolute Accuracy ⁽²⁾	—	—	1/4	LSB	$\text{DACREFH}/24$, CVRCON<CVRR> = 1
			—	—	1/2	LSB	$\text{DACREFH}/32$, CVRCON<CVRR> = 0

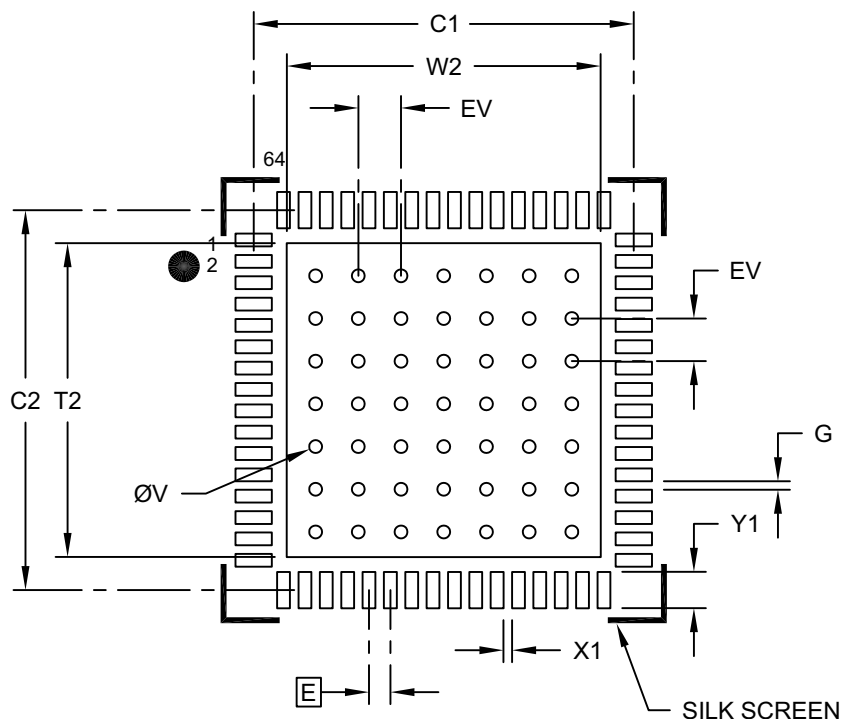
Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

PIC32MZ Embedded Connectivity (EC) Family

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 7.70x7.70mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			7.50
Optional Center Pad Length	T2			7.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.90
Contact Pad to Center Pad (X20)	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2213B

PIC32MZ Embedded Connectivity (EC) Family

A.3 CPU

The CPU in the PIC32MZ family of devices has been changed to the MIPS microAptiv™ MPU architecture. This CPU includes DSP ASE, internal data and instruction L1 caches, and a TLB-based MMU.

Table A-4 summarizes some of the key differences (indicated by **Bold** type) in the internal CPU registers.

TABLE A-4: CPU DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
L1 Data and Instruction Cache and Prefetch Wait States	
On PIC32MX devices, the cache was included in the prefetch module outside the CPU. PREFEN<1:0> (CHECON<5:4>) 11 = Enable predictive prefetch for both cacheable and non-cacheable regions 10 = Enable predictive prefetch for non-cacheable regions only 01 = Enable predictive prefetch for cacheable regions only 00 = Disable predictive prefetch DCSZ<1:0> (CHECON<9:8>) Changing these bits causes all lines to be reinitialized to the "invalid" state. 11 = Enable data caching with a size of 4 lines 10 = Enable data caching with a size of 2 lines 01 = Enable data caching with a size of 1 line 00 = Disable data caching CHECOH (CHECON<16>) 1 = Invalidate all data and instruction lines 0 = Invalidate all data and instruction lines that are not locked	On PIC32MZ devices, the CPU has a separate L1 instruction and data cache in the core. The PREFEN<1:0> bits still enable the prefetch module; however, the K0<2:0> bits in the CP0 registers controls the internal L1 cache for the designated regions. PREFEN<1:0> (PRECON<5:4>) 11 = Enable predictive prefetch for any address 10 = Enable predictive prefetch for CPU instructions and CPU data 01 = Enable predictive prefetch for CPU instructions only 00 = Disable predictive prefetch K0<2:0> (CP0 Reg 16, Select 0) 011 = Cacheable, non-coherent, write-back, write allocate 010 = Uncached 001 = Cacheable, non-coherent, write-through, write allocate 000 = Cacheable, non-coherent, write-through, no write allocate
PFMWS<2:0> (CHECON<2:0>) 111 = Seven Wait states 110 = Six Wait states 101 = Five Wait states 100 = Four Wait states 011 = Three Wait states 010 = Two Wait states (61-80 MHz) 001 = One Wait state (31-60 MHz) 000 = Zero Wait state (0-30 MHz)	The Program Flash Memory read wait state frequency points have changed in PIC32MZ devices. The register for accessing the PFMWS field has changed from CHECON to PRECON. PFMWS<2:0> (PRECON<2:0>) 111 = Seven Wait states • • • 011 = Three Wait states 010 = Two Wait states (133-200 MHz) 001 = One Wait state (66-133 MHz) 000 = Zero Wait states (0-66 MHz) Note: Wait states listed are for ECC enabled.