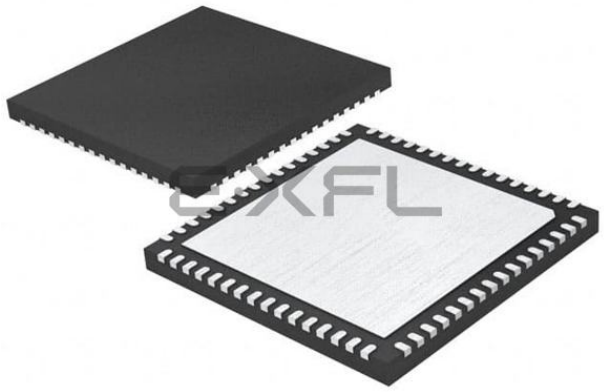
Microchip Technology - PIC32MZ1024ECM064-I/MR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ecm064-i-mr

TABLE 1-18: ALTERNATE ETHERNET MII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
AERXD0	—	18	—	—	I	ST	Alternate Ethernet Receive Data 0
AERXD1	—	19	—	—	I	ST	Alternate Ethernet Receive Data 1
AERXD2	—	28	—	—	I	ST	Alternate Ethernet Receive Data 2
AERXD3	—	29	—	—	I	ST	Alternate Ethernet Receive Data 3
AERXERR	—	1	—	—	I	ST	Alternate Ethernet Receive Error Input
AERXDV	—	12	—	—	I	ST	Alternate Ethernet Receive Data Valid
AERXCLK	—	16	—	—	I	ST	Alternate Ethernet Receive Clock
AETXD0	—	47	—	—	O	—	Alternate Ethernet Transmit Data 0
AETXD1	—	48	—	—	O	—	Alternate Ethernet Transmit Data 1
AETXD2	—	44	—	—	O	—	Alternate Ethernet Transmit Data 2
AETXD3	—	43	—	—	O	—	Alternate Ethernet Transmit Data 3
AETXERR	—	35	—	—	O	—	Alternate Ethernet Transmit Error
AECOL	—	42	—	—	I	ST	Alternate Ethernet Collision Detect
AECRS	—	41	—	—	I	ST	Alternate Ethernet Carrier Sense
AETXCLK	—	66	—	—	I	ST	Alternate Ethernet Transmit Clock
AEMDC	—	70	—	—	O	—	Alternate Ethernet Management Data Clock
AEMDIO	—	71	—	—	I/O	—	Alternate Ethernet Management Data
AETXEN	—	67	—	—	O	—	Alternate Ethernet Transmit Enable

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-19: ALTERNATE ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
AERXD0	43	18	—	—	I	ST	Alternate Ethernet Receive Data 0
AERXD1	46	19	—	—	I	ST	Alternate Ethernet Receive Data 1
AERXERR	51	1	—	—	I	ST	Alternate Ethernet Receive Error Input
AETXD0	57	47	—	—	O	—	Alternate Ethernet Transmit Data 0
AETXD1	56	48	—	—	O	—	Alternate Ethernet Transmit Data 1
AEMDC	30	70	—	—	O	—	Alternate Ethernet Management Data Clock
AEMDIO	49	71	—	—	I/O	—	Alternate Ethernet Management Data
AETXEN	50	67	—	—	O	—	Alternate Ethernet Transmit Enable
AEREFCLK	45	16	—	—	I	ST	Alternate Ethernet Reference Clock
AECRSDV	62	12	—	—	I	ST	Alternate Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

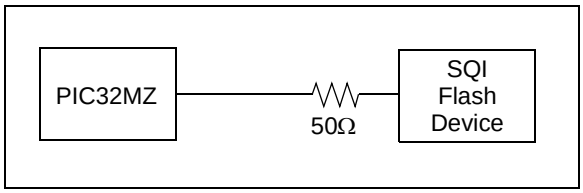
2.9.1 SYSTEM DESIGN

2.9.1.1 Impedance Matching

When selecting parts to place on high-speed buses, particularly the SQI bus, if the impedance of the peripheral device does not match the impedance of the pins on the PIC32MZ EC device to which it is connected, signal reflections could result, thereby degrading the quality of the signal.

If it is not possible to select a product that matches impedance, place a series resistor at the load to create the matching impedance. See Figure 2-4 for an example.

FIGURE 2-4: SERIES RESISTOR



2.9.1.2 PCB Layout Recommendations

The following list contains recommendations that will help ensure the PCB layout will promote the goals previously listed.

- **Component Placement**
  - Place bypass capacitors as close to their component power and ground pins as possible, and place them on the same side of the PCB
  - Devices on the same bus that have larger setup times should be placed closer to the PIC32MZ EC device
- **Power and Ground**
  - Multi-layer PCBs will allow separate power and ground planes
  - Each ground pin should be connected to the ground plane individually
  - Place bypass capacitor vias as close to the pad as possible (preferably inside the pad)
  - If power and ground planes are not used, maximize width for power and ground traces
  - Use low-ESR, surface-mount bypass capacitors
- **Clocks and Oscillators**
  - Place crystals as close as possible to the PIC32MZ EC device OSC/SOSC pins
  - Do not route high-speed signals near the clock or oscillator
  - Avoid via usage and branches in clock lines (SQICLK)
  - Place termination resistors at the end of clock lines
- **Traces**
  - Higher-priority signals should have the shortest traces
  - Match trace lengths for parallel buses (EBIAx, EBIDx, SQIDx)
  - Avoid long run lengths on parallel traces to reduce coupling
  - Make the clock traces as straight as possible
  - Use rounded turns rather than right-angle turns
  - Have traces on different layers intersect on right angles to minimize crosstalk
  - Maximize the distance between traces, preferably no less than three times the trace width
  - Power traces should be as short and as wide as possible
  - High-speed traces should be placed close to the ground plane

TABLE 4-14: SYSTEM BUS TARGET 6 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9820	SBT6ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9824	SBT6ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9828	SBT6ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9830	SBT6ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9838	SBT6ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9840	SBT6REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9850	SBT6RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9858	SBT6WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9860	SBT6REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9870	SBT6RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9878	SBT6WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	U-0
	WR(1)	WREN(1)	WRERR(1)	LVDERR(1)	—	—	—	—
7:0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	SWAP	—	—	—	NVMOP<3:0>			

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit(1)

This bit cannot be cleared and can be set only when WREN = 1 and the unlock sequence has been performed.
1 = Initiate a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit(1)

1 = Enable writes to the WR bit and disables writes to the NVMOP<3:0> bits
0 = Disable writes to WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **SWAP:** Program Flash Bank Swap Control bit

This bit can be modified only when the WREN bit is '0' and the unlock sequence has been performed.
1 = Program Flash Bank 2 is mapped to the lower mapped region and program Flash Bank 1 is mapped to the upper mapped region
0 = Program Flash Bank 1 is mapped to the lower mapped region and program Flash Bank 2 is mapped to the upper mapped region

bit 6-4 **Unimplemented:** Read as '0'

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This operation results in a "no operation" (NOP) when the Dynamic Flash ECC Configuration bits = 00 (FECCCON<1:0> (DVCFG0<9:8>)), which enables ECC at all times. For all other FECCCON<1:0> bit settings, this command will execute, but will not write the ECC bits for the word and can cause DED errors if dynamic Flash ECC is enabled (FECCCON<1:0> = 01). Refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) for information regarding ECC and Flash programming.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 7 uses Shadow Set 0)
0111 = Interrupt with a priority level of 7 uses Shadow Set 7
0110 = Interrupt with a priority level of 7 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 6 uses Shadow Set 0)
0111 = Interrupt with a priority level of 6 uses Shadow Set 7
0110 = Interrupt with a priority level of 6 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 5 uses Shadow Set 0)
0111 = Interrupt with a priority level of 5 uses Shadow Set 7
0110 = Interrupt with a priority level of 5 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 5 uses Shadow Set 1
0000 = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 4 uses Shadow Set 0)
0111 = Interrupt with a priority level of 4 uses Shadow Set 7
0110 = Interrupt with a priority level of 4 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 4 uses Shadow Set 1
0000 = Interrupt with a priority level of 4 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.

REGISTER 11-14: USBFIFOA: USB FIFO ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXFIFOAD<12:8>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXFIFOAD<7:0>							
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXFIFOAD<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXFIFOAD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-16 **RXFIFOAD<12:0>:** Receive Endpoint FIFO Address bits

Start address of the endpoint FIFO in units of 8 bytes as follows:

1111111111111 = 0xFFF8
•
•
•
0000000000010 = 0x0010
0000000000001 = 0x0008
0000000000000 = 0x0000

bit 15-13 **Unimplemented:** Read as '0'

bit 12-0 **TXFIFOAD<12:0>:** Transmit Endpoint FIFO Address bits

Start address of the endpoint FIFO in units of 8 bytes as follows:

1111111111111 = 0xFFF8
•
•
•
0000000000010 = 0x0010
0000000000001 = 0x0008
0000000000000 = 0x0000

TABLE 12-19: PORTJ REGISTER MAP FOR 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	ANSELJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ANSJ11	—	ANSJ9	ANSJ8	—	—	—	—	—	—	—	—	0B00
0810	TRISJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISJ15	TRISJ14	TRISJ13	TRISJ12	TRISJ11	TRISJ10	TRISJ9	TRISJ8	TRISJ7	TRISJ6	TRISJ5	TRISJ4	TRISJ3	TRISJ2	TRISJ1	TRISJ0	FFFF
0820	PORTJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RJ15	RJ14	RJ13	RJ12	RJ11	RJ10	RJ9	RJ8	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	xxxx
0830	LATJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATJ15	LATJ14	LATJ13	LATJ12	LATJ11	LATJ10	LATJ9	LATJ8	LATJ7	LATJ6	LATJ5	LATJ4	LATJ3	LATJ2	LATJ1	LATJ0	xxxx
0840	ODCJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCJ15	ODCJ14	ODCJ13	ODCJ12	ODCJ11	ODCJ10	ODCJ9	ODCJ18	ODCJ7	ODCJ6	ODCJ5	ODCJ4	ODCJ3	ODCJ2	ODCJ1	ODCJ0	0000
0850	CNPUJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUJ15	CNPUJ14	CNPUJ13	CNPUJ12	CNPUJ11	CNPUJ10	CNPUJ9	CNPUJ8	CNPUJ7	CNPUJ6	CNPUJ5	CNPUJ4	CNPUJ3	CNPUJ2	CNPUJ1	CNPUJ0	0000
0860	CNPDJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDJ15	CNPDJ14	CNPDJ13	CNPDJ12	CNPDJ11	CNPDJ10	CNPDJ9	CNPDJ8	CNPDJ7	CNPDJ6	CNPDJ5	CNPDJ4	CNPDJ3	CNPDJ2	CNPDJ1	CNPDJ0	0000
0870	CNCONJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0880	CNENJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEJ15	CNIEJ14	CNIEJ13	CNIEJ12	CNIEJ11	CNIEJ10	CNIEJ9	CNIEJ8	CNIEJ7	CNIEJ6	CNIEJ5	CNIEJ4	CNIEJ3	CNIEJ2	CNIEJ1	CNIEJ0	0000
0890	CNSTATJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATJ15	CN STATJ14	CN STATJ13	CN STATJ12	CN STATJ11	CN STATJ10	CN STATJ9	CN STATJ8	CN STATJ7	CN STATJ6	CN STATJ5	CN STATJ4	CN STATJ3	CN STATJ2	CN STATJ1	CN STATJ0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

25.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are key features of the RTCC module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

FIGURE 25-1: RTCC BLOCK DIAGRAM

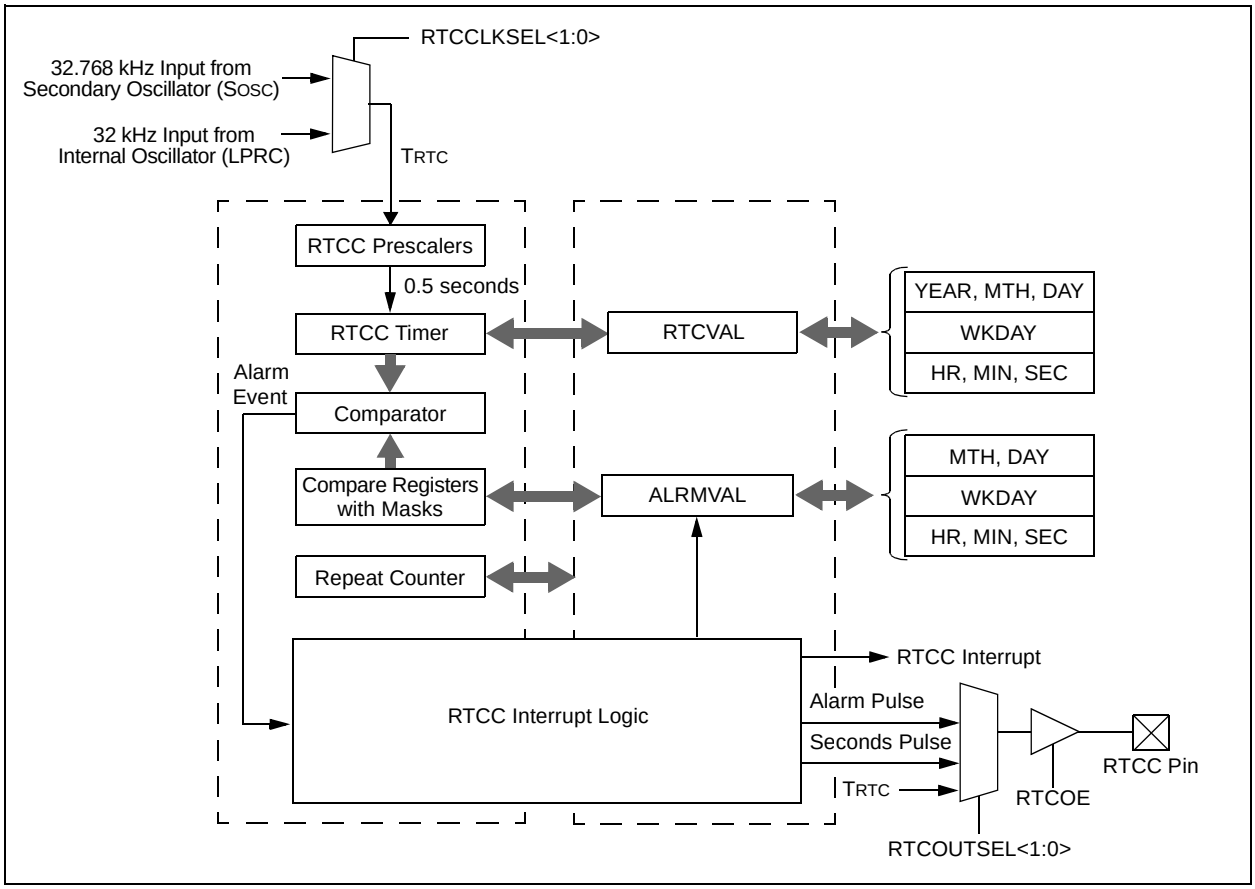


TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B0B8	AD1DATA0	31:16	ADC Output Register 0 <31:16>																0000
		15:0	ADC Output Register 0 <15:0>																0000
B0BC	AD1DATA1	31:16	ADC Output Register 1 <31:16>																0000
		15:0	ADC Output Register 1 <15:0>																0000
B0C0	AD1DATA2	31:16	ADC Output Register 2 <31:16>																0000
		15:0	ADC Output Register 2 <15:0>																0000
B0C4	AD1DATA3	31:16	ADC Output Register 3 <31:16>																0000
		15:0	ADC Output Register 3 <15:0>																0000
B0C8	AD1DATA4	31:16	ADC Output Register 4 <31:16>																0000
		15:0	ADC Output Register 4 <15:0>																0000
B0CC	AD1DATA5	31:16	ADC Output Register 5 <31:16>																0000
		15:0	ADC Output Register <15:0>																0000
B0D0	AD1DATA6	31:16	ADC Output Register 6 <31:16>																0000
		15:0	ADC Output Register 6 <15:0>																0000
B0D4	AD1DATA7	31:16	ADC Output Register 7 <31:16>																0000
		15:0	ADC Output Register 7 <15:0>																0000
B0D8	AD1DATA8	31:16	ADC Output Register 8 <31:16>																0000
		15:0	ADC Output Register 8 <15:0>																0000
B0DC	AD1DATA9	31:16	ADC Output Register 9 <31:16>																0000
		15:0	ADC Output Register 9 <15:0>																0000
B0E0	AD1DATA10	31:16	ADC Output Register 10 <31:16>																0000
		15:0	ADC Output Register 10 <15:0>																0000
B0E4	AD1DATA11	31:16	ADC Output Register 11 <31:16>																0000
		15:0	ADC Output Register 11 <15:0>																0000
B0E8	AD1DATA12	31:16	ADC Output Register 12 <31:16>																0000
		15:0	ADC Output Register 12 <15:0>																0000
B0EC	AD1DATA13	31:16	ADC Output Register 13 <31:16>																0000
		15:0	ADC Output Register 13 <15:0>																0000
B0F0	AD1DATA14	31:16	ADC Output Register 14 <31:16>																0000
		15:0	ADC Output Register 14 <15:0>																0000
B0F4	AD1DATA15	31:16	ADC Output Register 15 <31:16>																0000
		15:0	ADC Output Register 15 <15:0>																0000
B0F8	AD1DATA16	31:16	ADC Output Register 16 <31:16>																0000
		15:0	ADC Output Register 16 <15:0>																0000
B0FC	AD1DATA17	31:16	ADC Output Register 17 <31:16>																0000
		15:0	ADC Output Register 17<15:0>																0000
B100	AD1DATA18	31:16	ADC Output Register 18 <31:16>																0000
		15:0	ADC Output Register18 <15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 28-4: AD1IMOD: ADC1 INPUT MODE CONTROL REGISTER (CONTINUED)

bit 11-10 **SH5MOD<1:0>:** Input Configuration for S&H 5 (SH5) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 9-8 **SH4MOD<1:0>:** Input Configuration for S&H 4 (SH4) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 7-6 **SH3MOD<1:0>:** Input Configuration for S&H 3 (SH3) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 5-4 **SH2MOD<1:0>:** Input Configuration for S&H 2 (SH2) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 3-2 **SH1MOD<1:0>:** Input Configuration for S&H 1 (SH1) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 1-0 **SH0MOD<1:0>:** Input Configuration for S&H 0 (SH0) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

Note 1: Alternate inputs are only available for Class 1 Inputs.
2: When an alternate input is selected (SHxALT<1:0> ≠ 0), the data, status, and control registers for the default Class 1 input are still used. Selecting an alternate input changes the physical input source only.

REGISTER 28-16: AD1TRG2: ADC1 INPUT CONVERT CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC7<4:0>(1)				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC6<4:0>(1)				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC5<4:0>(1)				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC4<4:0>(1)				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC7<4:0>:** Trigger Source for Conversion of Analog Channel AN7 Select bits(1)

11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 COUT(2)
01011 = Comparator 1 COUT(2)
01010 = OCMP5(2)
01001 = OCMP3(2)
01000 = OCMP1(2)
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0
00011 = STRIG(3)
00010 = Reserved
00001 = Global software trigger (GSWTRG)
00000 = No trigger

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC6<4:0>:** Trigger Source for Conversion of Analog Channel AN6 Select bits(1)

See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC5<4:0>:** Trigger Source for Conversion of Analog Channel AN5 Select bits(1)

See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC4<4:0>:** Trigger Source for Conversion of Analog Channel AN4 Select bits(1)

See bits 28-24 for bit value definitions.

Note 1: If the same trigger source is used for multiple ANx channels, the trigger source must wait until the hold time for all channels has completed (due to the last trigger) and the sample time for all ANx channels is satisfied before issuing the next trigger. This condition can cause hole insertions into the ADC pipeline and affect overall ADC throughput.

2: The rising edge of the associated module output signal triggers the conversion. Refer to the block diagram of the specific module for more information.

3: Using STRIG as the trigger source specifies this input to use the Scan Trigger source for its trigger. The STRGSRC<4:0> bits (AD1CON1<26:22>), as well as the appropriate CSSx bit(s) in the AD1CSS1 and AD1CSS2 registers must be set for proper scan operation.

REGISTER 29-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

bit 7 **RXDONE:** Receive Done Interrupt bit(2)

1 = RX packet was successfully received
0 = No interrupt pending

This bit is set whenever an RX packet is successfully received. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 6 **PKTPEND:** Packet Pending Interrupt bit(2)

1 = RX packet pending in memory
0 = RX packet is not pending in memory

This bit is set when the BUFCNT counter has a value other than '0'. It is cleared by either a Reset or by writing the BUFCDEC bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 5 **RXACT:** Receive Activity Interrupt bit(2)

1 = RX packet data was successfully received
0 = No interrupt pending

This bit is set whenever RX packet data is stored in the RXBM FIFO. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONE:** Transmit Done Interrupt bit(1)

1 = TX packet was successfully sent
0 = No interrupt pending

This bit is set when the currently transmitted TX packet completes transmission, and the Transmit Status Vector is loaded into the first descriptor used for the packet. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 2 **TXABORT:** Transmit Abort Condition Interrupt bit(1)

1 = TX abort condition occurred on the last TX packet
0 = No interrupt pending

This bit is set when the MAC aborts the transmission of a TX packet for one of the following reasons:

- Jumbo TX packet abort
- Underrun abort
- Excessive defer abort
- Late collision abort
- Excessive collisions abort

This bit is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 1 **RXBUFNA:** Receive Buffer Not Available Interrupt bit(2)

1 = RX Buffer Descriptor Not Available condition has occurred
0 = No interrupt pending

This bit is set by a RX Buffer Descriptor Overrun condition. It is cleared by either a Reset or a CPU write of a '1' to the CLR register.

bit 0 **RXOVFLW:** Receive FIFO Over Flow Error bit(2)

1 = RX FIFO Overflow Error condition has occurred
0 = No interrupt pending

RXOVFLW is set by the RXBM Logic for an RX FIFO Overflow condition. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

Note 1: This bit is only used for TX operations.
2: This bit is only used for RX operations.

Note:	It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 30-34: EMAC1MWTD: ETHERNET CONTROLLER MAC MII MANAGEMENT WRITE DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MWTD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MWTD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MWTD<15:0>:** MII Management Write Data bits

When written, a MII Management write cycle is performed using the 16-bit data and the preconfigured PHY and Register addresses from the EMAC1MADR register.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 30-35: EMAC1MRDD: ETHERNET CONTROLLER MAC MII MANAGEMENT READ DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MRDD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MRDD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MRDD<15:0>:** MII Management Read Data bits

Following a MII Management Read Cycle, the 16-bit data can be read from this location.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 30-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR6<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR5<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits
These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits
These bits hold the fifth transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

TABLE 33-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS(1) (CONTINUED)

Peripheral	PMDx bit Name	Register Name and Bit Location
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
UART6	U6MD	PMD5<5>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
SPI3	SPI3MD	PMD5<10>
SPI4	SPI4MD	PMD5<11>
SPI5	SPI5MD	PMD5<12>
SPI6	SPI6MD	PMD5<13>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
I2C3	I2C3MD	PMD5<18>
I2C4	I2C4MD	PMD5<19>
I2C5	I2C5MD	PMD5<20>
USB(2)	USBMD	PMD5<24>
CAN1	CAN1MD	PMD5<28>
CAN2	CAN2MD	PMD5<29>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output 1	REFO1MD	PMD6<8>
Reference Clock Output 2	REFO2MD	PMD6<9>
Reference Clock Output 3	REFO3MD	PMD6<10>
Reference Clock Output 4	REFO4MD	PMD6<11>
PMP	PMPMD	PMD6<16>
EBI	EBIMD	PMD6<17>
SQI1	SQI1MD	PMD6<23>
Ethernet	ETHMD	PMD6<28>
DMA	DMAMD	PMD7<4>
Random Number Generator	RNGMD	PMD7<20>
Crypto	CRYPTMD	PMD7<22>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MZ EC Family Features"** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

REGISTER 34-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 3 **Reserved:** Write as '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

FIGURE 38-5: VOH – 12x DRIVER PINS

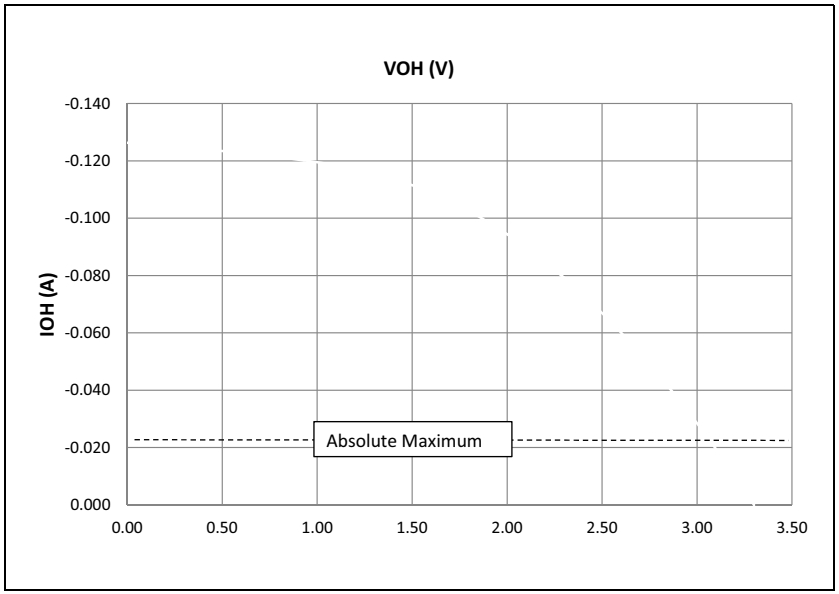


FIGURE 38-6: VOL – 12x DRIVER PINS

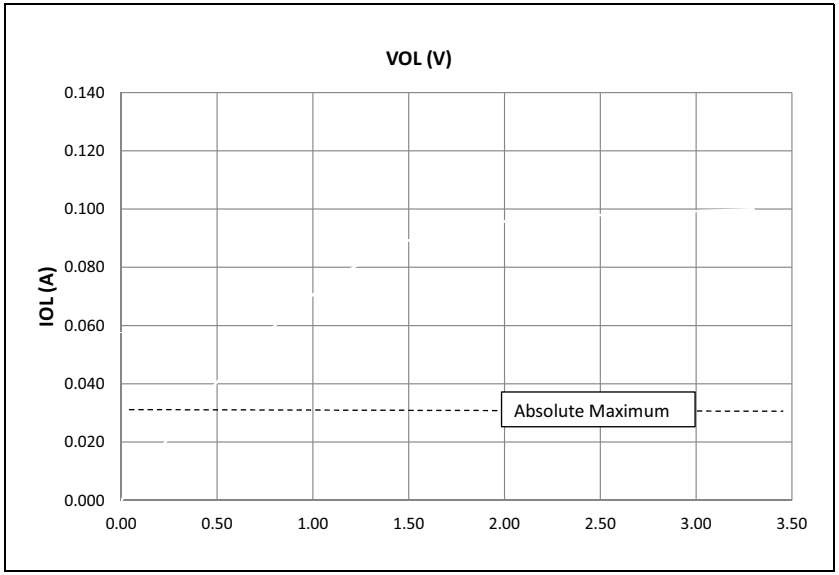
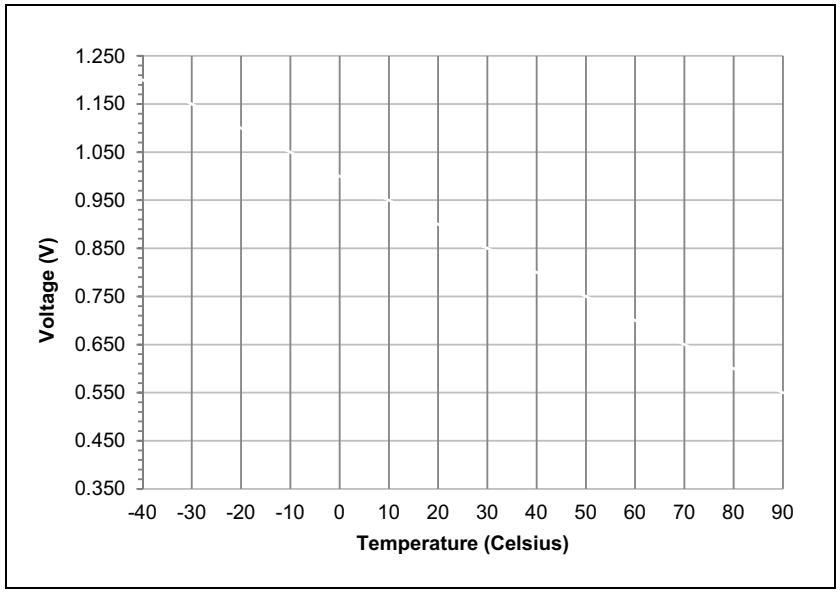


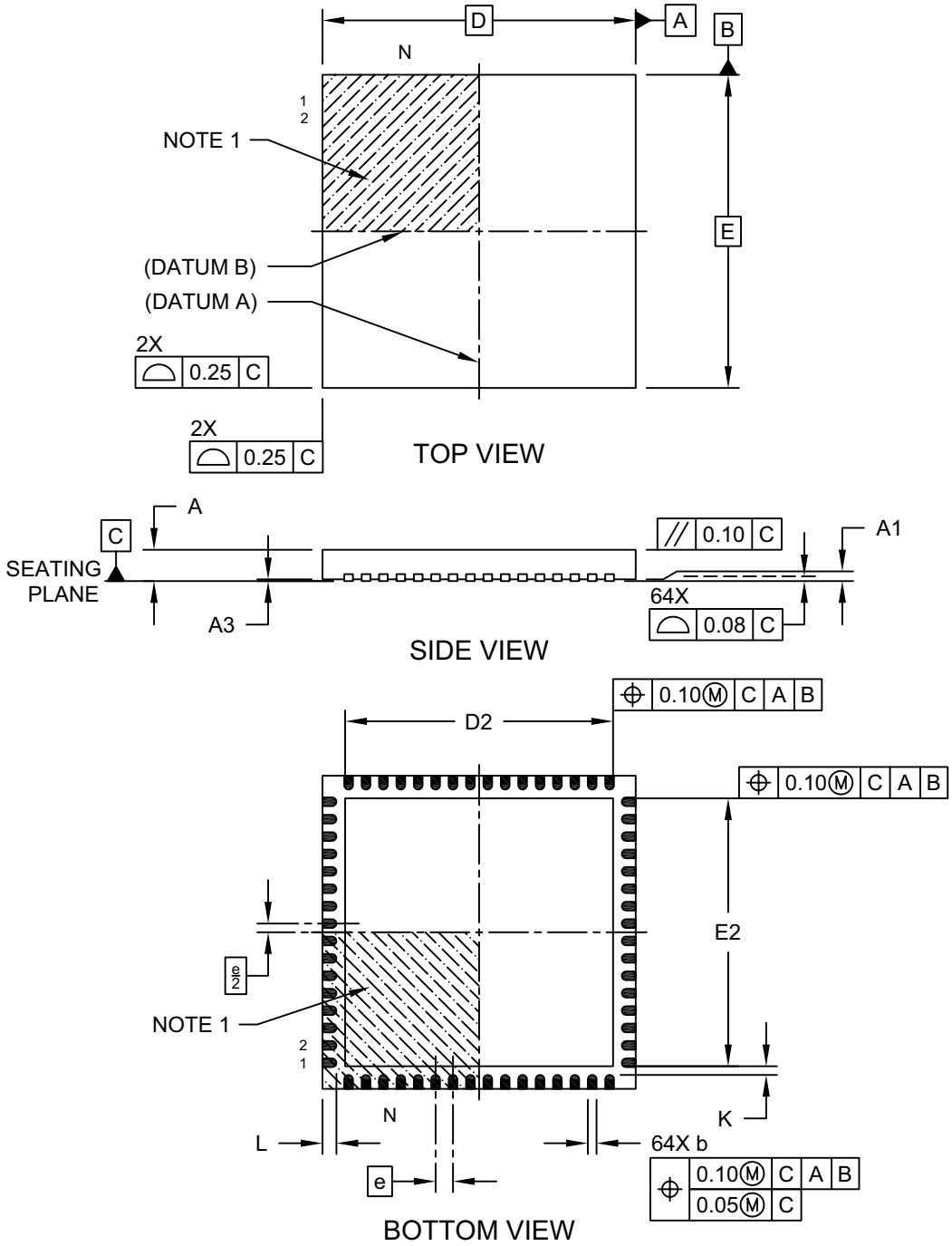
FIGURE 38-7: TYPICAL TEMPERATURE SENSOR VOLTAGE



39.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.70 x 7.70 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-213B Sheet 1 of 2