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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ecm100-i-pt

TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits															All Reset															
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0														
FF40	ABF1DEVCFG3	31:0	Note: See Table 34-2 for the bit descriptions.															xxxx															
FF44	ABF1DEVCFG2	31:0																xxxx															
FF48	ABF1DEVCFG1	31:0																xxxx															
FF4C	ABF1DEVCFG0	31:0																xxxx															
FF50	ABF1DEVCP3	31:0																xxxx															
FF54	ABF1DEVCP2	31:0																xxxx															
FF58	ABF1DEVCP1	31:0																xxxx															
FF5C	ABF1DEVCP0	31:0																xxxx															
FF60	ABF1DEVSIGN3	31:0																xxxx															
FF64	ABF1DEVSIGN2	31:0																xxxx															
FF68	ABF1DEVSIGN1	31:0																xxxx															
FF6C	ABF1DEVSIGN0	31:0																xxxx															
FF70	ABF1SEQ3	31:16																—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0																—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF74	ABF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx															
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx															
FF78	ABF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx															
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx															
FF7C	ABF1SEQ0	31:16	CSEQ<15:0>															xxxx															
		15:0	TSEQ<15:0>															xxxx															
FFC0	BF1DEVCFG3	31:0	Note: See Table 34-1 for the bit descriptions.															xxxx															
FFC4	BF1DEVCFG2	31:0																xxxx															
FFC8	BF1DEVCFG1	31:0																xxxx															
FFCC	BF1DEVCFG0	31:0																xxxx															
FFD0	BF1DEVCP3	31:0																xxxx															
FFD4	BF1DEVCP2	31:0																xxxx															
FFD8	BF1DEVCP1	31:0																xxxx															
FFDC	BF1DEVCP0	31:0																xxxx															
FFE0	BF1DEVSIGN3	31:0																xxxx															
FFE4	BF1DEVSIGN2	31:0																xxxx															
FFE8	BF1DEVSIGN1	31:0																xxxx															
FFEC	BF1DEVSIGN0	31:0																xxxx															
FFF0	BF1SEQ3	31:16																—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0																—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFF4	BF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx															
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx															
FFF8	BF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx															
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx															
FFFC	BF1SEQ0	31:16	CSEQ<15:0>															xxxx															
		15:0	TSEQ<15:0>															xxxx															

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
07CC	OFF163	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07D0	OFF164	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07D4	OFF165	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07D8	OFF166	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07DC	OFF167	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07E4	OFF169	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07E8	OFF170	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07EC	OFF171	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07F0	OFF172	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07F4	OFF173	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07F8	OFF174	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
07FC	OFF175	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0800	OFF176 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0804	OFF177 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

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REGISTER 8-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	PLLIDIV<2:0>						
7:0	R/W-y	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	PLLICK	—	—	—	—	PLLRANGE<2:0>		

Legend:	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits

- 111 = Reserved
- 110 = Reserved
- 101 = PLL Divide by 32
- 100 = PLL Divide by 16
- 011 = PLL Divide by 8
- 010 = PLL Divide by 4
- 001 = PLL Divide by 2
- 000 = Reserved

The default setting is specified by the FPLLODIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 “Special Features”** for information.

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits

- 1111111 = Multiply by 128
- 1111110 = Multiply by 127
- 1111101 = Multiply by 126
- 1111100 = Multiply by 125
-
-
-
- 0000000 = Multiply by 1

The default setting is specified by the FPLLMULT<6:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 “Special Features”** for information.

bit 15-11 **Unimplemented:** Read as '0'

- Note 1:** Writes to this register require an unlock sequence. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.
- 2:** Writes to this register are not allowed if the SPLLC is selected as a clock source (COSC<2:0> = 001).

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
1170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>																0000	
1180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000	
1190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000	
11A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000	
11B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000	
11C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCPTR<15:0>																0000	
11D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHPDAT<15:0>																0000	
11E0	DCH2CON	31:16	CHPIGN<7:0>																0000	
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	0000
11F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	—	CHAIRQ<7:0>						00FF		
		15:0	CHSIRQ<7:0>										CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—
1200	DCH2INT	31:16	—	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1210	DCH2SSA	31:16	CHSSA<31:0>																0000	
		15:0	CHSSA<31:0>																0000	
1220	DCH2DSA	31:16	CHDSA<31:0>																0000	
		15:0	CHDSA<31:0>																0000	
1230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSSIZ<15:0>																0000	
1240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDSIZ<15:0>																0000	
1250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHSPTR<15:0>																0000	
1260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHDPTR<15:0>																0000	
1270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	CHCSIZ<15:0>																0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

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REGISTER 11-4: USBCSR3: USB CONTROL STATUS REGISTER 3 (CONTINUED)

bit 19-16 **ENDPOINT<3:0>**: Endpoint Registers Select bits

1111 = Reserved

-
-
-

1000 = Reserved

0111 = Endpoint 7

-
-
-

0000 = Endpoint 0

These bits select which endpoint registers are accessed through addresses 3010-301F.

bit 15-11 **Unimplemented**: Read as '0'

bit 10-0 **RFRMNUM<10:0>**: Last Received Frame Number bits

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 19-16 **TXFIFOSZ<3:0>**: TX Endpoint FIFO packet size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved

-
-
-

1010 = Reserved

1001 = 4096 bytes

1000 = 2048 bytes

0111 = 1024 bytes

0110 = 512 bytes

0101 = 256 bytes

0100 = 128 bytes

0011 = 64 bytes

0010 = 32 bytes

0001 = 16 bytes

0000 = 8 bytes

bit 15-10 **Unimplemented**: Read as '0'

bit 9 **TXEDMA**: TX Endpoint DMA Assertion Control bit

1 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.

0 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 8 **RXEDMA**: RX Endpoint DMA Assertion Control bit

1 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.

0 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 7 **BDEV**: USB Device Type bit

1 = USB is operating as a 'B' device

0 = USB is operating as an 'A' device

bit 6 **FSDEV**: Full-Speed/Hi-Speed device detection bit (*Host mode*)

1 = A Full-Speed or Hi-Speed device has been detected being connected to the port

0 = No Full-Speed or Hi-Speed device detected

bit 5 **LSDEV**: Low-Speed Device Detection bit (*Host mode*)

1 = A Low-Speed device has been detected being connected to the port

0 = No Low-Speed device detected

bit 4-3 **VBUS<1:0>**: VBUS Level Detection bits

11 = Above VBUS Valid

10 = Above AValid, below VBUS Valid

01 = Above Session End, below AValid

00 = Below Session End

bit 2 **HOSTMODE**: Host Mode bit

1 = USB module is acting as a Host

0 = USB module is not acting as a Host

bit 1 **HOSTREQ**: Host Request Control bit

'B' device only:

1 = USB module initiates the Host Negotiation when Suspend mode is entered. This bit is cleared when Host Negotiation is completed.

0 = Host Negotiation is not taking place

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-15: USBHWVER: USB HARDWARE VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-0
	RC	VERMAJOR<4:0>					VERMINOR<9:8>	
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERMINOR<7:0>							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RC:** Release Candidate bit

1 = USB module was created using a release candidate

0 = USB module was created using a full release

bit 14-10 **VERMAJOR<4:0>:** USB Module Major Version number bits

This read-only number is the Major version number for the USB module.

bit 9-0 **VERMINOR<9:0>:** USB Module Minor Version number bits

This read-only number is the Minor version number for the USB module.

TABLE 12-21: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
1444	IC4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC4R<3:0>			
1448	IC5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC5R<3:0>			
144C	IC6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC6R<3:0>			
1450	IC7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC7R<3:0>			
1454	IC8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC8R<3:0>			
1458	IC9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC9R<3:0>			
1460	OCFAR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	OCFAR<3:0>			
1468	U1RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1RXR<3:0>			
146C	U1CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1CTSR<3:0>			
1470	U2RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2RXR<3:0>			
1474	U2CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2CTSR<3:0>			
1478	U3RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U3RXR<3:0>			
147C	U3CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U3CTSR<3:0>			
1480	U4RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U4RXR<3:0>			
1484	U4CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U4CTSR<3:0>			

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
 2: This register is not available on devices without a CAN module.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 20-12: SQI1STAT1: SQI STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TXFIFOFREE<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXFIFOCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **TXFIFOFREE<7:0>**: Transmit FIFO Available Word Space bits

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXFIFOCNT<7:0>**: Number of words of read data in the FIFO

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 20-20: SQ1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLN<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCURBUFLN<7:0>:** Current DMA Receive Buffer Length Status bits
These bits provide the length of the current DMA receive buffer.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 21-2: I2CxSTAT: I²C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R-0, HS, HC ACKSTAT	R-0, HS, HC TRSTAT	R/C-0, HS, HC ACKTIM	U-0 —	U-0 —	R/C-0, HS BCL	R-0, HS, HC GCSTAT	R-0, HS, HC ADD10
	R/C-0, HS IWCOL	R/C-0, HS I2COV	R-0, HS, HC D_A	R/C-0, HS, HC P	R/C-0, HS, HC S	R-0, HS, HC R_W	R-0, HS, HC RBF	R-0, HS, HC TBF

Legend:	HS = Hardware Set	HC = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I²C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (Valid in I²C Slave mode only)
1 = I²C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>**: Propagation Time Segment bits⁽⁴⁾

111 = Length is 8 x T_Q

-
-
-

000 = Length is 1 x T_Q

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits⁽³⁾

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

111111 = T_Q = (2 x 64)/TPBCLK5

111110 = T_Q = (2 x 63)/TPBCLK5

-
-
-

000001 = T_Q = (2 x 2)/TPBCLK5

000000 = T_Q = (2 x 1)/TPBCLK5

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

2: 3 Time bit sampling is not allowed for BRP < 2.

3: SJW ≤ SEG2PH.

4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 29-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)

- bit 15 **FLTEN5**: Filter 17 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 14-13 **MSEL5<1:0>**: Filter 5 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL5<4:0>**: FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN4**: Filter 4 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 6-5 **MSEL4<1:0>**: Filter 4 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL4<4:0>**: FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 30-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<7:0>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-24 **PMM<31:24>**: Pattern Match Mask 3 bits
bit 23-16 **PMM<23:16>**: Pattern Match Mask 2 bits
bit 15-8 **PMM<15:8>**: Pattern Match Mask 1 bits
bit 7-0 **PMM<7:0>**: Pattern Match Mask 0 bits

Note 1: This register is only used for RX operations.
Note 2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 30-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<39:32>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-24 **PMM<63:56>**: Pattern Match Mask 7 bits
bit 23-16 **PMM<55:48>**: Pattern Match Mask 6 bits
bit 15-8 **PMM<47:40>**: Pattern Match Mask 5 bits
bit 7-0 **PMM<39:32>**: Pattern Match Mask 4 bits

Note 1: This register is only used for RX operations.
Note 2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

31.1 Comparator Control Registers

TABLE 31-1: COMPARATOR REGISTER MAP

Virtual Address (BF84_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
C000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	—	COUT	EVPOL<1:0>	—	CREF	—	—	—	CCH<1:0>	00C3
C010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	—	COUT	EVPOL<1:0>	—	CREF	—	—	—	CCH<1:0>	00C3
C060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 “CLR, SET, and INV Registers” for more information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 32-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	U-0 —	R/W-0 CVROE	R/W-0 CVRR	R/W-0 CVRSS	R/W-0 CVR<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit

1 = Module is enabled

Setting this bit does not affect other bits in the register.

0 = Module is disabled and does not consume current.

Clearing this bit does not affect the other bits in the register.

bit 14-7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** CVREFOUT Enable bit

1 = Voltage level is output on CVREFOUT pin

0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit

1 = 0 to 0.625 CVRSRC, with CVRSRC/24 step size

0 = 0.25 CVRSRC to 0.719 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit

1 = Comparator voltage reference source, $CVRSRC = (VREF+) - (VREF-)$

0 = Comparator voltage reference source, $CVRSRC = AVDD - AVSS$

bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \leq CVR<3:0> \leq 15$ bits

When CVRR = 1:

$CVREF = (CVR<3:0>/24) \cdot (CVRSRC)$

When CVRR = 0:

$CVREF = 1/4 \cdot (CVRSRC) + (CVR<3:0>/32) \cdot (CVRSRC)$

TABLE 33-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
0040	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	CVRMD	—	—	—	—	—	—	—	—	—	—	—	—	AD1MD	0000
0050	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP2MD	CMP1MD	0000
0060	PMD3	31:16	—	—	—	—	—	—	—	OC9MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000	
		15:0	—	—	—	—	—	—	—	IC9MD	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000	
0070	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	T9MD	T8MD	T7MD	T6MD	T5MD	T4MD	T3MD	T2MD	T1MD	0000	
0080	PMD5	31:16	—	—	CAN2MD	CAN1MD	—	—	—	USBMD	—	—	—	I2C5MD	I2C4MD	I2C3MD	I2C2MD	I2C1MD	0000	
		15:0	—	—	SPI6MD	SPI5MD	SPI4MD	SPI3MD	SPI2MD	SPI1MD	—	—	—	U6MD	U5MD	U4MD	U3MD	U2MD	U1MD	0000
0090	PMD6	31:16	—	—	—	ETHMD	—	—	—	—	SQI1MD	—	—	—	—	—	—	EBIMD	PMPMD	0000
		15:0	—	—	—	—	—	REFO4MD	REFO3MD	REFO2MD	REFO1MD	—	—	—	—	—	—	—	—	RTCCMD
00A0	PMD7	31:16	—	—	—	—	—	—	—	—	—	—	CRYPTMD	—	RNGMD	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	DMAMD	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

PIC32MZ Embedded Connectivity (EC) Family

37.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ EC electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MZ EC devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias.....	-40°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS (Note 3).....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V (Note 3).....	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V (Note 3).....	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	-0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of VSS pin(s)	200 mA
Maximum current into VDD pin(s) (Note 2).....	200 mA
Maximum current sunk/sourced by any 4x I/O pin (Note 4).....	15 mA
Maximum current sunk/sourced by any 8x I/O pin (Note 4).....	25 mA
Maximum current sunk/sourced by any 12x I/O pin (Note 4).....	33 mA
Maximum current sunk by all ports	150 mA
Maximum current sourced by all ports (Note 2).....	150 mA

- Note 1:** Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2:** Maximum allowable current is a function of device maximum power dissipation (see Table 37-2).
- 3:** See the pin name tables (Table 2 through Table 4) for the 5V tolerant pins.
- 4:** Characterized, but not tested. Refer to parameters DO10, DO20, and DO20a for the 4x, 8x, and 12x I/O pin lists.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-26: TIMER2-TIMER9 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial					
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Max.	Units	Conditions
TB10	TtXH	TxCK High Time	Synchronous, with prescaler	$[(12.5 \text{ ns or } 1 \text{ TPBCLK}_3) / N] + 25 \text{ ns}$	—	ns	Must also meet parameter TB15 N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	TtXL	TxCK Low Time	Synchronous, with prescaler	$[(12.5 \text{ ns or } 1 \text{ TPBCLK}_3) / N] + 25 \text{ ns}$	—	ns	
TB15	TtXP	TxCK Input Period	Synchronous, with prescaler	$[(\text{Greater of } [(25 \text{ ns or } 2 \text{ TPBCLK}_3) / N] + 30 \text{ ns})]$	—	ns	VDD > 2.7V
				$[(\text{Greater of } [(25 \text{ ns or } 2 \text{ TPBCLK}_3) / N] + 50 \text{ ns})]$	—	ns	VDD < 2.7V
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPBCLK3	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 37-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS

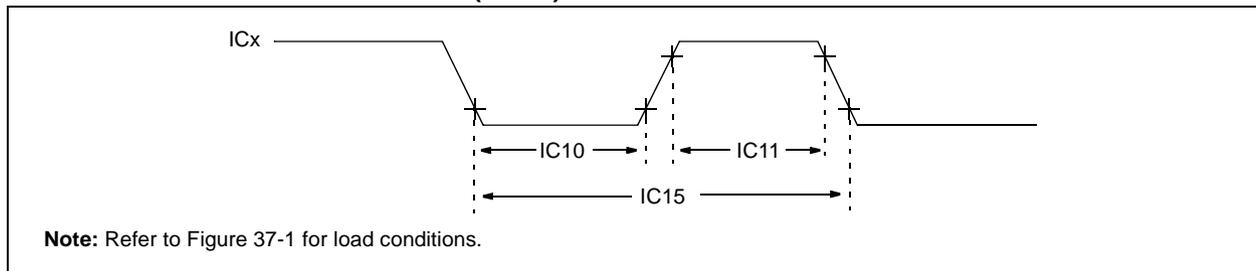


TABLE 37-27: INPUT CAPTURE MODULE TIMING REQUIREMENTS

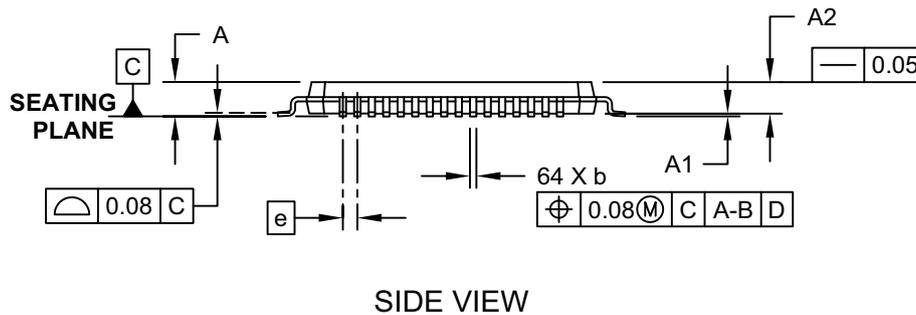
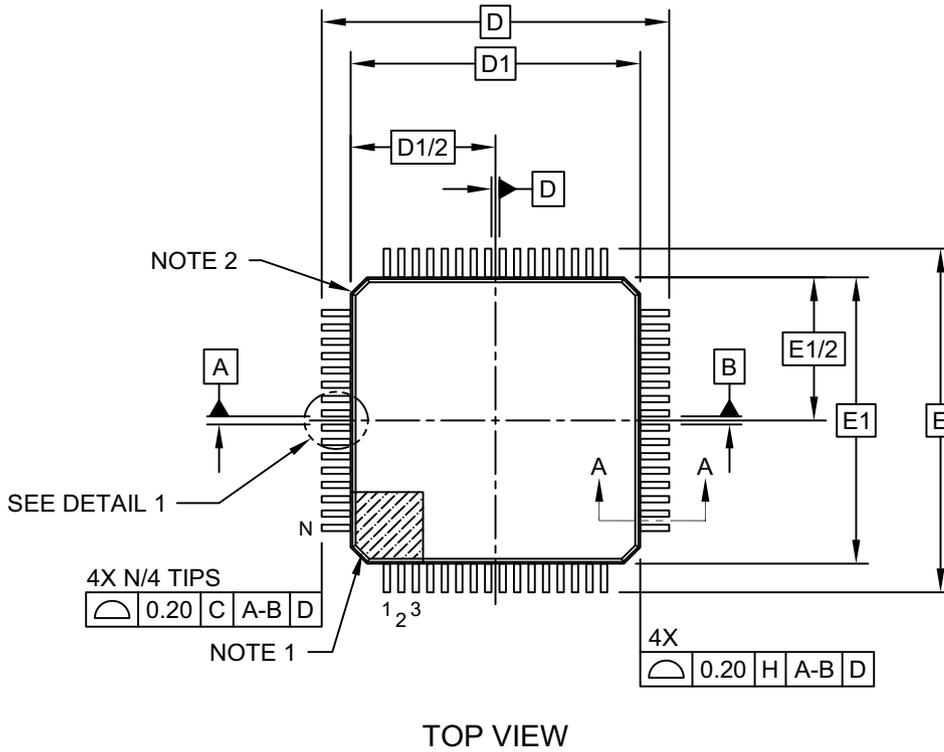
AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial					
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Max.	Units	Conditions
IC10	TcCL	ICx Input Low Time		$[(12.5 \text{ ns or } 1 \text{ TPBCLK}_3) / N] + 25 \text{ ns}$	—	ns	Must also meet parameter IC15. N = prescale value (1, 4, 16)
IC11	TcCH	ICx Input High Time		$[(12.5 \text{ ns or } 1 \text{ TPBCLK}_3) / N] + 25 \text{ ns}$	—	ns	
IC15	TcCP	ICx Input Period		$[(25 \text{ ns or } 2 \text{ TPBCLK}_3) / N] + 50 \text{ ns}$	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

PIC32MZ Embedded Connectivity (EC) Family

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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