Microchip Technology - PIC32MZ1024ECM144-I/PH Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ecm144-i-ph

TABLE 3: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EC(E/F/K)100
PIC32MZ1024EC(G/H/M)100
PIC32MZ1024EC(E/F/K)100
PIC32MZ2048EC(G/H/M)100

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/AERXERR/RG15	36	VSS
2	EBIA5/AN34/PMA5/RA5	37	VDD
3	EBID5/AN17/RPE5/PMD5/RE5	38	TCK/EBIA19/AN29/RA1
4	EBID6/AN16/PMD6/RE6	39	TDI/EBIA18/AN30/RPF13/SCK5/RF13
5	EBID7/AN15/PMD7/RE7	40	TDO/EBIA17/AN31/RPF12/RF12
6	EBIA6/AN22/RPC1/PMA6/RC1	41	EBIA11/AN7/ERXD0/AECRS/PMA11/RB12
7	EBIA12/AN21/RPC2/PMA12/RC2	42	AN8/ERXD1/AECOL/RB13
8	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	43	EBIA1/AN9/ERXD2/AETXD3/RPB14/SCK3/PMA1/RB14
9	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	44	EBIA0/AN10/ERXD3/AETXD2/RPB15/OCFB/PMA0/RB15
10	AN14/C1IND/ECOL/RPG6/SCK2/RG6	45	VSS
11	EBIA4/AN13/C1INC/ECRS/RPG7/SDA4/PMA4/RG7	46	VDD
12	EBIA3/AN12/C2IND/ERXDV/ECRSDV/AERXDV/ AECRSDV/RPG8/SCL4/PMA3/RG8	47	AN32/AETXD0/RPD14/RD14
13	VSS	48	AN33/AETXD1/RPD15/SCK6/RD15
14	VDD	49	OSC1/CLKI/RC12
15	$\overline{\text{MCLR}}$	50	OSC2/CLKO/RC15
16	EBIA2/AN11/C2INC/ERXCLK/EREFCLK/AERXCLK/ AEREFCLK/RPG9/PMA2/RG9	51	VBUS
17	TMS/EBIA16/AN24/RA0	52	VUSB3V3
18	AN25/AERXD0/RPE8/RE8	53	VSS
19	AN26/AERXD1/RPE9/RE9	54	D-
20	AN45/C1INA/RPB5/RB5	55	D+
21	AN4/C1INB/RB4	56	RPF3/USBID/RF3
22	AN3/C2INA/RPB3/RB3	57	EBIRDY3/RPF2/SDA3/RF2
23	AN2/C2INB/RPB2/RB2	58	EBIRDY2/RPF8/SCL3/RF8
24	PGEC1/AN1/RPB1/RB1	59	$\overline{\text{EBICS0}}$/SCL2/RA2
25	PGED1/AN0/RPB0/RB0	60	EBIRDY1/SDA2/RA3
26	PGEC2/AN46/RPB6/RB6	61	EBIA14/PMCS1/PMA14/RA4
27	PGED2/AN47/RPB7/RB7	62	VDD
28	VREF-/CVREF-/AN27/AERXD2/RA9	63	VSS
29	VREF+/CVREF+/AN28/AERXD3/RA10	64	EBIA9/RPF4/SDA5/PMA9/RF4
30	AVDD	65	EBIA8/RPF5/SCL5/PMA8/RF5
31	AVSS	66	AETXCLK/RPA14/SCL1/RA14
32	EBIA10/AN48/RPB8/PMA10/RB8	67	AETXEN/RPA15/SDA1/RA15
33	EBIA7/AN49/RPB9/PMA7/RB9	68	EBIA15/RPD9/PMCS2/PMA15/RD9
34	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	69	RPD10/SCK4/RD10
35	AN6/ERXERR/AETXERR/RB11	70	EMDC/AEMDC/RPD11/RD11

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

1.0 DEVICE OVERVIEW

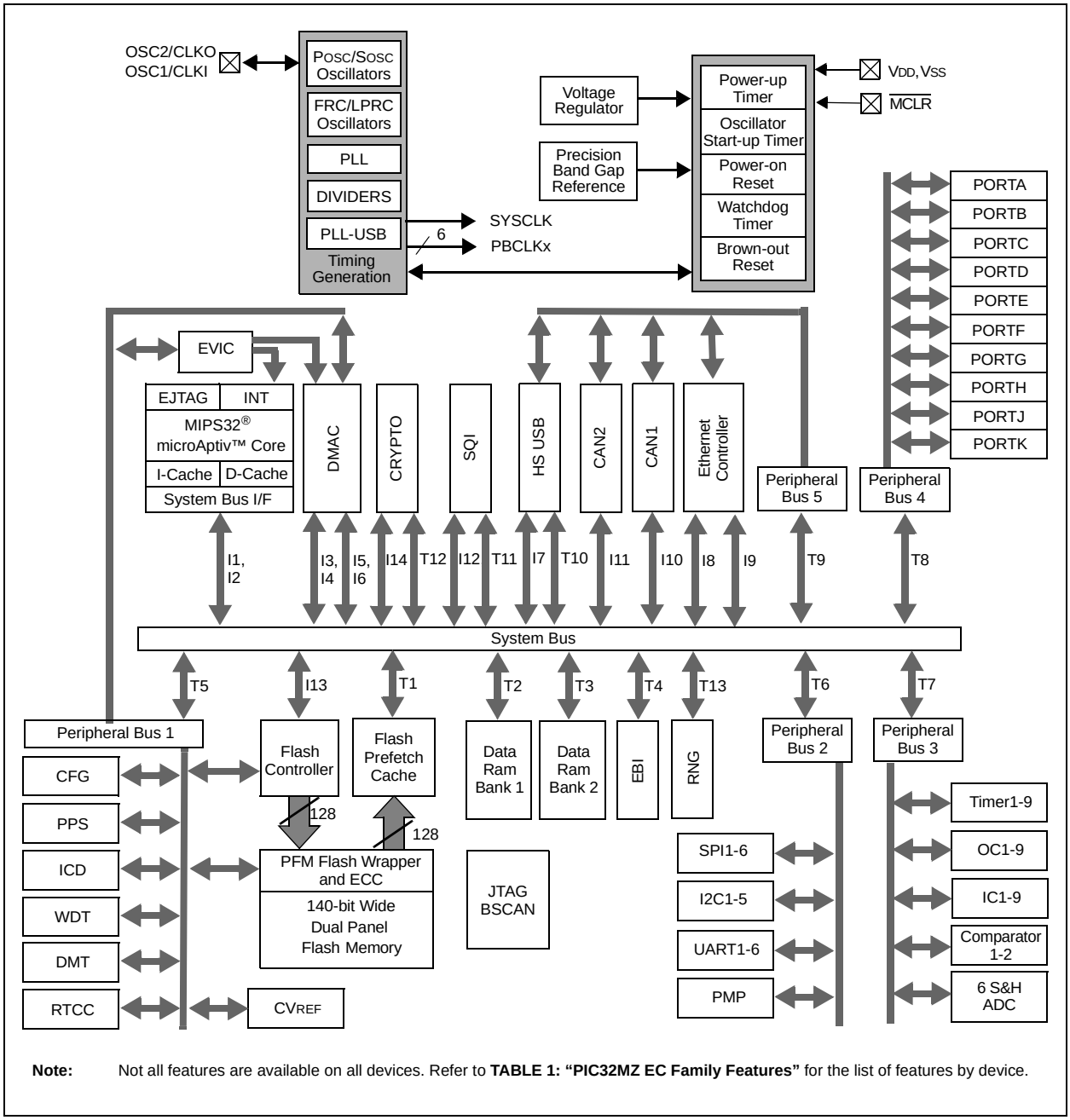
Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents provided in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This data sheet contains device-specific information for PIC32MZ Embedded Connectivity (EC) devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ EC family of devices.

Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 2 through Table 5).

FIGURE 1-1: PIC32MZ EC FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to **TABLE 1: "PIC32MZ EC Family Features"** for the list of features by device.

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Output Compare							
OC1	PPS	PPS	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	PPS	O	—	
OC6	PPS	PPS	PPS	PPS	O	—	
OC7	PPS	PPS	PPS	PPS	O	—	
OC8	PPS	PPS	PPS	PPS	O	—	
OC9	PPS	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	B24	62	I	ST	Output Compare Fault B Input

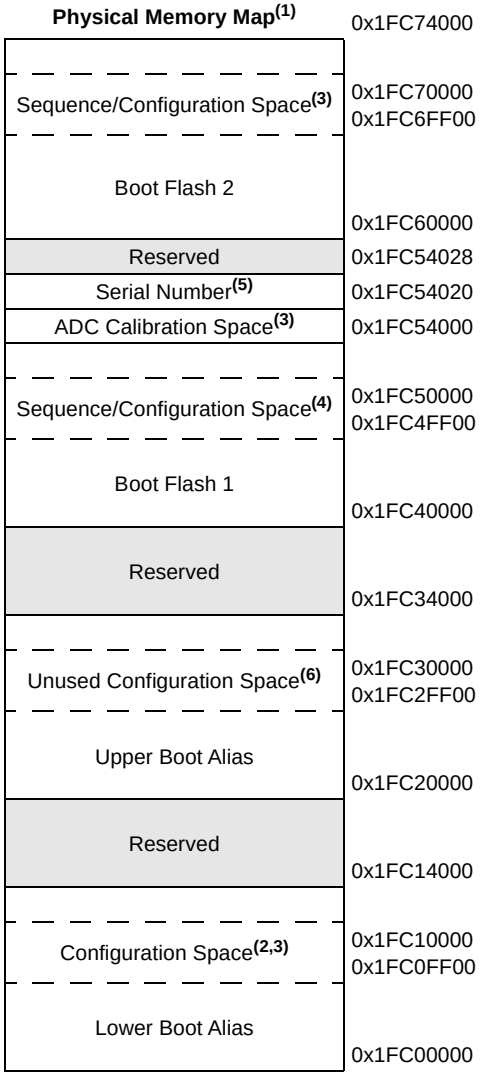
Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
External Interrupts							
INT0	46	71	A48	104	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

FIGURE 4-5: BOOT AND ALIAS MEMORY MAP



Note 1: Memory areas are not shown to scale.

2: Memory locations 0x1FC0FF40 through 0x1FC0FFFC are used to initialize Configuration registers (see **Section 34.0 "Special Features"**).

3: Memory locations 0x1FC54000 through 0x1FC54010 are used to initialize the ADC Calibration registers (see **Section 34.0 "Special Features"**).

4: Refer to**Section 4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

5: Memory locations 0x1FC54020 and 0x1FC54024 contain a unique device serial number (see **Section 34.0 "Special Features"**).

6: This configuration space cannot be used for executing code in the upper boot alias.

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
System Bus(1)	0xBF8F0000	0x0000
RNG	0xBF8E0000	0x6000
Crypto		0x5000
USB		0x3000
SQI1		0x2000
EBI		0x1000
Prefetch		0x0000
Ethernet	0xBF880000	0x2000
CAN1 and CAN2		0x0000
PORTA-PORTK	0xBF860000	0x0000
Comparator 1, 2	0xBF840000	0xC000
ADC1		0xB000
OC1-OC9		0x4000
IC1-IC9		0x2000
Timer1-Timer9		0x0000
PMP	0xBF820000	0xE000
UART1-UART6		0x2000
SPI1-SPI6		0x1000
I2C1-I2C5		0x0000
DMA	0xBF810000	0x1000
Interrupt Controller		0x0000
PPS	0xBF800000	0x1400
Oscillator		0x1200
CVREF		0x0E00
RTCC		0x0C00
Deadman Timer		0x0A00
Watchdog Timer		0x0800
Flash Controller		0x0600
Configuration		0x0000

Note 1: Refer to **4.2 "System Bus Arbitration"** for important legal information.

4.1.1 BOOT FLASH SEQUENCE AND CONFIGURATION SPACES

Sequence space is used to identify which boot Flash is aliased by aliased regions. If the value programmed into the TSEQ<15:0> bits of the BF1SEQ0 word is equal to or greater than the value programmed into the TSEQ<15:0> bits of the BF2SEQ0 word, Boot Flash 1 is aliased by the lower boot alias region, and Boot Flash 2 is aliased by the upper boot alias region. If TSEQ<15:0> bits of BF2SEQ0 is greater than TSEQ<15:0> bits of BF1SEQ0, the opposite is true (see Table 4-2 and Table 4-3 for BFxSEQ0 word memory locations).

The CSEQ<15:0> bits must contain the complement value of the TSEQ<15:0> bits; otherwise, the value of TSEQ<15:0> is considered invalid, and an alternate sequence is used. See **Section 4.1.2 "Alternate Sequence and Configuration Words"** for more information.

Once boot Flash memories are aliased, configuration space located in the lower boot alias region is used as the basis for the Configuration words, DEVSIGN0, DEVCP0, and DEVCFGx (and the associated alternate configuration registers). This means that the boot Flash region to be aliased by lower boot alias region memory must contain configuration values in the appropriate memory locations.

Note:	Do not use word program operation (NVMOP<3:0> = `0001`) when programming data into the sequence and configuration spaces.

4.1.2 ALTERNATE SEQUENCE AND CONFIGURATION WORDS

Every word in the configuration space and sequence space has an associated alternate word (designated by the letter A as the first letter in the name of the word). During device start-up, primary words are read and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and alternate words are used. If uncorrectable ECC errors are found in primary and alternate words, the BCFGFAIL (RCON<26>) flag is set and the default configuration is used.

TABLE 4-21: SYSTEM BUS TARGET 13 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B420	SBT13ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
B424	SBT13ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
B428	SBT13ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
B430	SBT13ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B438	SBT13ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B440	SBT13REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
B450	SBT13RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
B458	SBT13WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	U-0
	WR(1)	WREN(1)	WRERR(1)	LVDERR(1)	—	—	—	—
7:0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	SWAP	—	—	—	NVMOP<3:0>			

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit(1)

This bit cannot be cleared and can be set only when WREN = 1 and the unlock sequence has been performed.
1 = Initiate a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit(1)

1 = Enable writes to the WR bit and disables writes to the NVMOP<3:0> bits
0 = Disable writes to WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **SWAP:** Program Flash Bank Swap Control bit

This bit can be modified only when the WREN bit is '0' and the unlock sequence has been performed.
1 = Program Flash Bank 2 is mapped to the lower mapped region and program Flash Bank 1 is mapped to the upper mapped region
0 = Program Flash Bank 1 is mapped to the lower mapped region and program Flash Bank 2 is mapped to the upper mapped region

bit 6-4 **Unimplemented:** Read as '0'

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This operation results in a "no operation" (NOP) when the Dynamic Flash ECC Configuration bits = 00 (FECCCON<1:0> (DVCFG0<9:8>)), which enables ECC at all times. For all other FECCCON<1:0> bit settings, this command will execute, but will not write the ECC bits for the word and can cause DED errors if dynamic Flash ECC is enabled (FECCCON<1:0> = 01). Refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) for information regarding ECC and Flash programming.

NOTES:

7.3 Interrupt Control Registers

TABLE 7-3: INTERRUPT REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
0010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
0020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
0030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
0040	IFS0	31:16	OC6IF	IC6IF	IC6EIF	T6IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
0050	IFS1	31:16	AD1D4IF	AD1D3IF	AD1D2IF	AD1D1IF	AD1D0IF	—	AD1DF6IF	AD1DF5IF	AD1DF4IF	AD1DF3IF	AD1DF2IF	AD1DF1IF	AD1DC6IF	AD1DC5IF	AD1DC4IF	AD1DC3IF	0000
		15:0	AD1DC2IF	AD1DC1IF	—	AD1IF	OC9IF	IC9IF	IC9EIF	T9IF	OC8IF	IC8IF	IC8EIF	T8IF	OC7IF	IC7IF	IC7EIF	T7IF	0000
0060	IFS2(5)	31:16	AD1D36IF	AD1D35IF	AD1D34IF	AD1D33IF	AD1D32IF	AD1D31IF	AD1D30IF	AD1D29IF	AD1D28IF	AD1D27IF	AD1D26IF	AD1D25IF	AD1D24IF	AD1D23IF	AD1D22IF	AD1D21IF	0000
		15:0	AD1D20IF	AD1D19IF	AD1D18IF	AD1D17IF	AD1D16IF	AD1D15IF	AD1D14IF	AD1D13IF	AD1D12IF	AD1D11IF	AD1D10IF	AD1D9IF	AD1D8IF	AD1D7IF	AD1D6IF	AD1D5IF	0000
0070	IFS3(6)	31:16	CNKIF	CNJIF	CNHIF	CNGIF	CNFIF	CNEIF	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	0000
		15:0	SPI1TXIF	SPI1RXIF	SPI1EIF	—	CRPTIF	SBIF	CFDCIF	CPCIF	AD1D44IF	AD1D43IF	AD1D42IF	AD1D41IF	AD1D40IF	AD1D39IF	AD1D38IF	AD1D37IF	0000
0080	IFS4	31:16	U3TXIF	U3RXIF	U3EIF	SPI3TXIF	SPI3RXIF	SPI3EIF	ETHIF	CAN2IF(3)	CAN1IF(3)	I2C2MIF(2)	I2C2SIF(2)	I2C2BIF(2)	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	0000
		15:0	SPI2RXIF	SPI2EIF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	USBDMAIF	USBIF	CMP2IF	CMP1IF	PMPEIF	PMPIF	0000
0090	IFS5	31:16	—	U6TXIF	U6RXIF	U6EIF	SPI6TX(2)	SPI6RXIF(2)	SPI6IF(2)	I2C5MIF	I2C5SIF	I2C5BIF	U5TXIF	U5RXIF	U5EIF	SPI5TXIF(2)	SPI5RXIF(2)	SPI5EIF(2)	0000
		15:0	I2C4MIF	I2C4SIF	I2C4BIF	U4TXIF	U4RXIF	U4EIF	SQI1IF	PREIF	FCEIF	RTCCIF	SPI4TXIF	SPI4RXIF	SPI4EIF	I2C3MIF	I2C3SIF	I2C3BIF	0000
00C0	IEC0	31:16	OC6IE	IC6IE	IC6EIE	T6IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
00D0	IEC1	31:16	AD1D4IE	AD1D3IE	AD1D2IE	AD1D1IE	AD1D0IE	—	AD1DF6IE	AD1DF5IE	AD1DF4IE	AD1DF3IE	AD1DF2IE	AD1DF1IE	AD1DC6IE	AD1DC5IE	AD1DC4IE	AD1DC3IE	0000
		15:0	AD1DC2IE	AD1DC1IE	—	AD1IE	OC9IE	IC9IE	IC9EIE	T9IE	OC8IE	IC8IE	IC8EIE	T8IE	OC7IE	IC7IE	IC7EIE	T7IE	0000
00E0	IEC2(5)	31:16	AD1D36IE	AD1D35IE	AD1D34IE	AD1D33IE	AD1D32IE	AD1D31IE	AD1D30IE	AD1D29IE	AD1D28IE	AD1D27IE	AD1D26IE	AD1D25IE	AD1D24IE	AD1D23IE	AD1D22IE	AD1D21IE	0000
		15:0	AD1D20IE	AD1D19IE	AD1D18IE	AD1D17IE	AD1D16IE	AD1D15IE	AD1D14IE	AD1D13IE	AD1D12IE	AD1D11IE	AD1D10IE	AD1D9IE	AD1D8IE	AD1D7IE	AD1D6IE	AD1D5IE	0000
00F0	IEC3(6)	31:16	CNKIE	CNJIE	CNHIE	CNGIE	CNFIE	CNEIE	CNDIE	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	0000
		15:0	SPI1TXIE	SPI1RXIE	SPI1EIE	—	CRPTIE	SBIE	CFDCIE	CPCIE	AD1D44IE	AD1D43IE	AD1D42IE	AD1D41IE	AD1D40IE	AD1D39IE	AD1D38IE	AD1D37IE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0660	OFF072	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0664	OFF073	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0668	OFF074	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
066C	OFF075	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0670	OFF076	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0674	OFF077(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0678	OFF078(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
067C	OFF079(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0680	OFF080(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0684	OFF081(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0688	OFF082(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
068C	OFF083(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0690	OFF084(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0694	OFF085(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0698	OFF086(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

11.0 HI-SPEED USB WITH ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 51. "Hi-Speed USB with On-The-Go (OTG)"** (DS60001232), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 embedded host, device, or OTG implementation with a minimum of external components.

The module supports Hi-Speed, Full-Speed, or Low-Speed in any of the operating modes. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the RAM controller, packet encode/decode, UTM synchronization, end-point control, a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

Note: To avoid cache coherency problems on devices with L1 cache, USB buffers must only be allocated or accessed from the KSEG1 segment.

The USB module includes the following features:

- USB Hi-Speed, Full-Speed, and Low-Speed support for host and device
- USB OTG support with one or more Hi-Speed, Full-Speed, or Low-Speed device
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Integrated 8-channel DMA to access system RAM and Flash
- Seven transmit endpoints and seven receive endpoints, in addition to Endpoint 0
- Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) support
- Suspend and resume signaling support
- Dynamic FIFO sizing
- Integrated RAM for the FIFOs, eliminating the need for system RAM for the FIFOs
- Link power management support

Note 1: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

2: If the USB module is used, the Primary Oscillator (POSC) is limited to either 12 MHz or 24 MHz.

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AUTOSET	ISO	MODE	DMAREQEN	FRCDATTG	DMAREQMD	—	—
		—					DATAWEN	DATATGGL
23:16	R/W-0, HS	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0	R/W-0, HS	R/W-0	R/W-0, HC
	INCOMPTX	CLRDT	SENTSTALL	SENDSTALL	FLUSH	UNDERRUN	FIFONE	TXPKTRDY
	NAKTMOUT		RXSTALL	SETUPPKT		ERROR		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					TXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXMAXP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **AUTOSET:** Auto Set Control bit

1 = TXPKTRDY will be automatically set when data of the maximum packet size (value in TXMAXP) is loaded into the TX FIFO. If a packet of less than the maximum packet size is loaded, then TXPKTRDY will have to be set manually.

0 = TXPKTRDY must be set manually for all packet sizes

bit 30 **ISO:** Isochronous TX Endpoint Enable bit (Device mode)

1 = Enables the endpoint for Isochronous transfers

0 = Disables the endpoint for Isochronous transfers and enables it for Bulk or Interrupt transfers.

This bit only has an effect in Device mode. In Host mode, it always returns '0'.

bit 29 **MODE:** Endpoint Direction Control bit

1 = Endpoint is TX

0 = Endpoint is RX

This bit only has any effect where the same endpoint FIFO is used for both TX and RX transactions.

bit 28 **DMAREQEN:** Endpoint DMA Request Enable bit

1 = DMA requests are enabled for this endpoint

0 = DMA requests are disabled for this endpoint

bit 27 **FRCDATTG:** Force Endpoint Data Toggle Control bit

1 = Forces the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.

0 = No forced behavior

bit 26 **DMAREQMD:** Endpoint DMA Request Mode Control bit

1 = DMA Request Mode 1

0 = DMA Request Mode 0

This bit must not be cleared either before or in the same cycle as the above DMAREQEN bit is cleared.

bit 25 **DATAWEN:** Data Toggle Write Enable bit (Host mode)

1 = Enable the current state of the TX Endpoint data toggle (DATATGGL) to be written

0 = Disables writing the DATATGGL bit

bit 24 **DATATGGL:** Data Toggle Control bit (Host mode)

When read, this bit indicates the current state of the TX Endpoint data toggle. If DATAWEN = 1, this bit may be written with the required setting of the data toggle. If DATAWEN = 0, any value written to this bit is ignored.

REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1 (CONTINUED)

bit 16 **LPMXMT:** LPM Transition to the L1 State bit

When in *Device mode*:

1 = USB module will transition to the L1 state upon the receipt of the next LPM transaction. LPMEN must be set to '0b11. Both LPMXMT and LPMEN must be set in the same cycle.

0 = Maintain current state

When LPMXMT and LPMEN are set, the USB module can respond in the following ways:

- If no data is pending (all TX FIFOs are empty), the USB module will respond with an ACK. The bit will self clear and a software interrupt will be generated.
- If data is pending (data resides in at least one TX FIFO), the USB module will respond with a NYET. In this case, the bit will not self clear however a software interrupt will be generated.

When in *Host mode*:

1 = USB module will transmit an LPM transaction. This bit is self clearing, and will be immediately cleared upon receipt of any Token or three time-outs have occurred.

0 = Maintain current state

bit 15-12 **ENDPOINT<3:0>:** LPM Token Packet Endpoint bits

This is the endpoint in the token packet of the LPM transaction.

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **RMTWAK:** Remote Wake-up Enable bit

This bit is applied on a temporary basis only and is only applied to the current suspend state.

1 = Remote wake-up is enabled

0 = Remote wake-up is disabled

bit 7-4 **HIRD<3:0>:** Host Initiated Resume Duration bits

The minimum time the host will drive resume on the bus. The value in this register corresponds to an actual resume time of:

Resume Time = 50 µs + HIRD * 75 µs. The resulting range is 50 µs to 1200 µs.

bit 3-0 **LNKSTATE<3:0>:** Link State bits

This value is provided by the host to the peripheral to indicate what state the peripheral must transition to after the receipt and acceptance of a LPM transaction. The only valid value for this register is '1' for Sleep State (L1). All other values are reserved.

REGISTER 19-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN(1)	—	—	—	AUDMONO(1,2)	—	AUDMOD<1:0>(1,2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit
- 1 = Data from RX FIFO is sign extended
- 0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
- 1 = Frame Error overflow generates error events
- 0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
- 1 = Receive overflow generates error events
- 0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
- 1 = Transmit Underrun Generates Error Events
- 0 = Transmit Underrun Does Not Generates Error Events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
- 1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
- 0 = A ROV is a critical error which stop SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
- 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
- 0 = A TUR is a critical error which stop SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit(1)
- 1 = Audio protocol enabled
- 0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
- 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
- 0 = Audio data is stereo

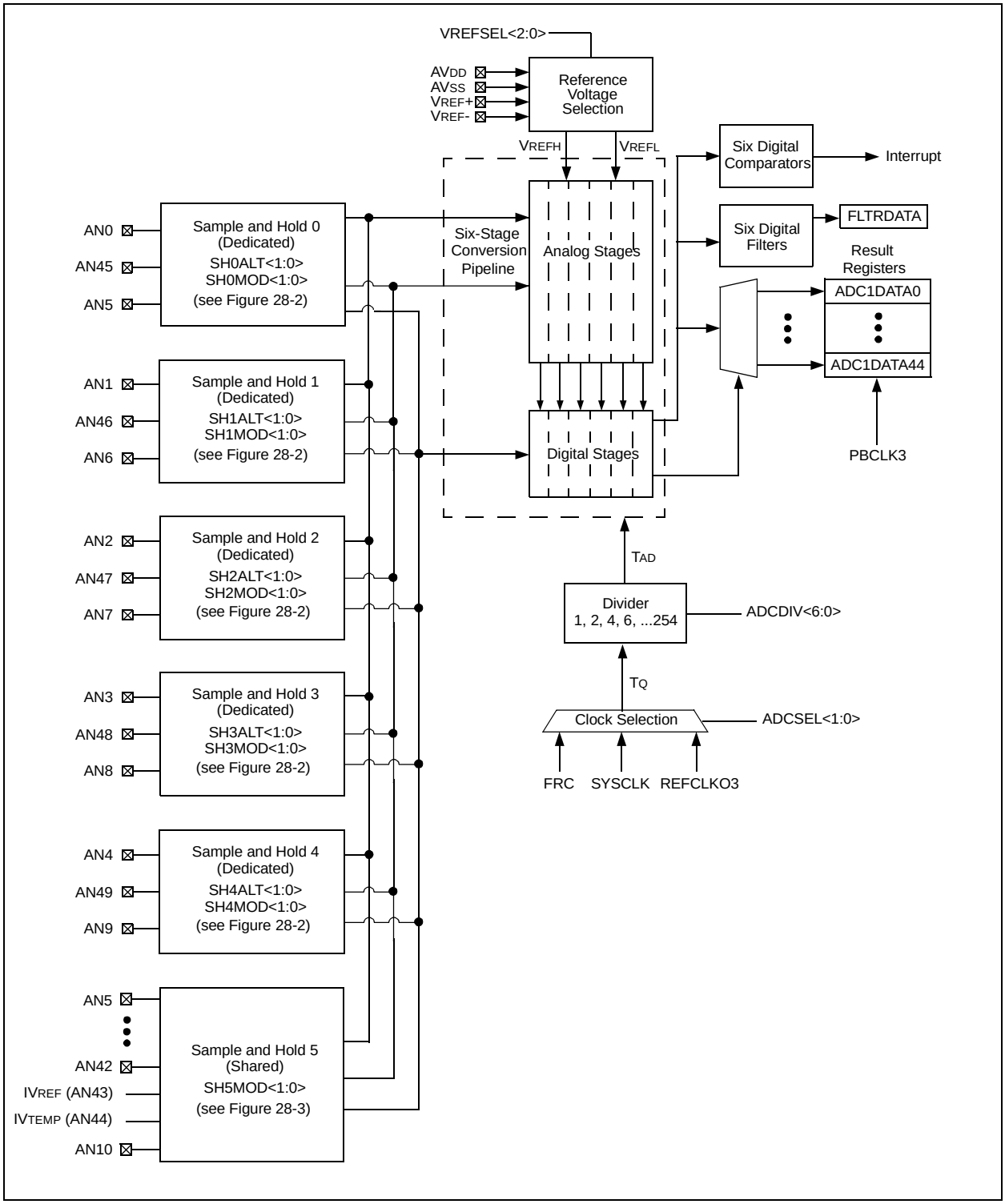
bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit(1,2)
- 11 = PCM/DSP mode
- 10 = Right Justified mode
- 01 = Left Justified mode
- 00 = I^2S mode

Note 1: This bit can only be written when the ON bit = 0.

2: This bit is only valid for AUDEN = 1.

FIGURE 28-1: ADC1 MODULE BLOCK DIAGRAM



REGISTER 28-2: AD1CON2: ADC1 CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ADCRDY(1)	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	BOOST	LOWPWR	—	—	—	ADCSEL<1:0>(2)	
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	ADCDIV<6:0>(2)						

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **ADCRDY:** ADC Ready bit(1)
1 = ADC module is ready for normal operation
0 = ADC is not ready for use

bit 30-24 **Unimplemented:** Read as '0'

bit 23-16 **SAMC<7:0>:** Sample Time for Shared S&H bits
11111111 = 256 TAD
•
•
•
00000001 = 2 TAD
00000000 = 1 TAD
This field specifies the number of ADC clock cycles allocated to the ADC sample time for the shared S&H circuit.

bit 15 **Unimplemented:** Read as '0'

bit 14 **BOOST:** Voltage Reference Boost bit
1 = Boost VREF
0 = Do not boost VREF
Changing the state of this bit requires that the ADC module be recalibrated by setting the CAL bit (AD1CON3<31>).

bit 13 **LOWPWR:** ADC Low-power bit
1 = Force the ADC module into a low-power state
0 = Exit ADC low-power state

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **ADCSEL<1:0>:** ADC Clock Source (TQ) bits(2)
11 = FRC
10 = REFCLKO3
01 = SYSCLK
00 = Reserved

bit 7 **Unimplemented:** Read as '0'

Note 1: This bit is set to '0' when ADCEN (AD1CON1<15>) = 0.
2: These bits should be configured prior to enabling the ADC by setting the ADCEN bit (AD1CON1<15>) = 1.

REGISTER 28-7: AD1CSS1: ADC1 INPUT SCAN SELECT REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25	CSS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CSSx:** ADC Input Scan Select bits ('x' = 0-31)
1 = Select ANx for input scan
0 = Skip ANx for input scan

Note 1: CSSx = ANx, where 'x' = 0-31.
2: Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSSx bits. Refer to the bit descriptions in the AD1TRGn register (Register 28-15) for selecting the STRIG option.

REGISTER 28-8: AD1CSS2: ADC1 INPUT SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CSS44	CSS43	CSS42	CSS41	CSS40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS39	CSS38	CSS37	CSS36	CSS35	CSS34	CSS33	CSS32

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'
bit 12-0 **CSSx:** ADC Input Scan Select bits ('x' = 32-44)
1 = Select ANx for input scan
0 = Skip ANx for input scan

Note 1: CSSx = ANx, where 'x' = 32-42, CSS43 = IV_{REF}, and CS44 = IV_{TEMP}.
2: Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSSx bits. Refer to the bit descriptions in the AD1TRGn register (Register 28-15) for selecting the STRIG option.

REGISTER 30-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)

bit 7 **AUTOFC:** Automatic Flow Control bit

1 = Automatic Flow Control enabled
0 = Automatic Flow Control disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **MANFC:** Manual Flow Control bit

1 = Manual Flow Control is enabled
0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every 128 * PTV<15:0>/2 TX clock cycles until the bit is cleared.

Note: For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 **Unimplemented:** Read as '0'

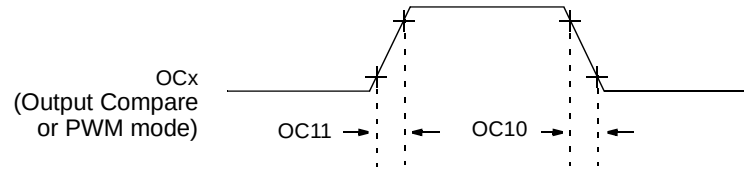
bit 0 **BUFCDEC:** Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

This bit is only used for RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

FIGURE 37-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

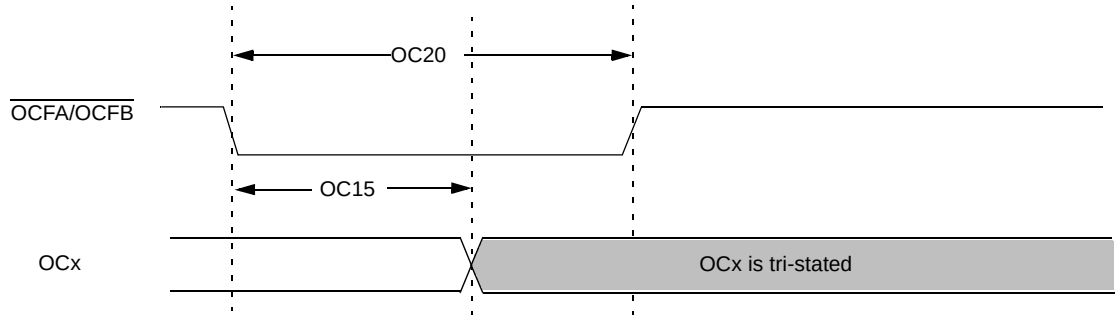
TABLE 37-28: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 37-9: OCx/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

TABLE 37-29: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typ.(2)**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 37-23: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

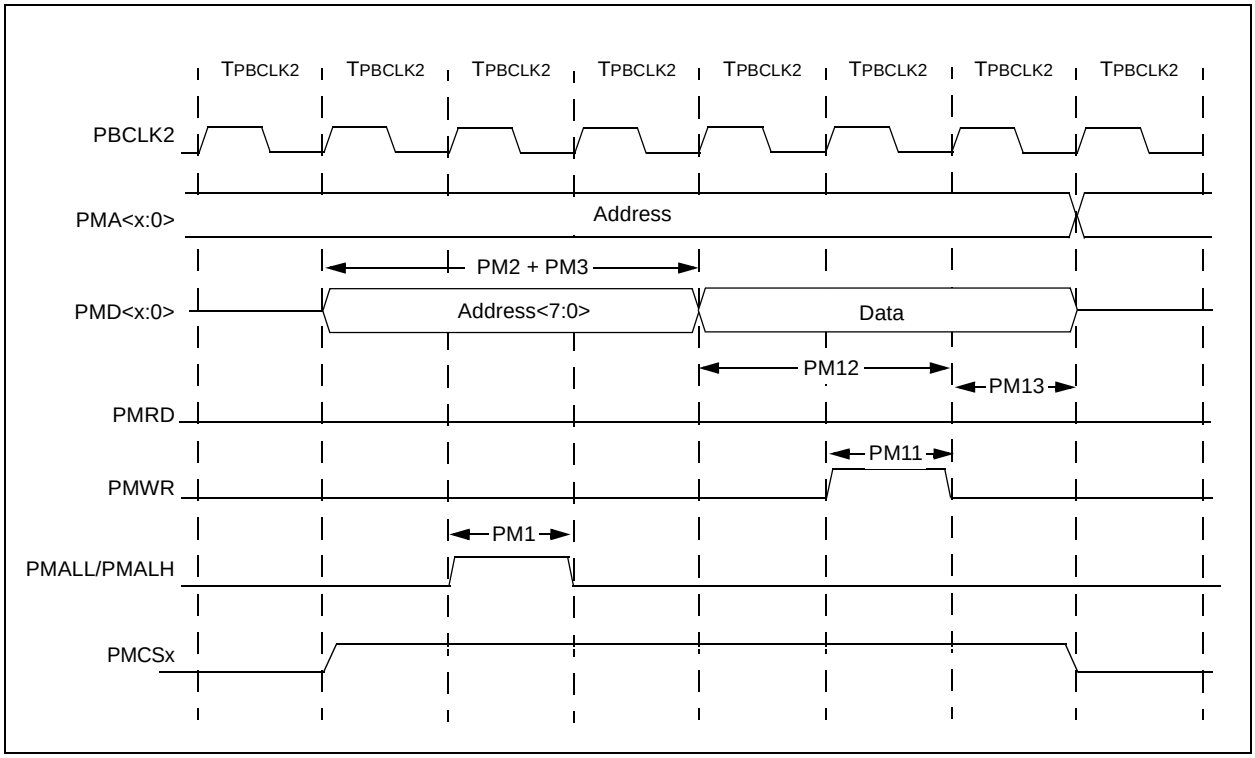


TABLE 37-43: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM11	TWR	PMWR Pulse Width	—	1 TPBCLK2	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPBCLK2	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPBCLK2	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.