Microchip Technology - PIC32MZ1024ECM144T-I/PH Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024ecm144t-i-ph

TABLE 1-16: ETHERNET MII I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
ERXD0	61	41	B32	81	I	ST	Ethernet Receive Data 0
ERXD1	58	42	B26	66	I	ST	Ethernet Receive Data 1
ERXD2	57	43	A31	67	I	ST	Ethernet Receive Data 2
ERXD3	56	44	A40	82	I	ST	Ethernet Receive Data 3
ERXERR	64	35	A30	65	I	ST	Ethernet Receive Error Input
ERXDV	62	12	B40	101	I	ST	Ethernet Receive Data Valid
ERXCLK	63	16	B12	27	I	ST	Ethernet Receive Clock
ETXD0	2	86	A5	7	O	—	Ethernet Transmit Data 0
ETXD1	3	85	B4	8	O	—	Ethernet Transmit Data 1
ETXD2	43	79	B17	43	O	—	Ethernet Transmit Data 2
ETXD3	46	80	A22	44	O	—	Ethernet Transmit Data 3
ETXERR	50	87	B44	114	O	—	Ethernet Transmit Error
ETXEN	1	77	A57	120	O	—	Ethernet Transmit Enable
ETXCLK	51	78	B47	121	I	ST	Ethernet Transmit Clock
ECOL	44	10	B33	83	I	ST	Ethernet Collision Detect
ECRS	45	11	A47	100	I	ST	Ethernet Carrier Sense
EMDC	30	70	B39	99	O	—	Ethernet Management Data Clock
EMDIO	49	71	A55	115	I/O	—	Ethernet Management Data

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-17: ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Ethernet MII Interface							
ERXD0	61	41	B32	81	I	ST	Ethernet Receive Data 0
ERXD1	58	42	B26	66	I	ST	Ethernet Receive Data 1
ERXERR	64	35	A30	65	I	ST	Ethernet Receive Error Input
ETXD0	2	86	A5	7	O	—	Ethernet Transmit Data 0
ETXD1	3	85	B4	8	O	—	Ethernet Transmit Data 1
ETXEN	1	77	A57	120	O	—	Ethernet Transmit Enable
EMDC	30	70	B39	99	O	—	Ethernet Management Data Clock
EMDIO	49	71	A55	115	I/O	—	Ethernet Management Data
EREFCLK	63	16	B12	27	I	ST	Ethernet Reference Clock
ECRSDV	62	12	B40	101	I	ST	Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

2.7.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- COUT = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e.,12 mm length) = 2.5 pF

Crystals with a speed of 4 MHz to 12 MHz that meet the following requirements will meet the PIC32MZ EC oscillation requirements when configured, as depicted in Figure 8-1.

1. Manufacturer Drive Level (min) ≤ 10 µW (hard requirements, 1 µW preferred).
2. Manufacturer ESR ≤ 50Ω (hard requirement, lower is better).

2.7.1.1 Calculating XTAL Capacitive Loading:

1. PIC32 CIN = COUT = ~4 pF (PIC32 OSCI and OSCO package pin capacitance).
2. C1MFG = C2MFG = Manufacturer Recommended Load Capacitance.
3. CLOAD = {([CIN + C1MFG] [C2MFG + COUT]) / [CIN + C1MFG + C2MFG + COUT]} + estimated PCB stray capacitance (2.5 pF).

   (Simplified) CLOAD = (((CIN + C1MFG) / 2) + 2.5 pF).

Actual C1, C2 Load value to use:

- C2 = CLOAD
- C1 = (CLOAD - 2 pF)

Note:	These recommendations are atypical, and are only applicable to the PIC32MZ EC family.

2.7.1.2 Validated Crystals

Temperature Range: (-45°C to +110°C)

VDD = 2.4V to 3.6V, RP = 1 MΩ, RK = 10 kΩ

- ABLS-12.000 MHz-L4Q-T (12 MHz surface mount)

Note:	These recommendations are atypical, and only applicable to the PIC32MZ EC family.

2.7.1.3 Additional Microchip References

- AN588 *"PICmicro® Microcontroller Oscillator Design Guide"*
- AN826 *"Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- AN849 *"Basic PICmicro® Oscillator Design"*

2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to VSS through a 1k to 10k resistor and configuring the pin as an input.

2.9 Designing for High-Speed Peripherals

The PIC32MZ EC family devices have peripherals that operate at frequencies much higher than typical for an embedded environment. Table 2-1 lists the peripherals that produce high-speed signals on their external pins:

TABLE 2-1: PERIPHERALS THAT PRODUCE HS SIGNALS ON EXTERNAL PINS

Peripheral	High-Speed Signal Pins	Maximum Speed on Signal Pin
EBI	EBIAx, EBIDx	50 MHz
SQI1	SQICLK, $\overline{\text{SQICSx}}$, SQIDx	50 MHz
HS USB	D+, D-	480 MHz

Due to these high-speed signals, it is important to take into consideration several factors when designing a product that uses these peripherals, as well as the PCB on which these components will be placed. Adhering to these recommendations will help achieve the following goals:

- Minimize the effects of electromagnetic interference to the proper operation of the product
- Ensure signals arrive at their intended destination at the same time
- Minimize crosstalk
- Maintain signal integrity
- Reduce system noise
- Minimize ground bounce and power sag

NOTES:

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
03F0	IPC43	31:16	—	—	—	I2C4MIP<2:0>			I2C4MIS<1:0>		—	—	—	I2C4SIP<2:0>			I2C4SIS<1:0>		0000
		15:0	—	—	—	I2C4BIP<2:0>			I2C4BIS<1:0>		—	—	—	U4TXIP<2:0>			U4TXIS<1:0>		0000
0400	IPC44	31:16	—	—	—	U5EIP<2:0>			U5EIS<1:0>		—	—	—	SPI5TXIP<2:0>(2)			SPI5TXIS<1:0>(2)		0000
		15:0	—	—	—	SPI5RXIP<2:0>(2)			SPI5RXIS<1:0>(2)		—	—	—	SPI5EIP<2:0>(2)			SPI5EIS<1:0>(2)		0000
0410	IPC45	31:16	—	—	—	I2C5SIP<2:0>			I2C5SIS<1:0>		—	—	—	I2C5BIP<2:0>			I2C5BIS<1:0>		0000
		15:0	—	—	—	U5TXIP<2:0>			U5TXIS<1:0>		—	—	—	U5RXIP<2:0>			U5RXIS<1:0>		0000
0420	IPC46	31:16	—	—	—	SPI6TXIP<2:0>(2)			SPI6TXIS<1:0>(2)		—	—	—	SPI6RXIP<2:0>(2)			SPI6RXIS<1:0>(2)		0000
		15:0	—	—	—	SPI6EIP<2:0>(2)			SPI6EIS<1:0>(2)		—	—	—	I2C5MIP<2:0>			I2C5MIS<1:0>		0000
0430	IPC47	31:16	—	—	—	—	—	—	—	—	—	—	—	U6TXIP<2:0>			U6TXIS<1:0>		0000
		15:0	—	—	—	U6RXIP<2:0>			U6RXIS<1:0>		—	—	—	U6EIP<2:0>			U6EIS<1:0>		0000
0540	OFF000	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0544	OFF001	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0548	OFF002	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
054C	OFF003	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0550	OFF004	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0554	OFF005	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0558	OFF006	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
055C	OFF007	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0560	OFF008	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0564	OFF009	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

9.2 Prefetch Control Registers

TABLE 9-1: PREFETCH REGISTER MAP

Virtual Address (BF8E_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	PRECON	31:16	—	—	—	—	—	PFMSECEN	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	PREFEN<1:0>		—	PFMWS<2:0>			0007
0010	PRESTAT	31:16	—	—	—	—	PFMDED	PFMSEC	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PFMSECCNT<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15B0	DCH7ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
15C0	DCH7INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
15D0	DCH7SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
15E0	DCH7DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
15F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 11-5: USBIE0CSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0, HC	R/W-0	R/W-0, HC
	—	—	—	—	—	—	—	FLSHFIFO
					DISPING	DTWREN	DATATGGL	
23:16	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/C-0, HS	R/W-0, HS	R-0, HS	R-0	R-0
	SVCSETEND	SVCRPR	SENDSTALL	SETUPEND	DATAEND	SENTSTALL	TXPKTRDY	RXPKTRDY
	NAKTMOUT	STATPKT	REQPKT	ERROR	SETUPPKT	RXSTALL		
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **DISPING:** Disable Ping tokens control bit (*Host mode*)
1 = USB Module will not issue PING tokens in data and status phases of a Hi-Speed Control transfer
0 = Ping tokens are issued

bit 26 **DTWREN:** Data Toggle Write Enable bit (*Host mode*)
1 = Enable the current state of the Endpoint 0 data toggle to be written. Automatically cleared.
0 = Disable data toggle write

bit 25 **DATATGGL:** Data Toggle bit (*Host mode*)
When read, this bit indicates the current state of the Endpoint 0 data toggle.
If DTWREN = 1, this bit is writable with the desired setting.
If DTWREN = 0, this bit is read-only.

bit 24 **FLSHFIFO:** Flush FIFO Control bit
1 = Flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset and the TXPKTRDY/RXPKTRDY bit is cleared. Automatically cleared when the operation completes. Should only be used when TXPKTRDY/RXPKTRDY = 1.
0 = No Flush operation

bit 23 **SVCSETEND:** Clear SETUPEND Control bit (*Device mode*)
1 = Clear the SETUPEND bit in this register. This bit is automatically cleared.
0 = Do not clear

NAKTMOUT: NAK Time-out Control bit (*Host mode*)
1 = Endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the NAKLIM<4:0> bits (USBICSR<28:24>)
0 = Allow the endpoint to continue

bit 22 **SVCRPR:** Serviced RXPKTRDY Clear Control bit (*Device mode*)
1 = Clear the RXPKTRDY bit in this register. This bit is automatically cleared.
0 = Do not clear

STATPKT: Status Stage Transaction Control bit (*Host mode*)
1 = When set at the same time as the TXPKTRDY or REQPKT bit is set, performs a status stage transaction
0 = Do not perform a status stage transaction

REGISTER 11-16: USBINFO: USB INFORMATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	VPLEN<7:0>							
23:16	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	WTCON<3:0>				WTID<3:0>			
15:8	R-1	R-0	R-0	R-0	R-1	R-1	R-0	R-0
	DMACHANS<3:0>				RAMBITS<3:0>			
7:0	R-0	R-1	R-1	R-1	R-0	R-1	R-1	R-1
	RXENDPTS<3:0>				TXENDPTS<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **VPLEN<7:0>:** VBUS pulsing charge length bits

Sets the duration of the VBUS pulsing charge in units of 546.1 µs. (The default setting corresponds to 32.77 ms.)

bit 23-20 **WTCON<3:0>:** Connect/Disconnect filter control bits

Sets the wait to be applied to allow for the connect/disconnect filter in units of 533.3 ns. The default setting corresponds to 2.667 µs.

bit 19-6 **WTID<3:0>:** ID delay valid control bits

Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. The default setting corresponds to 52.43ms.

bit 15-12 **DMACHANS<3:0>:** DMA Channels bits

These read-only bits provide the number of DMA channels in the USB module. For the PIC32MZ EC family, this number is 8.

bit 11-8 **RAMBITS<3:0>:** RAM address bus width bits

These read-only bits provide the width of the RAM address bus. For the PIC32MZ EC family, this number is 12.

bit 7-4 **RXENDPTS<3:0>:** Included RX Endpoints bits

This read-only register gives the number of RX endpoints in the design. For the PIC32MZ EC family, this number is 7.

bit 3-0 **TXENDPTS<3:0>:** Included TX Endpoints bits

These read-only bits provide the number of TX endpoints in the design. For the PIC32MZ EC family, this number is 7.

16.1 Watchdog Timer Control Registers

TABLE 16-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	WDTCON(1)	31:16	WDTCLRKEY<15:0>																0000
		15:0	ON	—	—	—	—	—	—	—	—	SWDTPS<4:0>					WDTWINEN	—	x0xx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 20-5: SQI1CLKCON: SQI CLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CLKDIV<7:0>(1)							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R/W-0
	—	—	—	—	—	—	STABLE	EN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **CLKDIV<7:0>:** SQI Clock TSQI Frequency Select bit(1)

10000000 = Base clock TBC is divided by 512
01000000 = Base clock TBC is divided by 256
00100000 = Base clock TBC is divided by 128
00010000 = Base clock TBC is divided by 64
00001000 = Base clock TBC is divided by 32
00000100 = Base clock TBC is divided by 16
00000010 = Base clock TBC is divided by 8
00000001 = Base clock TBC is divided by 4
00000000 = Base clock TBC is divided by 2

Setting these bits to '00000000' specifies the highest frequency of the SQI clock.

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **STABLE:** TSQI Clock Stable Select bit

This bit is set to '1' when the SQI clock, TSQI, is stable after writing a '1' to the EN bit.
1 = TSQI clock is stable
0 = TSQI clock is not stable

bit 0 **EN:** TSQI Clock Enable Select bit

When clock oscillation is stable, the SQI module will set the STABLE bit to '1'.
1 = Enable the SQI clock (TSQI) (when clock oscillation is stable, the SQI module sets the STABLE bit to '1')
0 = Disable the SQI clock (TSQI) (the SQI module should stop its clock to enter a low power state); SFRs can still be accessed, as they use PBCLK5

Note 1: Refer to Table in **Section 37.0 "Electrical Characteristics"** for the maximum clock frequency specifications.

REGISTER 24-3: EBISMTx: EXTERNAL BUS INTERFACE STATIC MEMORY TIMING REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	PAGEMODE	TPRC<3:0>(1)				TBTA<2:0>(1)		
15:8	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
	TWP<5:0>(1)						TWR<1:0>(1)	
7:0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1
	TAS<1:0>(1)		TRC<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **RDYMODE:** Data Ready Device Select bit
The device associated with register set 'x' is a data-ready device, and will use the EBIRDYx pin.
1 = EBIRDYx input is used
0 = EBIRDYx input is not used

bit 25-24 **PAGESIZE<1:0>:** Page Size for Page Mode Device bits
11 = 32-word page
10 = 16-word page
01 = 8-word page
00 = 4-word page

bit 23 **PAGEMODE:** Memory Device Page Mode Support bit
1 = Device supports Page mode
0 = Device does not support Page mode

bit 22-19 **TPRC<3:0>:** Page Mode Read Cycle Time bits(1)
Read cycle time is TPRC + 1 clock cycle.

bit 18-16 **TBTA<2:0>:** Data Bus Turnaround Time bits(1)
Clock cycles (0-7) for static memory between read-to-write, write-to-read, and read-to-read when Chip Select changes.

bit 15-10 **TWP<5:0>:** Write Pulse Width bits(1)
Write pulse width is TWP + 1 clock cycle.

bit 9-8 **TWR<1:0>:** Write Address/Data Hold Time bits(1)
Number of clock cycles to hold address or data on the bus.

bit 7-6 **TAS<1:0>:** Write Address Setup Time bits(1)
Clock cycles for address setup time. A value of '0' is only valid in the case of SSRAM.

bit 5-0 **TRC<5:0>:** Read Cycle Time bits(1)
Read cycle time is TRC + 1 clock cycle.

Note 1: Please refer to **Section 47. "External Bus Interface (EBI)"** (DS60001245) in the *"PIC32 Family Reference Manual"* for the EBI timing diagrams and additional information.

25.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

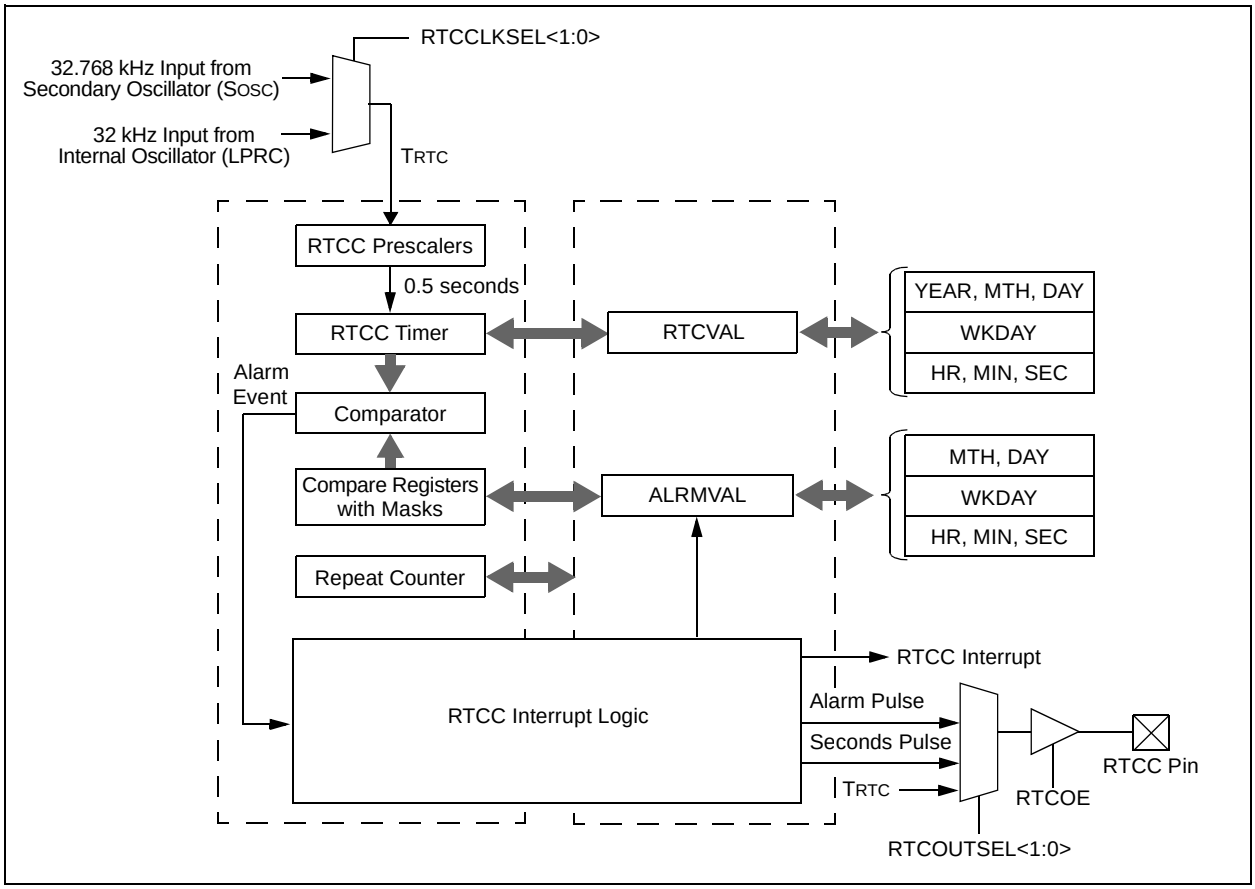
Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are key features of the RTCC module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

FIGURE 25-1: RTCC BLOCK DIAGRAM



26.0 CRYPTO ENGINE

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Crypto Engine is intended to accelerate applications that need cryptographic functions. By executing these functions in the hardware module, software overhead is reduced, and actions such as encryption, decryption, and authentication can execute much more quickly.

The Crypto Engine uses an internal descriptor-based DMA for efficient programming of the security association data and packet pointers (allowing scatter/gather data fetching). An intelligent state machine schedules the Crypto Engines based on the protocol selection and packet boundaries. The hardware engines can perform the encryption and authentication in sequence or in parallel.

Note: To avoid cache coherency problems on devices with L1 cache, Crypto buffers must only be allocated or accessed from the KSEG1 segment.

Key features of the Crypto Engine include:

- Bulk ciphers and hash engines
- Integrated DMA to off-load processing:
  - Buffer descriptor-based
  - Secure association per buffer descriptor
- Some functions can execute in parallel

Bulk ciphers that are handled by the Crypto Engine include:

- AES:
  - 128-bit, 192-bit, and 256-bit key sizes
  - CBC, ECB, CTR, CFB, and OFB modes
- DES/TDES:
  - CBC, ECB, CFB, and OFB modes

Authentication engines that are available through the Crypto Engine include:

- SHA-1
- SHA-256
- MD-5
- AES-GCM
- HMAC operation (for all authentication engines)

The rate of data that can be processed by the Crypto Engine depends on a number of factors, including:

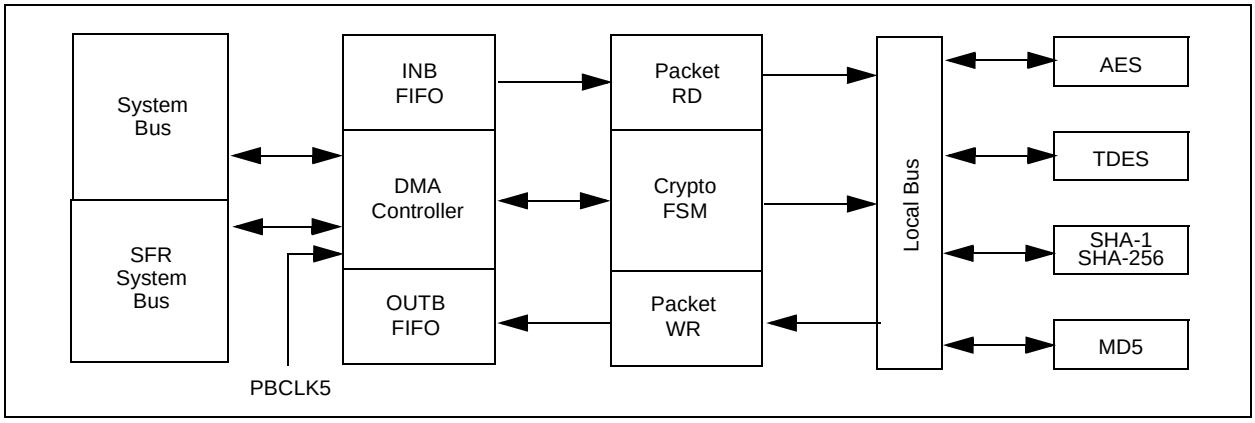
- Which engine is in use
- Whether the engines are used in parallel or in series
- The demands on source and destination memories by other parts of the system (i.e., CPU, DMA, etc.)
- The speed of PBCLK5, which drives the Crypto Engine

Table 26-1 shows typical performance for various engines.

TABLE 26-1: CRYPTO ENGINE PERFORMANCE

Engine/ Algorithm	Performance Factor (Mbps/MHz)	Maximum Mbps (PBCLK5 = 100 MHz)
DES	14.4	1440
TDES	6.6	660
AES-128	9.0	900
AES-192	7.9	790
AES-256	7.2	720
MD5	15.6	1560
SHA-1	13.2	1320
SHA-256	9.3	930

FIGURE 26-1: CRYPTO ENGINE BLOCK DIAGRAM



REGISTER 26-5: CESTAT: CRYPTO ENGINE STATUS REGISTER (CONTINUED)

bit 16 **ACTIVE:** Buffer Descriptor Processor Status bit
1 = BDP is active
0 = BDP is idle

bit 15-0 **BDCTRL<15:0>:** Descriptor Control Word Status bits
These bits contain the current descriptor control word.

REGISTER 31-1: CMxCON: COMPARATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON	COE	CPOL(1)	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit
- 1 = Module is enabled. Setting this bit does not affect the other bits in this register
- 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is driven on the output CxOUT pin
- 0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit(1)
- 1 = Output is inverted
- 0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
- 1 = Output of the Comparator is a '1'
- 0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
- 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
- 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
- 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
- 00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit
- 1 = Comparator non-inverting input is connected to the internal CVREF
- 0 = Comparator non-inverting input is connected to the CXINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
- 11 = Comparator inverting input is connected to the IVREF
- 10 = Comparator inverting input is connected to the CxIND pin
- 01 = Comparator inverting input is connected to the CxINC pin
- 00 = Comparator inverting input is connected to the CxINB pin

Note 1: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

REGISTER 34-1: DEVSIGN0/ADEVSIGN0: DEVICE SIGNATURE WORD 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '0'

bit 30-0 **Reserved:** Write as '1'

Note:	The DEVSIGN1 through DEVSIGN3 and ADEVSIGN1 through ADEVSIGN3 registers are used for Quad Word programming operation when programming the DEVSIGN0/ADESIGN0 registers, and do not contain any valid information.

REGISTER 34-2: DEVCP0/ADEVCP0: DEVICE CODE-PROTECT 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	R/P	r-1	r-1	r-1	r-1
	—	—	—	CP	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Reserved:** Write as '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection is disabled
0 = Protection is enabled

bit 27-0 **Reserved:** Write as '1'

Note:	The DEVCP1 through DEVCP3 and ADEVCP1 through ADEVCP3 registers are used for Quad Word programming operation when programming the DEVCP0/ADEVCP0 registers, and do not contain any valid information.

REGISTER 34-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 3 **Reserved:** Write as '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 2)**	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 2)**	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

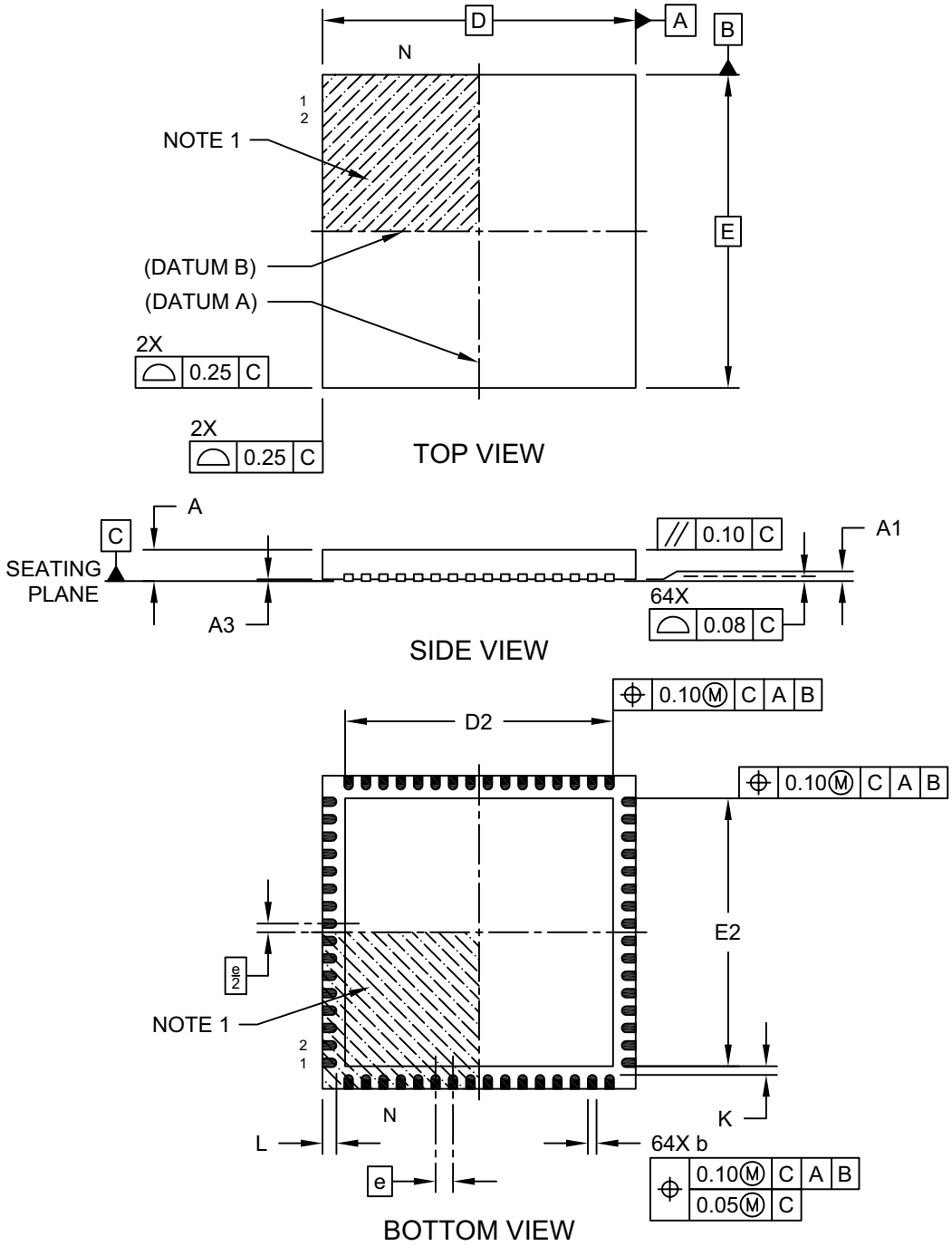
2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

39.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.70 x 7.70 Exposed Pad [QFN]

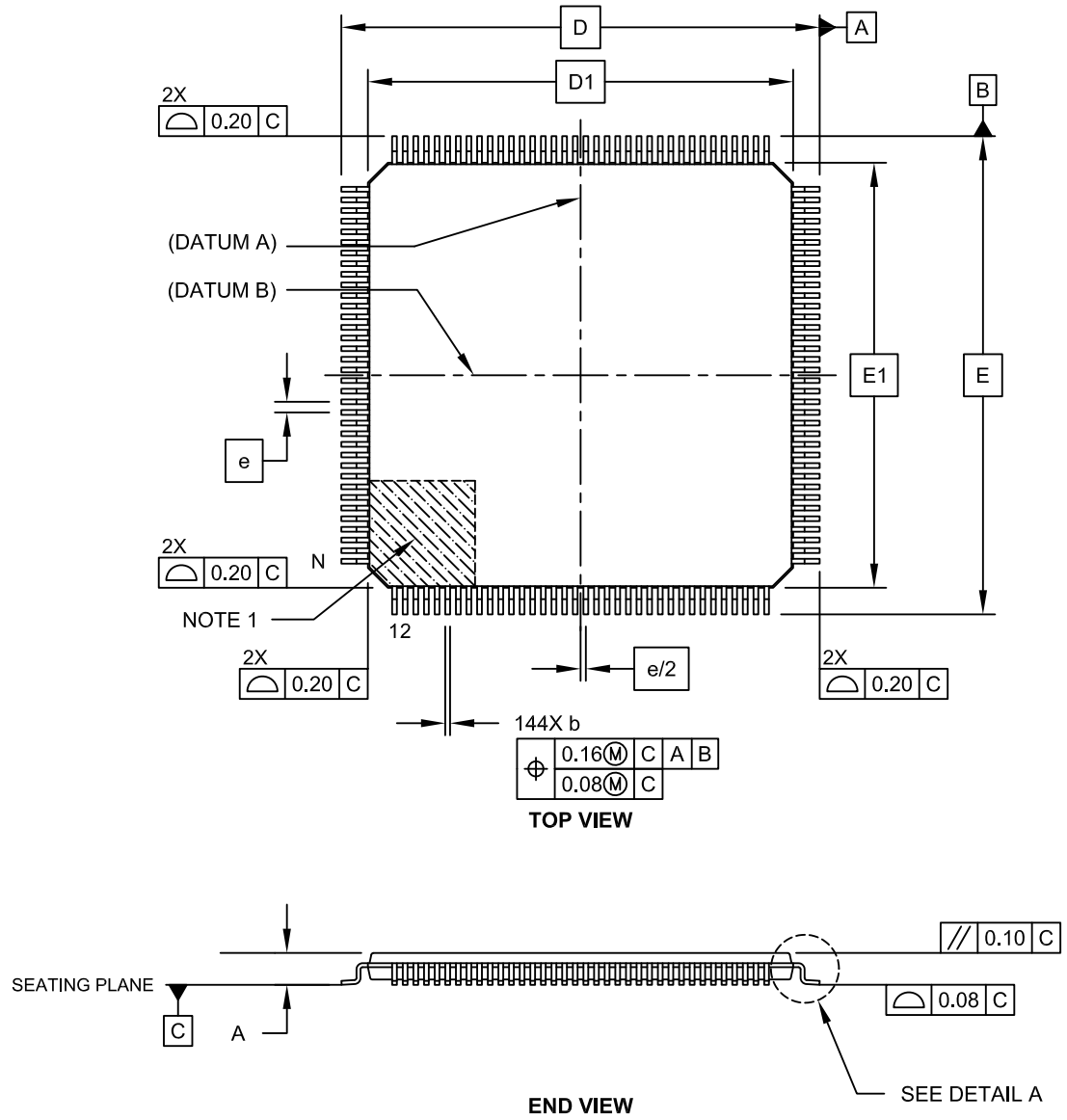
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-213B Sheet 1 of 2

144-Lead Plastic Thin Quad Flatpack (PH)-16x16x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-155B Sheet 1 of 2