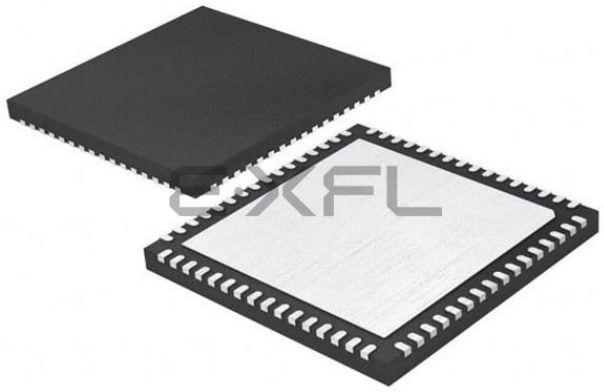

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Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecg064-i-mr

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Output Compare							
OC1	PPS	PPS	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	PPS	O	—	
OC6	PPS	PPS	PPS	PPS	O	—	
OC7	PPS	PPS	PPS	PPS	O	—	
OC8	PPS	PPS	PPS	PPS	O	—	
OC9	PPS	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	B24	62	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
External Interrupts							
INT0	46	71	A48	104	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

REGISTER 4-1: BFxSEQ0/ABFxSEQ0: BOOT FLASH 'x' SEQUENCE WORD 0 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<7:0>							
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CSEQ<15:0>:** Boot Flash Complement Sequence Number bits

bit 15-0 **TSEQ<15:0>:** Boot Flash True Sequence Number bits

Note: The BFxSEQ1 through BFxSEQ3 and ABFxSEQ1 through ABFxSEQ3 registers are used for Quad Word programming operation when programming the BFxSEQ0/ABFxSEQ0 registers, and do not contain any valid information.

TABLE 4-21: SYSTEM BUS TARGET 13 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B420	SBT13ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
B424	SBT13ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
B428	SBT13ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
B430	SBT13ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B438	SBT13ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B440	SBT13REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
B450	SBT13RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
B458	SBT13WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 7 uses Shadow Set 0)
0111 = Interrupt with a priority level of 7 uses Shadow Set 7
0110 = Interrupt with a priority level of 7 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 6 uses Shadow Set 0)
0111 = Interrupt with a priority level of 6 uses Shadow Set 7
0110 = Interrupt with a priority level of 6 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 5 uses Shadow Set 0)
0111 = Interrupt with a priority level of 5 uses Shadow Set 7
0110 = Interrupt with a priority level of 5 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 5 uses Shadow Set 1
0000 = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 4 uses Shadow Set 0)
0111 = Interrupt with a priority level of 4 uses Shadow Set 7
0110 = Interrupt with a priority level of 4 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 4 uses Shadow Set 1
0000 = Interrupt with a priority level of 4 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

REGISTER 11-7: USBIE0CSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-0	R-x	R-x	R-x	R-1	R-0
	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **MPRXEN:** Automatic Amalgamation Option bit
1 = Automatic amalgamation of bulk packets is done
0 = No automatic amalgamation

bit 30 **MPTXEN:** Automatic Splitting Option bit
1 = Automatic splitting of bulk packets is done
0 = No automatic splitting

bit 29 **BIGEND:** Byte Ordering Option bit
1 = Big Endian ordering
0 = Little Endian ordering

bit 28 **HBRXEN:** High-bandwidth RX ISO Option bit
1 = High-bandwidth RX ISO endpoint support is selected
0 = No High-bandwidth RX ISO support

bit 27 **HBTXEN:** High-bandwidth TX ISO Option bit
1 = High-bandwidth TX ISO endpoint support is selected
0 = No High-bandwidth TX ISO support

bit 26 **DYNFIFOS:** Dynamic FIFO Sizing Option bit
1 = Dynamic FIFO sizing is supported
0 = No Dynamic FIFO sizing

bit 25 **SOFTCONE:** Soft Connect/Disconnect Option bit
1 = Soft Connect/Disconnect is supported
0 = Soft Connect/Disconnect is not supported

bit 24 **UTMIDWID:** UTMI+ Data Width Option bit
Always '0', indicating 8-bit UTMI+ data width

bit 23-0 **Unimplemented:** Read as '0'

REGISTER 11-17: USBEOFRST: USB END-OF-FRAME/SOFT RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	NRSTX	NRST
23:16	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-0	R/W-1	R/W-0
	LSEOF<7:0>							
15:8	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-1	R/W-1	R/W-1
	FSEOF<7:0>							
7:0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R.W-0	R/W-0	R/W-0
	HSEOF<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **NRSTX:** Reset of XCLK Domain bit
1 = Reset the XCLK domain, which is clock recovered from the received data by the PHY
0 = Normal operation

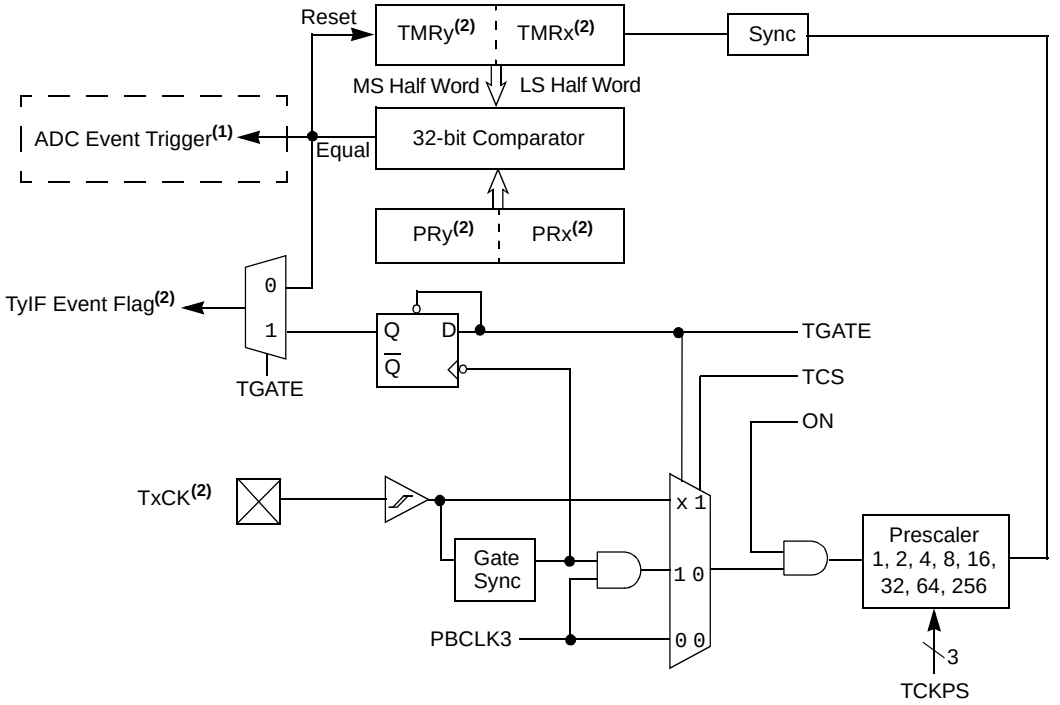
bit 24 **NRST:** Reset of CLK Domain bit
1 = Reset the CLK domain, which is clock recovered from the peripheral bus
0 = Normal operation

bit 23-16 **LSEOF<7:0>:** Low-Speed EOF bits
These bits set the Low-Speed transaction in units of 1.067 µs (default setting is 121.6 µs) prior to the EOF to stop new transactions from beginning.

bit 15-8 **FSEOF<7:0>:** Full-Speed EOF bits
These bits set the Full-Speed transaction in units of 533.3 µs (default setting is 63.46 µs) prior to the EOF to stop new transactions from beginning.

bit 7-0 **HSEOF<7:0>:** Hi-Speed EOF bits
These bits set the Hi-Speed transaction in units of 133.3 µs (default setting is 17.07 µs) prior to the EOF to stop new transactions from beginning.

FIGURE 14-2: TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9 BLOCK DIAGRAM (32-BIT)



Note 1: ADC event trigger is available only on the Timer2/3 and TImer4/5 pairs.
2: In this diagram, 'x' represents Timer2, 4, 6, or 8, and 'y' represents Timer3, 5, 7, or 9.

18.1 Output Compare Control Registers

TABLE 18-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
4020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
4200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
4220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
4400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
4420	OC3RS	31:16	OC3RS<31:0>																xxxx
		15:0																	xxxx
4600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
4620	OC4RS	31:16	OC4RS<31:0>																xxxx
		15:0																	xxxx
4800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
4820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 20-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCURBUFLEN<7:0>:** Current DMA Receive Buffer Length Status bits
These bits provide the length of the current DMA receive buffer.

REGISTER 20-22: SQI1INTSEN: SQI INTERRUPT SIGNAL ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	PKT DONEISE	BD DONEISE	CON THRISE
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10 **PKTDONEISE:** Receive Error Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 9 **BDDONEISE:** Transmit Error Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 8 **CONTHRISE:** Control Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 7 **CONEMPTYISE:** Control Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 6 **CONFULLISE:** Control Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 5 **RXTHRISE:** Receive Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 4 **RXFULLISE:** Receive Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 3 **RXEMPTYISE:** Receive Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 2 **TXTHRISE:** Transmit Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 1 **TXFULLISE:** Transmit Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 0 **TXEMPTYISE:** Transmit Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

REGISTER 25-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN(1,2)	CHIME(2)	PIV(2)	ALRMSYNC	AMASK<3:0>(2)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit(1,2)
- 1 = Alarm is enabled
- 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)
- 1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit
- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing.
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is more than 32 real-time clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(2)
- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved
- 1011 = Reserved
- 11xx = Reserved

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note: This register is reset only on a Power-on Reset (POR).

REGISTER 28-13: AD1CMPn: ADC1 DIGITAL COMPARATOR REGISTER 'n' ('n' = 1, 2, 3, 4, 5 OR 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPHI<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPHI<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPLO<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPLO<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **ADCMPHI<15:0>:** Digital Analog Comparator High Limit Value bits

These bits store the high limit value, which is used for comparisons with the analog-to-digital conversion data. The user is responsible for formatting the data as signed or unsigned to match the data format as specified by the SHxMOD<1:0> bits for the associated S&H circuit and the FRACT bit.

bit 15-0 **ADCMPLO<15:0>:** Digital Analog Comparator Low Limit Value bits

These bits store the low limit value, which is used for comparisons with the analog-to-digital conversion data. The user is responsible for formatting the data as signed or unsigned to match the data format as specified by the SHxMOD<1:0> bits for the associated S&H circuit and the FRACT bit.

Note: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

Table 30-1, Table 30-2, Table 30-3 and Table 30-4 show four interfaces and the associated pins that can be used with the Ethernet Controller.

TABLE 30-1: MII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXCLK	Transmit Clock
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
ETXD2	Transmit Data
ETXD3	Transmit Data
ETXERR	Transmit Error
ERXCLK	Receive Clock
ERXDV	Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXD2	Receive Data
ERXD3	Receive Data
ERXERR	Receive Error
ECRS	Carrier Sense
ECOL	Collision Indication

TABLE 30-2: RMII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
EREFCLK	Reference Clock
ECRSDV	Carrier Sense – Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXERR	Receive Error

Note: Ethernet controller pins that are not used by a selected interface can be used by other peripherals.

TABLE 30-3: MII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 0)

Pin Name	Description
AEMDC	Management Clock
AEMDIO	Management I/O
AETXCLK	Transmit Clock
AETXEN	Transmit Enable
AETXD0	Transmit Data
AETXD1	Transmit Data
AETXD2	Transmit Data
AETXD3	Transmit Data
AETXERR	Transmit Error
AERXCLK	Receive Clock
AERXDV	Receive Data Valid
AERXD0	Receive Data
AERXD1	Receive Data
AERXD2	Receive Data
AERXD3	Receive Data
AERXERR	Receive Error
AECRS	Carrier Sense
AECOL	Collision Indication

Note: The MII mode Alternate Interface is not available on 64-pin devices.

TABLE 30-4: RMII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 0)

Pin Name	Description
AEMDC	Management Clock
AEMDIO	Management I/O
AETXEN	Transmit Enable
AETXD0	Transmit Data
AETXD1	Transmit Data
AEREFCLK	Reference Clock
AECRSDV	Carrier Sense – Receive Data Valid
AERXD0	Receive Data
AERXD1	Receive Data
AERXERR	Receive Error

REGISTER 30-5: ETHHT0: ETHERNET CONTROLLER HASH TABLE 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **HT<31:0>:** Hash Table Bytes 0-3 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 30-6: ETHHT1: ETHERNET CONTROLLER HASH TABLE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<39:32>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **HT<63:32>:** Hash Table Bytes 4-7 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 30-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 30-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

bit 6 **VLANPAD:** VLAN Pad Enable bit(1,2)
1 = The MAC will pad all short frames to 64 bytes and append a valid CRC
0 = The MAC does not perform padding of short frames

bit 5 **PADENABLE:** Pad/CRC Enable bit(1,3)
1 = The MAC will pad all short frames
0 = The frames presented to the MAC have a valid length

bit 4 **CRCENABLE:** CRC Enable1 bit
1 = The MAC will append a CRC to every frame whether padding was required or not. Must be set if the PADENABLE bit is set.
0 = The frames presented to the MAC have a valid CRC

bit 3 **DELAYCRC:** Delayed CRC bit
This bit determines the number of bytes, if any, of proprietary header information that exist on the front of the IEEE 802.3 frames.
1 = Four bytes of header (ignored by the CRC function)
0 = No proprietary header

bit 2 **HUGEFRM:** Huge Frame enable bit
1 = Frames of any length are transmitted and received
0 = Huge frames are not allowed for receive or transmit

bit 1 **LENGTHCK:** Frame Length checking bit
1 = Both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the transmit/receive statistics vector.
0 = Length/Type field check is not performed

bit 0 **FULLDPLX:** Full-Duplex Operation bit
1 = The MAC operates in Full-Duplex mode
0 = The MAC operates in Half-Duplex mode

Note 1: Table 30-6 provides a description of the pad function based on the configuration of this register.
2: This bit is ignored if the PADENABLE bit is cleared.
3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note:	Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

TABLE 30-6: PAD OPERATION

Type	AUTOPAD	VLANPAD	PADENABLE	Action
Any	x	x	0	No pad, check CRC
Any	0	0	1	Pad to 60 Bytes, append CRC
Any	x	1	1	Pad to 64 Bytes, append CRC
Any	1	0	1	If untagged: Pad to 60 Bytes, append CRC If VLAN tagged: Pad to 64 Bytes, append CRC

35.0 INSTRUCTION SET

The PIC32MZ Embedded Connectivity (EC) Family family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32MZ EC device family *does not* support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

FIGURE 37-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

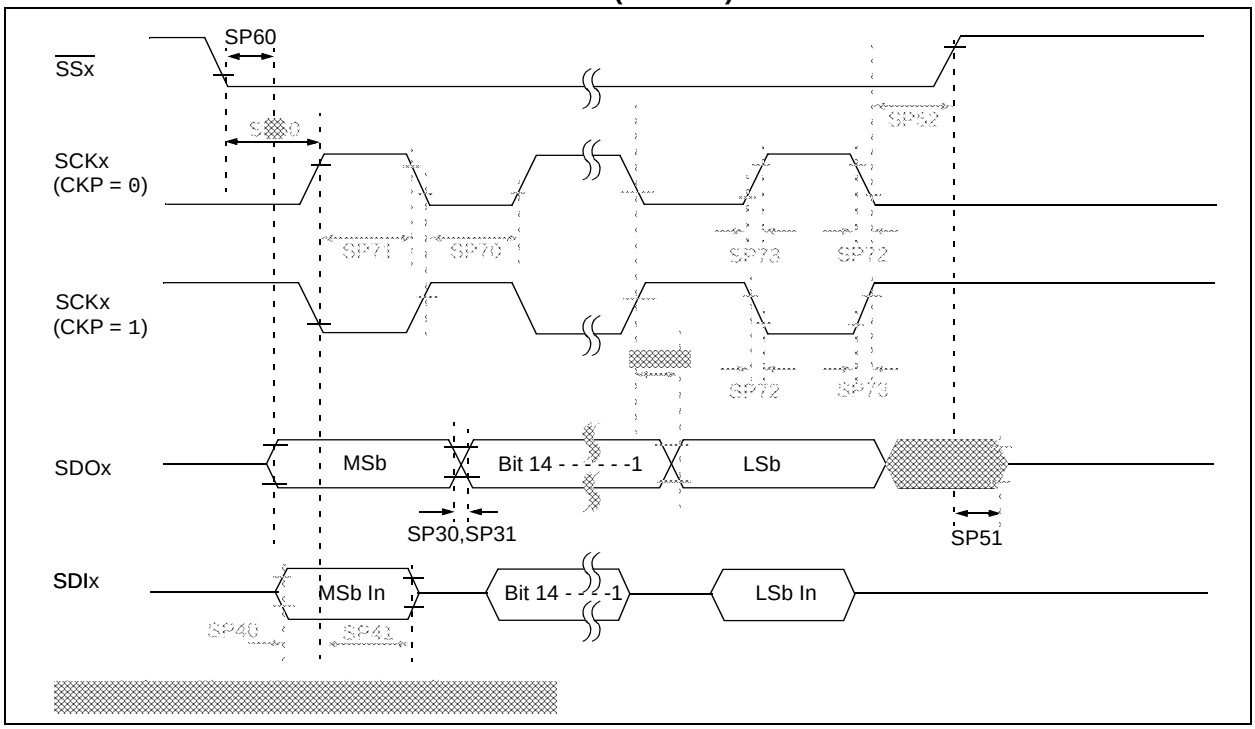


TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	—	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	10	ns	VDD > 2.7V
			—	—	15	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

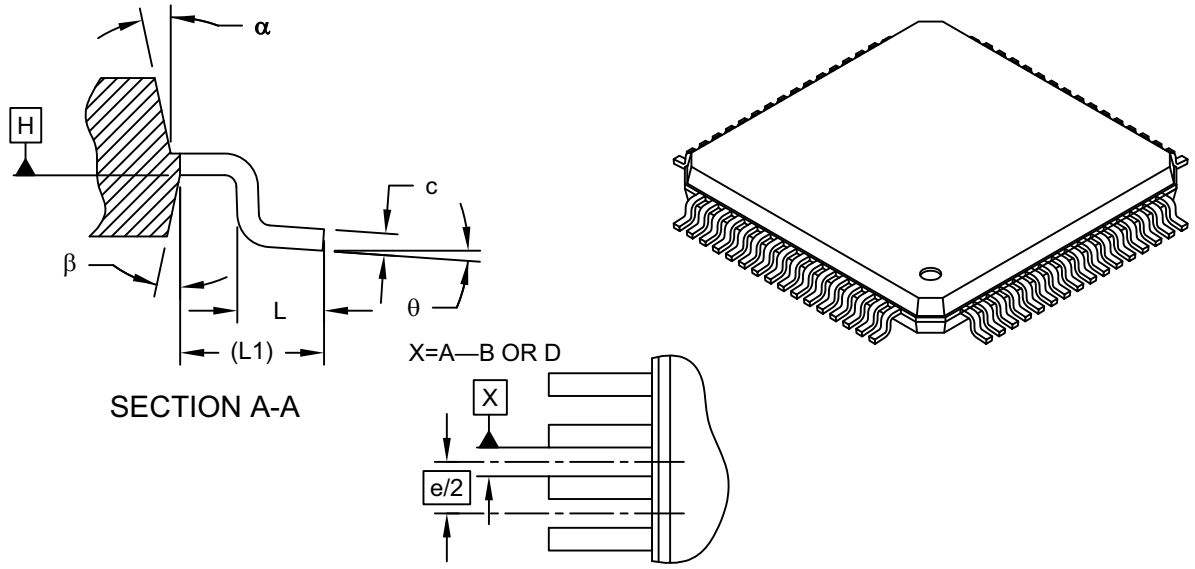
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 10 pF load on all SPIx pins.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

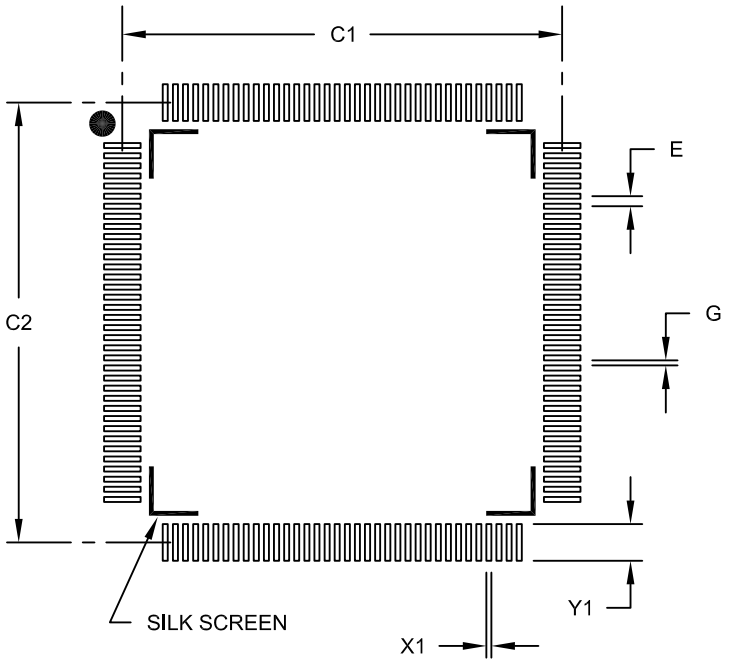
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

144-Lead Plastic Thin Quad Flat Pack (PH) - 16x16 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		17.40	
Contact Pad Spacing	C2		17.40	
Contact Pad Width (X144)	X1			0.20
Contact Pad Length (X144)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2155B