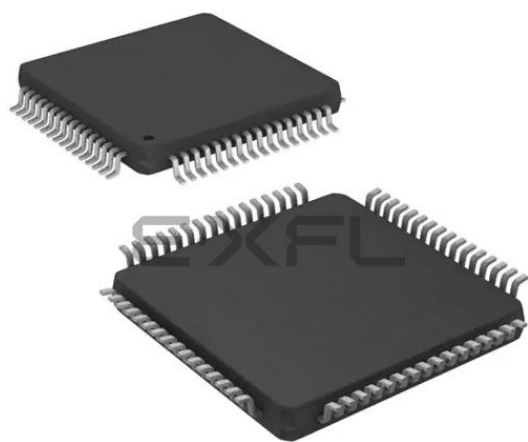




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecg064-i-pt

PIC32MZ Embedded Connectivity (EC) Family

Device Pin Tables

TABLE 2: PIN NAMES FOR 64-PIN DEVICES

64-PIN QFN ⁽⁴⁾ AND TQFP (TOP VIEW)			
PIC32MZ0512EC(E/F/K)064 PIC32MZ1024EC(G/H/M)064 PIC32MZ1024EC(E/F/K)064 PIC32MZ2048EC(G/H/M)064			
		64	1
		QFN ⁽⁴⁾	TQFP ¹
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN17/ETXEN/RPE5/PMD5/RE5	33	VBUS
2	AN16/ETXD0/PMD6/RE6	34	VUSB3V3
3	AN15/ETXD1/PMD7/RE7	35	Vss
4	AN14/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN13/C1INC/RPG7/SDA4/PMA4/RG7	37	D+
6	AN12/C2IND/RPG8/SCL4/PMA3/RG8	38	RPF3/USBID/RF3
7	Vss	39	VDD
8	VDD	40	Vss
9	MCLR	41	RPF4/SDA5/PMA9/RF4
10	AN11/C2INC/RPG9/PMA2/RG9	42	RPF5/SCL5/PMA8/RF5
11	AN45/C1INA/RPB5/RB5	43	AERXD0/ETXD2/RPD9/SDA1/PMCS2/PMA15/RD9
12	AN4/C1INB/RB4	44	ECOL/RPD10/SCL1/SCK4/RD10
13	AN3/C2INA/RPB3/RB3	45	AERXCLK/AEREFCLK/ECRS/RPD11/PMCS1/PMA14/RD11
14	AN2/C2INB/RPB2/RB2	46	AERXD1/ETXD3/RPD0/RTCC/INT0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN46/RPB6/RB6	49	EMDIO/AEMDIO/RPD1/SCK1/RD1
18	PGED2/AN47/RPB7/RB7	50	ETXERR/AETXEN/RPD2/SDA3/RD2
19	AVDD	51	AERXERR/ETXCLK/RPD3/SCL3/RD3
20	AVss	52	SQICS0/RPD4/PMWR/RD4
21	AN48/RPB8/PMA10/RB8	53	SQICS1/RPD5/PMRD/RD5
22	AN49/RPB9/PMA7/RB9	54	VDD
23	TMS/CVREFOUT/AN5/RPB10/PMA13/RB10	55	Vss
24	TDO/AN6/PMA12/RB11	56	ERXD3/AETXD1/RPF0/RF0
25	Vss	57	TRCLK/SQICLK/ERXD2/AETXD0/RPF1/RF1
26	VDD	58	TRD0/SQID0/ERXD1/PMD0/RE0
27	TCK/AN7/PMA11/RB12	59	Vss
28	TDI/AN8/RB13	60	VDD
29	AN9/RPB14/SCK3/PMA1/RB14	61	TRD1/SQID1/ERXD0/PMD1/RE1
30	AN10/EMDC/AEMDC/RPB15/OCFB/PMA0/RB15	62	TRD2/SQID2/ERXDV/ECRSDV/AECRSDV/PMD2/RE2
31	OSC1/CLK1/RC12	63	TRD3/SQID3/ERXCLK/EREFCLK/RPE3/PMD3/RE3
32	OSC2/CLK0/RC15	64	AN18/ERXERR/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 “Peripheral Pin Select (PPS)”** for restrictions.
 - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.
 - 4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

PIC32MZ Embedded Connectivity (EC) Family

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Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

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When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

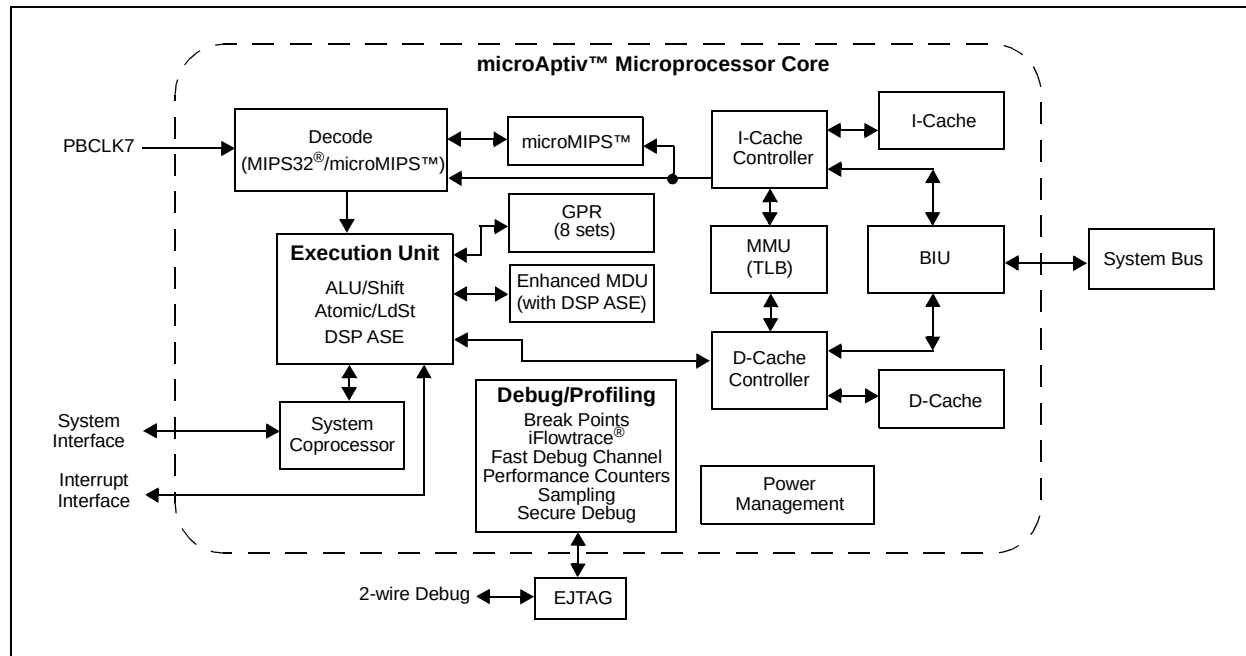
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PIC32MZ Embedded Connectivity (EC) Family

A block diagram of the PIC32MZ EC family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MZ EC FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



PIC32MZ Embedded Connectivity (EC) Family

6.0 RESETS

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS60001118), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM

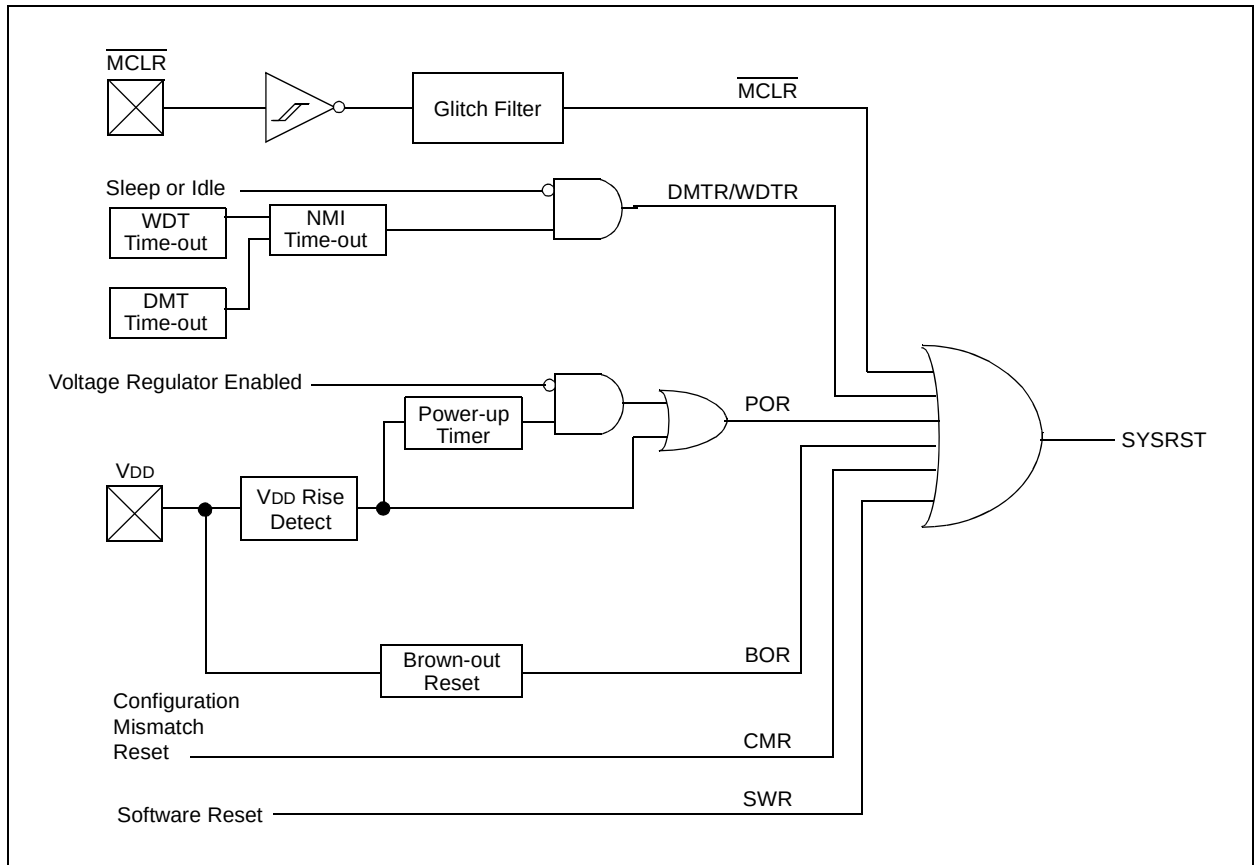


TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC1 Digital Comparator 3	_ADC1_DC3_VECTOR	48	OFF048<17:1>	IFS1<16>	IEC1<16>	IPC12<4:2>	IPC12<1:0>	Yes
ADC1 Digital Comparator 4	_ADC1_DC4_VECTOR	49	OFF049<17:1>	IFS1<17>	IEC1<17>	IPC12<12:10>	IPC12<9:8>	Yes
ADC1 Digital Comparator 5	_ADC1_DC5_VECTOR	50	OFF050<17:1>	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	Yes
ADC1 Digital Comparator 6	_ADC1_DC6_VECTOR	51	OFF051<17:1>	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	Yes
ADC1 Digital Filter 1	_ADC1_DF1_VECTOR	52	OFF052<17:1>	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	Yes
ADC1 Digital Filter 2	_ADC1_DF2_VECTOR	53	OFF053<17:1>	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
ADC1 Digital Filter 3	_ADC1_DF3_VECTOR	54	OFF054<17:1>	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
ADC1 Digital Filter 4	_ADC1_DF4_VECTOR	55	OFF055<17:1>	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes
ADC1 Digital Filter 5	_ADC1_DF5_VECTOR	56	OFF056<17:1>	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
ADC1 Digital Filter 6	_ADC1_DF6_VECTOR	57	OFF057<17:1>	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
Reserved	—	58	—	—	—	—	—	—
ADC1 Data 0	_ADC1_DATA0_VECTOR	59	OFF059<17:1>	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
ADC1 Data 1	_ADC1_DATA1_VECTOR	60	OFF060<17:1>	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
ADC1 Data 2	_ADC1_DATA2_VECTOR	61	OFF061<17:1>	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
ADC1 Data 3	_ADC1_DATA3_VECTOR	62	OFF062<17:1>	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	Yes
ADC1 Data 4	_ADC1_DATA4_VECTOR	63	OFF063<17:1>	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	Yes
ADC1 Data 5	_ADC1_DATA5_VECTOR	64	OFF064<17:1>	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	Yes
ADC1 Data 6	_ADC1_DATA6_VECTOR	65	OFF065<17:1>	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
ADC1 Data 7	_ADC1_DATA7_VECTOR	66	OFF066<17:1>	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
ADC1 Data 8	_ADC1_DATA8_VECTOR	67	OFF067<17:1>	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
ADC1 Data 9	_ADC1_DATA9_VECTOR	68	OFF068<17:1>	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
ADC1 Data 10	_ADC1_DATA10_VECTOR	69	OFF069<17:1>	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
ADC1 Data 11	_ADC1_DATA11_VECTOR	70	OFF070<17:1>	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
ADC1 Data 12	_ADC1_DATA12_VECTOR	71	OFF071<17:1>	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
ADC1 Data 13	_ADC1_DATA13_VECTOR	72	OFF072<17:1>	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
ADC1 Data 14	_ADC1_DATA14_VECTOR	73	OFF073<17:1>	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
ADC1 Data 15	_ADC1_DATA15_VECTOR	74	OFF074<17:1>	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	Yes

- Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EC Family Features”** for the list of available peripherals.
- 2:** This interrupt source is not available on 64-pin devices.
- 3:** This interrupt source is not available on 100-pin devices.
- 4:** This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81 #)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0718	OFF118 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
071C	OFF119	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0720	OFF120	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0724	OFF121	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0728	OFF122	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
072C	OFF123	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0730	OFF124	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0734	OFF125 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0738	OFF126 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
073C	OFF127 ^(2,4,8)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0740	OFF128	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0744	OFF129	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0748	OFF130	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
074C	OFF131	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0750	OFF132	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81 #)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0790	OFF148 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0794	OFF149 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0798	OFF150 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
079C	OFF151 ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07A0	OFF152 ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07A4	OFF153	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07A8	OFF154	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07AC	OFF155	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07B0	OFF156	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07B4	OFF157	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07B8	OFF158	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07BC	OFF159	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07C0	OFF160	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07C4	OFF161	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
07C8	OFF162	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
 - 2: This bit or register is not available on 64-pin devices.
 - 3: This bit or register is not available on devices without a CAN module.
 - 4: This bit or register is not available on 100-pin devices.
 - 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
 - 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
 - 7: This bit or register is not available on devices without a Crypto module.
 - 8: This bit or register is not available on 124-pin devices.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-29: USBLPMR2: USB LINK POWER MANAGEMENT CONTROL REGISTER 2

bit 0 **LPMSTIF:** LPM STALL Interrupt Flag bit

When in *Device mode*:
1 = A LPM transaction was received and the USB Module responded with a STALL
0 = No Stall condition

When in *Host mode*:
1 = A LPM transaction was transmitted and the device responded with a STALL
0 = No Stall condition

PIC32MZ Embedded Connectivity (EC) Family

12.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

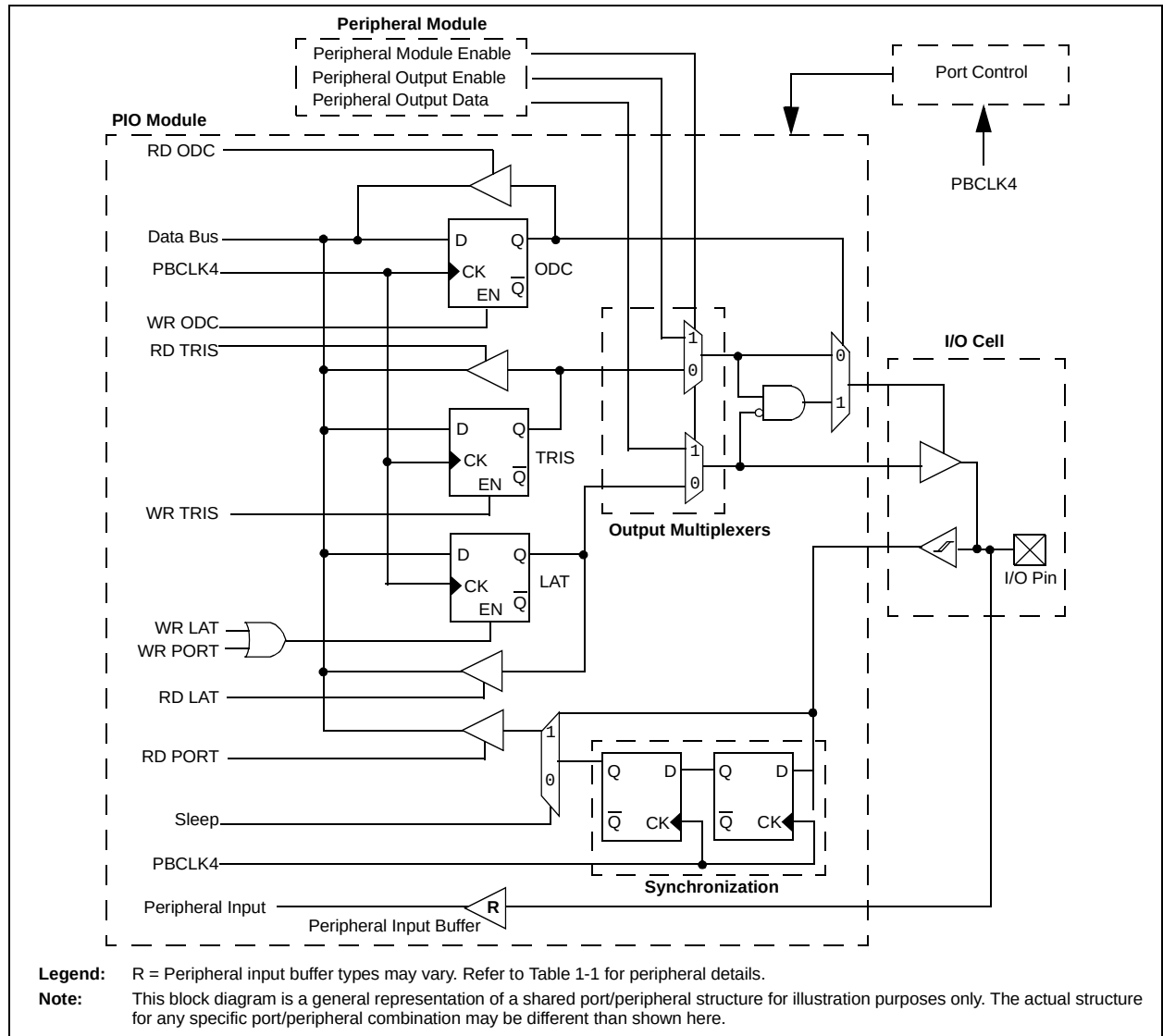
General purpose I/O pins are the simplest of peripherals. They allow the PIC32MZ EC family device to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Key features of the I/O ports include:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



PIC32MZ Embedded Connectivity (EC) Family

REGISTER 23-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0> ⁽¹⁾		WAITM<3:0> ⁽¹⁾				WAITE<1:0> ⁽¹⁾	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)

1 = Port is busy

0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

11 = Reserved, do not use

10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> = 11 (Addressable Slave mode only)

01 = Interrupt generated at the end of the read/write cycle

00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits

11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)

10 = Decrement ADDR<15:0> and ADDR<14> by 1 every read/write cycle⁽²⁾

01 = Increment ADDR<15:0> and ADDR<14> by 1 every read/write cycle⁽²⁾

00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit

1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer

0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits

11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<15:0>)⁽³⁾

10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, and PMD<15:0>)⁽³⁾

01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCSx, PMD<7:0>, and PMA<1:0>)

00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCSx, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits⁽¹⁾

11 = Data wait of 4 TPBCLK2; multiplexed address phase of 4 TPBCLK2

10 = Data wait of 3 TPBCLK2; multiplexed address phase of 3 TPBCLK2

01 = Data wait of 2 TPBCLK2; multiplexed address phase of 2 TPBCLK2

00 = Data wait of 1 TPBCLK2; multiplexed address phase of 1 TPBCLK2 (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK2 cycle for a write operation; WAITB = 1 TPBCLK2 cycle, WAITE = 0 TPBCLK2 cycles for a read operation.

2: Address bits 14 and 15 are not subject to auto-increment/decrement if configured as Chip Select.

3: The PMD<15:8> bits are not active if the MODE16 bit = 1.

PIC32MZ Embedded Connectivity (EC) Family

Figure 26-10 shows the Security Association control word structure.

The Crypto Engine fetches different structures for different flows and ensures that hardware fetches minimum words from SA required for processing. The structure is ready for hardware optimal data fetches.

FIGURE 26-10: FORMAT OF SA_CTRL

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	—	—	VERIFY	—	NO_RX	OR_EN	ICVONLY	IRFLAG
23-16	LNC	LOADIV	FB	FLAGS	—	—	—	ALGO<6>
15-8	ALGO<5:0>						ENC	KEY SIZE<1>
7-0	KEY SIZE<0>	MULTITASK<2:0>			CRYPTOALGO<3:0>			

bit 31-30 **Reserved:** Do not use

bit 29 **VERIFY:** NIST Procedure Verification Setting

1 = NIST procedures are to be used

0 = Do not use NIST procedures

bit 28 **Reserved:** Do not use

bit 27 **NO_RX:** Receive DMA Control Setting

1 = Only calculate ICV for authentication calculations

0 = Normal processing

bit 26 **OR_EN:** OR Register Bits Enable Setting

1 = OR the register bits with the internal value of the CSR register

0 = Normal processing

bit 25 **ICVONLY:** Incomplete Check Value Only Flag

This affects the SHA-1 algorithm only. It has no effect on the AES algorithm.

1 = Only three words of the HMAC result are available

0 = All results from the HMAC result are available

bit 24 **IRFLAG:** Immediate Result of Hash Setting

This bit is set when the immediate result for hashing is requested.

1 = Save the immediate result for hashing

0 = Do not save the immediate result

bit 23 **LNC:** Load New Keys Setting

1 = Load a new set of keys for encryption and authentication

0 = Do not load new keys

bit 22 **LOADIV:** Load IV Setting

1 = Load the IV from this Security Association

0 = Use the next IV

bit 21 **FB:** First Block Setting

This bit indicates that this is the first block of data to feed the IV value.

1 = Indicates this is the first block of data

0 = Indicates this is not the first block of data

bit 20 **FLAGS:** Incoming/Outgoing Flow Setting

1 = Security Association is associated with an outgoing flow

0 = Security Association is associated with an incoming flow

bit 19-17 **Reserved:** Do not use

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 28-4: AD1IMOD: ADC1 INPUT MODE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SH4ALT<1:0> ^(1,2)	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SH3ALT<1:0> ^(1,2)		SH2ALT<1:0> ^(1,2)		SH1ALT<1:0> ^(1,2)		SH0ALT<1:0> ^(1,2)	
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SH5MOD<1:0>		SH4MOD<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SH3MOD<1:0>		SH2MOD<1:0>		SH1MOD<1:0>		SH0MOD<1:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-26 **Unimplemented:** Read as '0'
- bit 25-24 **SH4ALT<1:0>:** Analog Input to Dedicated S&H 4 (SH4) Select bits^(1,2)
 11 = Reserved
 10 = Reserved
 01 = Alternate input AN49
 00 = Default Class 1 input AN4
- bit 23-22 **SH3ALT<1:0>:** Analog Input to Dedicated S&H 3 (SH3) Select bits^(1,2)
 11 = Reserved
 10 = Reserved
 01 = Alternate input AN48
 00 = Default Class 1 input AN3
- bit 21-20 **SH2ALT<1:0>:** Analog Input to Dedicated S&H 2 (SH2) Select bits^(1,2)
 11 = Reserved
 10 = Reserved
 01 = Alternate input AN47
 00 = Default Class 1 input AN2
- bit 19-18 **SH1ALT<1:0>:** Analog Input to Dedicated S&H 1 (SH1) Select bits^(1,2)
 11 = Reserved
 10 = Reserved
 01 = Alternate input AN46
 00 = Default Class 1 input AN1
- bit 17-16 **SH0ALT<1:0>:** Analog Input to Dedicated S&H 0 (SH0) Select bits^(1,2)
 11 = Reserved
 10 = Reserved
 01 = Alternate input AN45
 00 = Default Class 1 input AN0
- bit 15-12 **Unimplemented:** Read as '0'

- Note 1:** Alternate inputs are only available for Class 1 Inputs.
- 2:** When an alternate input is selected (SHxALT<1:0> ≠ 0), the data, status, and control registers for the default Class 1 input are still used. Selecting an alternate input changes the physical input source only.

TABLE 30-5: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2110	ETH FRMTXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMTXOKCNT<15:0>																0000
2120	ETH SCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SCOLFRMCNT<15:0>																0000
2130	ETH MCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MCOLFRMCNT<15:0>																0000
2140	ETH FRMRXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMRXOKCNT<15:0>																0000
2150	ETH FCSERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FCSERRCNT<15:0>																0000
2160	ETH ALGNERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALGNERRCNT<15:0>																0000
2200	EMAC1 CFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN	—	—	—	LOOPBACK	TXPAUSE	RXPAUSE	PASSALL	RXENABLE	0000
2210	EMAC1 CFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	EXCESS DFR	BP NOBKOFF	NOBKOFF	—	—	LONGPRE	PUREPRE	AUTOPAD	VLANPAD	PAD ENABLE	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX	4082
2220	EMAC1 IPGT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0012
2230	EMAC1 IPGR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	NB2BIPKTGP1<6:0>							—	NB2BIPKTGP2<6:0>							0C12
2240	EMAC1 CLRT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CWINDOW<5:0>							—	—	—	RETX<3:0>				370F
2250	EMAC1 MAXF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MACMAXF<15:0>																05EE
2260	EMAC1 SUPP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RESET RMII	—	—	SPEED RMII	—	—	—	—	—	—	—	—	1000
2270	EMAC1 TEST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	TESTBP	TESTPAUSE	SHRTQNTA	0000
2280	EMAC1 MCFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RESET MGMT	—	—	—	—	—	—	—	—	—	CLKSEL<3:0>				NOPRE	SCANINC	0020
2290	EMAC1 MCMD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCAN	READ	0000
22A0	EMAC1 MADR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PHYADDR<4:0>					—	—	—	REGADDR<4:0>					0100

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.
- 2: Reset values default to the factory programmed value.

TABLE 30-5: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
22B0	EMAC1 MWTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MWTD<15:0>															0000
22C0	EMAC1 MRDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MRDD<15:0>															0000
22D0	EMAC1 MIND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	LINKFAIL	NOTVALID	SCAN	MIIMBUSY	0000
2300	EMAC1 SA0 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	STNADDR6<7:0>							STNADDR5<7:0>							XXXX	
2310	EMAC1 SA1 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	STNADDR4<7:0>							STNADDR3<7:0>							XXXX	
2320	EMAC1 SA2 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	STNADDR2<7:0>							STNADDR1<7:0>							XXXX	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.
- 2: Reset values default to the factory programmed value.

32.1 Comparator Voltage Reference Control Registers

TABLE 32-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0E00	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 32-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	CVROE	CVRR	CVRSS	CVR<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit

1 = Module is enabled

Setting this bit does not affect other bits in the register.

0 = Module is disabled and does not consume current.

Clearing this bit does not affect the other bits in the register.

bit 14-7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** CVREFOUT Enable bit

1 = Voltage level is output on CVREFOUT pin

0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit

1 = 0 to 0.625 CVRSRC, with CVRSRC/24 step size

0 = 0.25 CVRSRC to 0.719 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit

1 = Comparator voltage reference source, $CVRSRC = (VREF+) - (VREF-)$

0 = Comparator voltage reference source, $CVRSRC = AVDD - AVSS$

bit 3-0 **CVR<3:0>:** CVREF Value Selection $0 \leq CVR<3:0> \leq 15$ bits

When CVRR = 1:

$CVREF = (CVR<3:0>/24) \cdot (CVRSRC)$

When CVRR = 0:

$CVREF = 1/4 \cdot (CVRSRC) + (CVR<3:0>/32) \cdot (CVRSRC)$

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-44: USB OTG ELECTRICAL SPECIFICATIONS

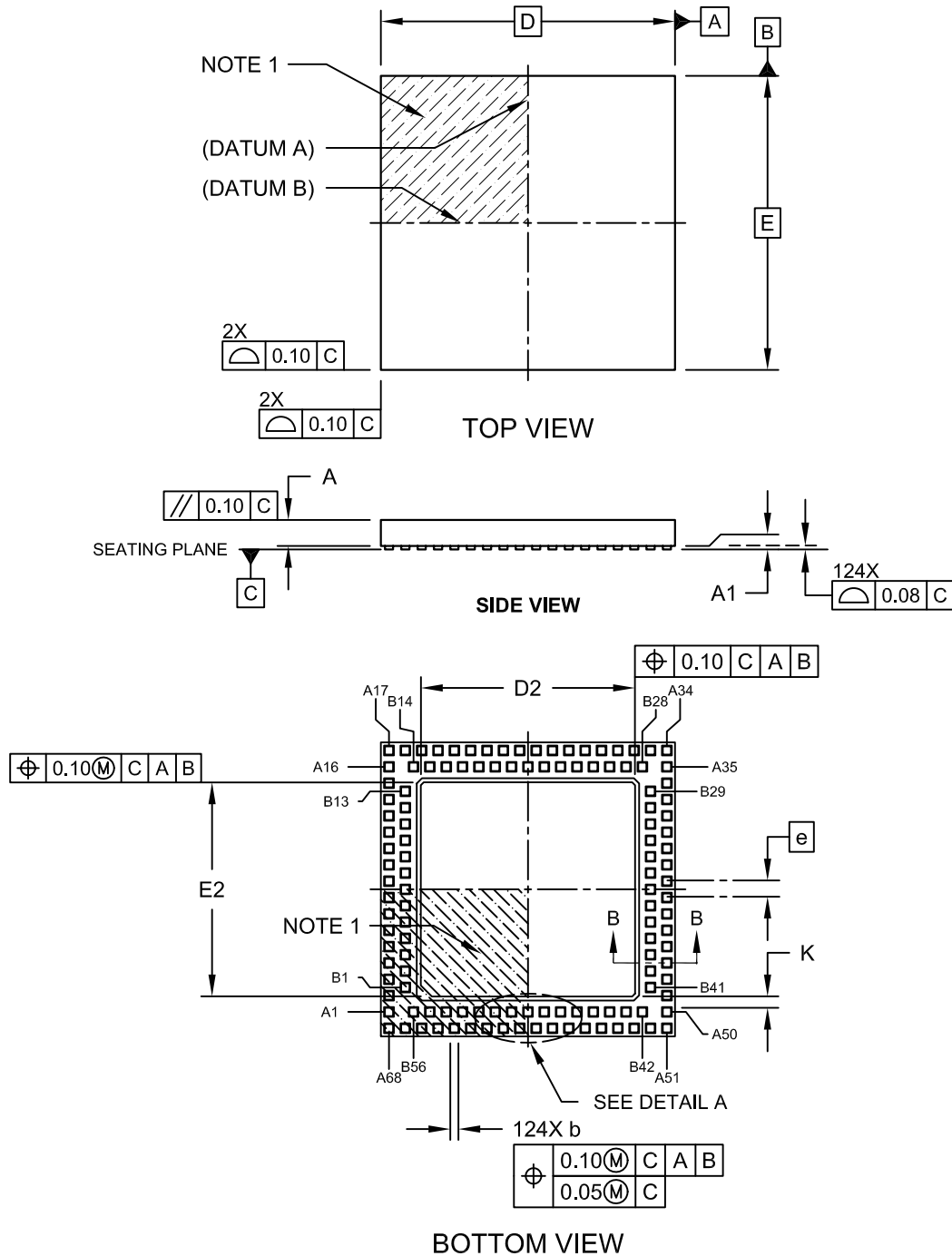
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
Low-Speed and Full-Speed Modes							
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	0.2	—	—	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB321	VoL	Voltage Output Low	0.0	—	0.3	V	1.425 k Ω load connected to VUSB3V3
USB322	VoH	Voltage Output High	2.8	—	3.6	V	14.25 k Ω load connected to ground
Hi-Speed Mode							
USB323	VHSDI	Differential input signal level	150	—	—	mV	—
USB324	VHSSQ	SQ detection threshold	100	—	150	mV	—
USB325	VHSCM	Common mode voltage range	-50	—	500	mV	—
USB326	VHSH	Data signaling high	360	—	440	mV	—
USB327	VHSL	Data signaling low	-10	—	10	mV	—
USB328	VCHIRPJ	Chirp J level	700	—	1100	mV	—
USB329	VCHIRPK	Chirp K level	-900	—	-500	mV	—
USB330	ZHSDRV	Driver output resistance	—	45	—	Ω	—

Note 1: These parameters are characterized, but not tested in manufacturing.

PIC32MZ Embedded Connectivity (EC) Family

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-193A Sheet 1 of 2

PIC32MZ Embedded Connectivity (EC) Family

Revision F (June 2016)

The Preliminary status was removed and minor typographical updates to text and formatting were incorporated.

This revision also includes the following changes, which are referenced by their respective chapter in Table B-6.

TABLE B-6: MAJOR SECTION UPDATES

Section Name	Update Description
7.0 “CPU Exceptions and Interrupt Controller”	The Cache Error microprocessor exception type was removed (see Table 7-1).
8.0 “Oscillator Configuration”	The bit value definitions for the PLLDIV<2:0> bits in the System PLL Control register were updated (see Register 8-3).
11.0 “Hi-Speed USB with On-The-Go (OTG)”	The VBUS bit value is updated (see Register 11-13)
37.0 “Electrical Characteristics”	The typical value and the units for parameter OS42 in the External Clock Timing Requirements were updated (see Table 37-17).
39.0 “Packaging Information”	The 64-pin QFN (MR) package drawings land pattern were updated.
Appendix A: “Migrating from PIC32MX5XX/6XX/7XX to PIC32MZ”	The Primary Oscillator Configuration section of the Oscillator Configuration Differences was updated (see Table A-1).

Revision G (December 2016)

A recommendation was added to the first page, indicating that the PIC32MZ Embedded Connectivity (EC) Family of devices are not recommended for use in new designs. Instead, the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family of devices should be used.

TABLE B-7: MAJOR SECTION UPDATES

Section Name	Update Description
4.0 “Memory Organization”	Updated Figure 4-1 through Figure 4-5

PIC32MZ Embedded Connectivity (EC) Family

INDEX

A

AC Characteristics	579
ADC Specifications	601
Analog-to-Digital Conversion Requirements	602
EJTAG Timing Requirements	612
Ethernet	608
Internal FRC Accuracy	582
Internal RC Accuracy	582
OTG Electrical Specifications	607
Parallel Master Port Read Requirements	605
Parallel Master Port Write	606
Parallel Master Port Write Requirements	606
Parallel Slave Port Requirements	604
PLL Clock Timing	581
Assembler	
MPASM Assembler	562

B

Block Diagrams	
Comparator I/O Operating Modes	521
Comparator Voltage Reference	525
CPU	48
Crypto Engine	383
DMA	165
Ethernet Controller	477
I2C Circuit	340
Input Capture	295
Interrupt Controller	113
JTAG Programming, Debugging and Trace Ports	557
Output Compare Module	299
PIC32 CAN Module	439
PMP Pinout and Connections to External Devices	355
Prefetch Module	161
Prefetch Module Block Diagram	161
Random Number Generator (RNG)	403
Reset System	107
RTCC	373
Serial Quad Interface (SQI)	315
SPI Module	305
Timer1	273
Timer2/3/4/5 (16-Bit)	277
Typical Multiplexed Port Structure	237
UART	347
WDT and Power-up Timer	291
Brown-out Reset (BOR)	
and On-Chip Voltage Regulator	557

C

C Compilers	
MPLAB C18	562
Comparator	
Specifications	578
Comparator Module	521
Comparator Voltage Reference (CVref)	525
Configuration Bit	535
Configuring Analog Port Pins	238
Controller Area Network (CAN)	439
CP0 Register 16, Select 1)	55
CP0 Register 16, Select 2)	57
CP0 Register 16, Select 3)	56
CPU	
Architecture Overview	49
Coprocessor 0 Registers	51

Core Exception Types	114
EJTAG Debug Support	53
Power Management	53
CPU Module	37, 47
Crypto Engine	383
Customer Change Notification Service	663
Customer Notification Service	663
Customer Support	663

D

DC Characteristics	566
I/O Pin Input Specifications	571, 573
I/O Pin Output Specifications	574
Idle Current (I _{IDLE})	569
Power-Down Current (I _{PD})	570
Program Memory	577
Temperature and Voltage Specifications	567
Development Support	561
Direct Memory Access (DMA) Controller	165

E

Electrical Characteristics	565
AC	579
Errata	12
Ethernet Controller	477
ETHPMM0 (Ethernet Controller Pattern Match Mask 0)	487
ETHPMM1 (Ethernet Controller Pattern Match Mask 1)	487
External Bus Interface (EBI)	365
External Clock	
Timer1 Timing Requirements	587
Timer2, 3, 4, 5 Timing Requirements	588
Timing Requirements	580

F

Flash Program Memory	97, 107
RTSP Operation	97

H

High-Voltage Detect (HVD)	109
---------------------------------	-----

I

I/O Ports	237
Parallel I/O (PIO)	238
Write/Read Timing	238
Input Change Notification	238
Instruction Set	559
Inter-Integrated Circuit (I2C)	339
Internet Address	663
Interrupt Controller	
IRG, Vector and Bit Location	116

M

Memory Maps	
Devices with 1024 KB Program Memory and 512 KB RAM	61, 62
Devices with 2048 KB Program Memory	63
Devices with 512 KB Program Memory	60
Memory Organization	59
Layout	59
Microchip Internet Web Site	663
MPLAB ASM30 Assembler, Linker, Librarian	562
MPLAB Integrated Development Environment Software	561
MPLAB PM3 Device Programmer	563
MPLAB REAL ICE In-Circuit Emulator System	563