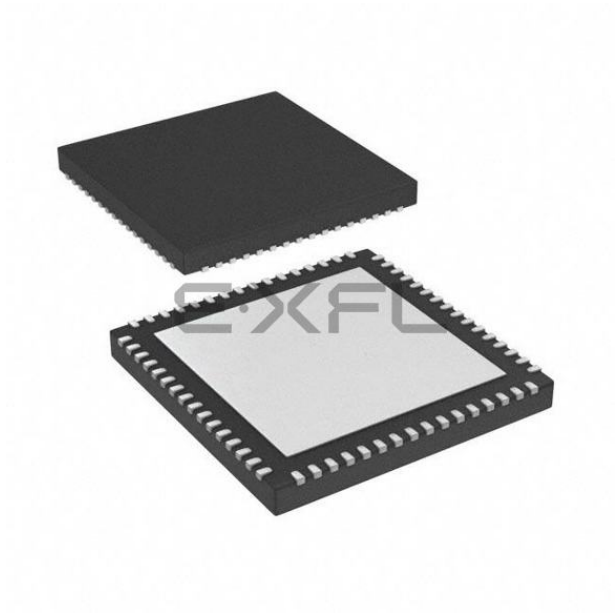
Microchip Technology - PIC32MZ2048ECG064T-I/MR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecg064t-i-mr

TABLE 1-16: ETHERNET MII I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
ERXD0	61	41	B32	81	I	ST	Ethernet Receive Data 0
ERXD1	58	42	B26	66	I	ST	Ethernet Receive Data 1
ERXD2	57	43	A31	67	I	ST	Ethernet Receive Data 2
ERXD3	56	44	A40	82	I	ST	Ethernet Receive Data 3
ERXERR	64	35	A30	65	I	ST	Ethernet Receive Error Input
ERXDV	62	12	B40	101	I	ST	Ethernet Receive Data Valid
ERXCLK	63	16	B12	27	I	ST	Ethernet Receive Clock
ETXD0	2	86	A5	7	O	—	Ethernet Transmit Data 0
ETXD1	3	85	B4	8	O	—	Ethernet Transmit Data 1
ETXD2	43	79	B17	43	O	—	Ethernet Transmit Data 2
ETXD3	46	80	A22	44	O	—	Ethernet Transmit Data 3
ETXERR	50	87	B44	114	O	—	Ethernet Transmit Error
ETXEN	1	77	A57	120	O	—	Ethernet Transmit Enable
ETXCLK	51	78	B47	121	I	ST	Ethernet Transmit Clock
ECOL	44	10	B33	83	I	ST	Ethernet Collision Detect
ECRS	45	11	A47	100	I	ST	Ethernet Carrier Sense
EMDC	30	70	B39	99	O	—	Ethernet Management Data Clock
EMDIO	49	71	A55	115	I/O	—	Ethernet Management Data

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-17: ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Ethernet MII Interface							
ERXD0	61	41	B32	81	I	ST	Ethernet Receive Data 0
ERXD1	58	42	B26	66	I	ST	Ethernet Receive Data 1
ERXERR	64	35	A30	65	I	ST	Ethernet Receive Error Input
ETXD0	2	86	A5	7	O	—	Ethernet Transmit Data 0
ETXD1	3	85	B4	8	O	—	Ethernet Transmit Data 1
ETXEN	1	77	A57	120	O	—	Ethernet Transmit Enable
EMDC	30	70	B39	99	O	—	Ethernet Management Data Clock
EMDIO	49	71	A55	115	I/O	—	Ethernet Management Data
EREFCLK	63	16	B12	27	I	ST	Ethernet Reference Clock
ECRSDV	62	12	B40	101	I	ST	Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

2.10.2 5V TOLERANT INPUT PINS

The internal high side diode on 5V tolerant pins are bussed to an internal floating node, rather than being connected to VDD, as shown in Figure 2-7. Voltages on these pins, if VDD < 2.3V, should not exceed roughly 3.2V relative to VSS of the PIC32 device. Voltage of 3.6V or higher will violate the absolute maximum specification, and will stress the oxide layer separating the high side floating node, which impacts device reliability. If a remotely powered "digital-only" signal can be guaranteed to always be ≤ 3.2V relative to Vss on the PIC32 device side, a 5V tolerant pin could be used without the need for a digital isolator. This is assuming there is not a ground loop issue, logic ground of the two circuits not at the same absolute level, and a remote logic low input is not less than VSS - 0.3V.

FIGURE 2-7: PIC32 5V TOLERANT PIN ARCHITECTURE EXAMPLE

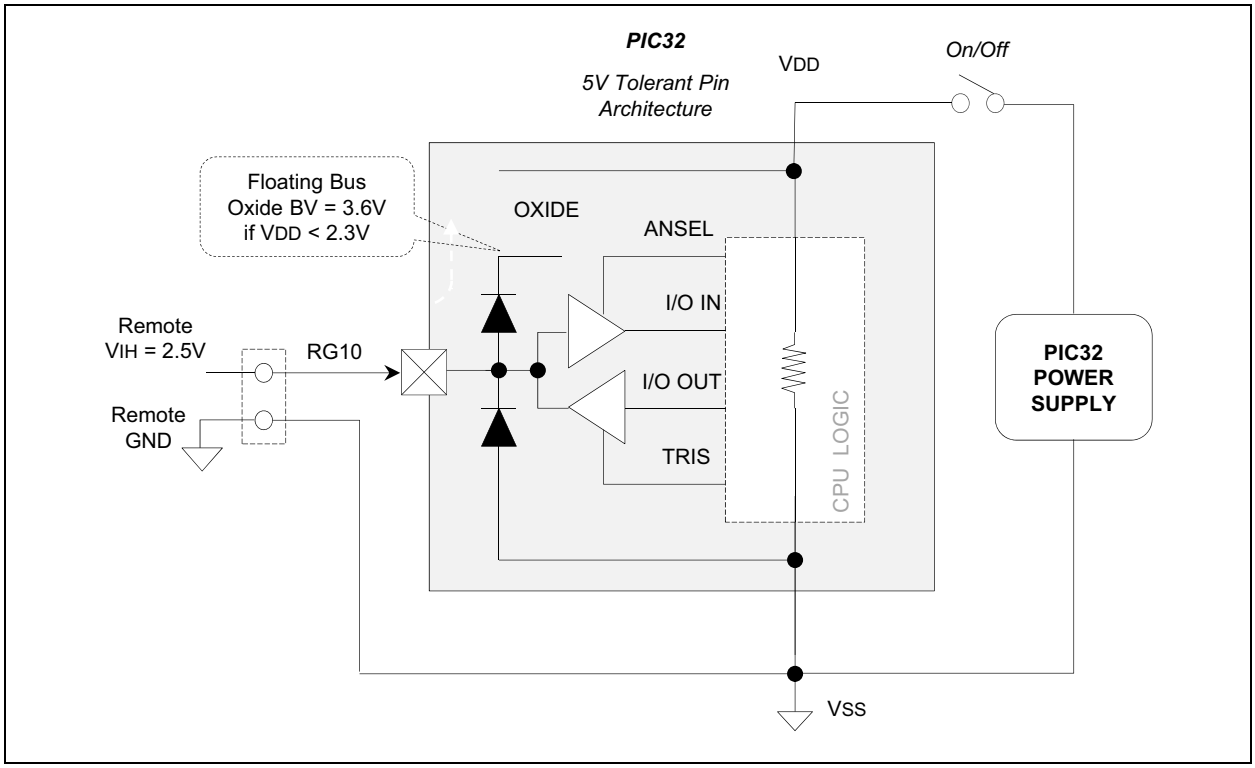
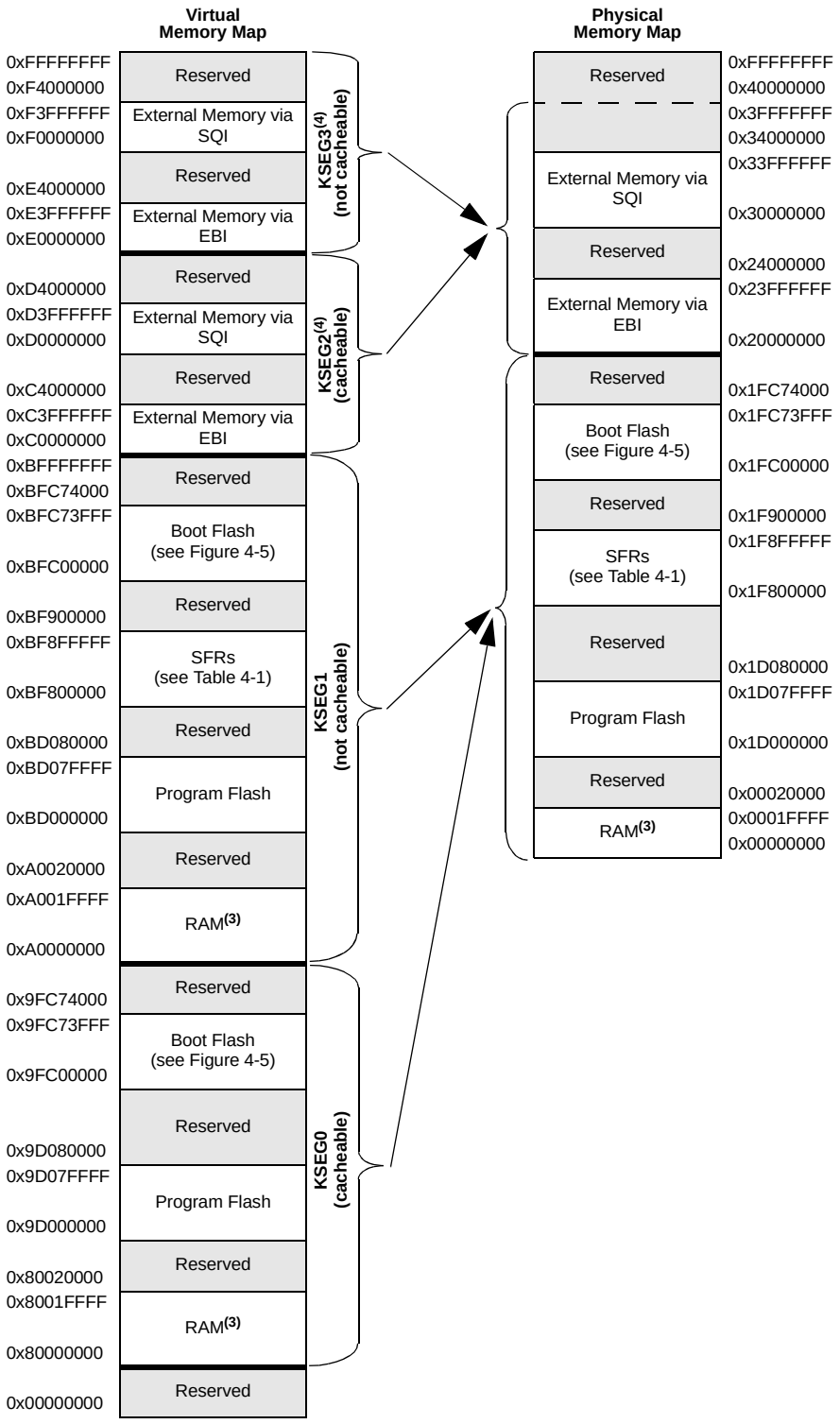


FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY(1,2)



Note 1: Memory areas are not shown to scale.
2: The Cache, MMU, and TLB are initialized by compiler start-up code.
3: RAM memory is divided into two equal banks: RAM Bank 1 and RAM Bank 2 on a half boundary.
4: The MMU must be enabled and the TLB must be set up to access this segment.

REGISTER 5-7: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	LBWPULOCK	—	—	LBWP4(1)	LBWP3(1)	LBWP2(1)	LBWP1(1)	LBWP0(1)
7:0	R/W-1	r-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	UBWPULOCK	—	—	UBWP4(1)	UBWP3(1)	UBWP2(1)	UBWP1(1)	UBWP0(1)

Legend:		r = Reserved	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **LBWPULOCK:** Lower Boot Alias Write-protect Unlock bit
1 = LBWPx bits are not locked and can be modified
0 = LBWPx bits are locked and cannot be modified
This bit is only clearable and cannot be set except by any reset.

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **LBWP4:** Lower Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC10000 through 0x1FC13FFF enabled
0 = Write protection for physical address 0x01FC10000 through 0x1FC13FFF disabled

bit 11 **LBWP3:** Lower Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC0C000 through 0x1FC0FFFF enabled
0 = Write protection for physical address 0x01FC0C000 through 0x1FC0FFFF disabled

bit 10 **LBWP2:** Lower Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC08000 through 0x1FC0BFFF enabled
0 = Write protection for physical address 0x01FC08000 through 0x1FC0BFFF disabled

bit 9 **LBWP1:** Lower Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC04000 through 0x1FC07FFF enabled
0 = Write protection for physical address 0x01FC04000 through 0x1FC07FFF disabled

bit 8 **LBWP0:** Lower Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC00000 through 0x1FC03FFF enabled
0 = Write protection for physical address 0x01FC00000 through 0x1FC03FFF disabled

bit 7 **UBWPULOCK:** Upper Boot Alias Write-protect Unlock bit
1 = UBWPx bits are not locked and can be modified
0 = UBWPx bits are locked and cannot be modified
This bit is only user-clearable and cannot be set except by any reset.

bit 6 **Reserved:** This bit is reserved for use by development tools

bit 5 **Unimplemented:** Read as '0'

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.

8.2 Oscillator Control Registers

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1200	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			DRMEN	SOSCRDY	—	—	—	—	—	—	0000
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK	SLOCK	SLPEN	CF	—	SOSCEN	OSWEN	xx0x
1210	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
1220	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>							01xx
		15:0	—	—	—	—	—	PLLIDIV<2:0>			PLLICLK	—	—	—	—	PLLRANGE<2:0>			0x0x
1280	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
1290	REFO1TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12A0	REFO2CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12B0	REFO2TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12C0	REFO3CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12D0	REFO3TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12E0	REFO4CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12F0	REFO4TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1300	PB1DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1310	PB2DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1320	PB3DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1330	PB4DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1340	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1360	PB7DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1370	PB8DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

TABLE 11-1: USB REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3170	USB E7CSR0	31:16	Indexed by the same bits in USBIE7CSR0																0000
		15:0																	0000
3174	USB E7CSR1	31:16	Indexed by the same bits in USBIE7CSR1																0000
		15:0																	0000
3178	USB E7CSR2	31:16	Indexed by the same bits in USBIE7CSR2																0000
		15:0																	0000
317C	USB E7CSR3	31:16	Indexed by the same bits in USBIE7CSR3																0000
		15:0																	0000
3200	USB DMAINT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DMA8IF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF	0000
3204	USB DMA1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3208	USB DMA1A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
320C	USB DMA1N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3214	USB DMA2C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3218	USB DMA2A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
321C	USB DMA2N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3224	USB DMA3C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3228	USB DMA3A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
322C	USB DMA3N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3234	USB DMA4C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3238	USB DMA4A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
323C	USB DMA4N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3244	USB DMA5C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2 (CONTINUED)

bit 19 **SOFIF:** Start of Frame Interrupt bit
1 = A new frame has started
0 = No start of frame detected

bit 18 **RESETIF:** Reset/Babble Interrupt bit
1 = In *Host mode*, indicates babble is detected. In *Device mode*, indicates reset signaling is detected on the bus.
0 = No reset/babble detected

bit 17 **RESUMEIF:** Resume Interrupt bit
1 = Resume signaling is detected on the bus while USB module is in Suspend mode
0 = No Resume signaling detected

bit 16 **SUSPIF:** Suspend Interrupt bit
1 = Suspend signaling is detected on the bus *(Device mode)*
0 = No suspend signaling detected

bit 15-8 **Unimplemented:** Read as '0'

bit 7-1 **EP7RXIE:EP1RXIE:** Endpoint 'n' Receive Interrupt Enable bit
1 = Receive interrupt is enabled for this endpoint
0 = Receive interrupt is not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 11-10: USBIENCSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXINTERV<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			
15:8	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	RXCNT<13:8>					
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXCNT<7:0>							

Legend:	HC = Hardware Clearable	HS = Hardware Settable	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **TXINTERV<7:0>:** Endpoint TX Polling Interval/NAK Limit bits (*Host mode*)

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and interpretation for these bits:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low/Full	0x01 to 0xFF	Polling interval is 'm' frames.
	High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames.
Isochronous	Full or High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames/microframes.
Bulk	Full or High	0x02 to 0x10	NAK limit is $2^{(m-1)}$ frames/microframes. A value of '0' or '1' disables the NAK time-out function.

bit 23-22 **SPEED<1:0>:** TX Endpoint Operating Speed Control bits (*Host mode*)
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-20 **PROTOCOL<1:0>:** TX Endpoint Protocol Control bits
11 = Interrupt
10 = Bulk
01 = Isochronous
00 = Control

bit 19-16 **TEP<3:0>:** TX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **RXCNT<13:0>:** Receive Count bits

The number of received data bytes in the endpoint RX FIFO. The value returned changes as the contents of the FIFO change and is only valid while RXPKTRDY is set.

REGISTER 20-18: SQI1BDPOLLCON: SQI BUFFER DESCRIPTOR POLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **POLLCON<15:0>:** Buffer Descriptor Processor Poll Status bits
These bits indicate the number of cycles the BDP block would wait before refetching the descriptor control word if the previous descriptor fetched was disabled.

REGISTER 20-19: SQI1BDTXDSTAT: SQI BUFFER DESCRIPTOR DMA TRANSMIT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	TXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	TXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	TXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **TXSTATE<3:0>:** Current DMA Transmit State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **TXCURBUFLEN<7:0>:** Current DMA Transmit Buffer Length Status bits
These bits provide the length of the current DMA transmit buffer.

REGISTER 20-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCURBUFLEN<7:0>:** Current DMA Receive Buffer Length Status bits
These bits provide the length of the current DMA receive buffer.

REGISTER 25-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

bit 10-9 **RTCCLKSEL<1:0>:** RTCC Clock Select bits

When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

11 = Reserved
10 = Reserved
01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)
00 = RTCC uses the internal 32 kHz oscillator (LPRC)

bit 8-7 **RTCOUTSEL<1:0>:** RTCC Output Data Select bits(2)

11 = Reserved
10 = RTCC Clock is presented on the RTCC pin
01 = Seconds Clock is presented on the RTCC pin
00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit(5)

1 = RTCC Clock is actively running
0 = RTCC Clock is not running

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **RTCWREN:** Real-Time Clock Value Registers Write Enable bit(3)

1 = Real-Time Clock Value registers can be written to by the user
0 = Real-Time Clock Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** Real-Time Clock Value Registers Read Synchronization bit

1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = Real-time clock value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(4)

1 = Second half period of a second
0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit

1 = RTCC output is enabled
0 = RTCC output is not enabled

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).
5: This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

Note:	This register is reset only on a Power-on Reset (POR).

REGISTER 25-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN(1,2)	CHIME(2)	PIV(2)	ALRMSYNC	AMASK<3:0>(2)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit(1,2)
- 1 = Alarm is enabled
- 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)
- 1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit
- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing.
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is more than 32 real-time clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(2)
- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved
- 1011 = Reserved
- 11xx = Reserved

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note: This register is reset only on a Power-on Reset (POR).

REGISTER 28-4: AD1IMOD: ADC1 INPUT MODE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SH4ALT<1:0>(1,2)	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SH3ALT<1:0>(1,2)		SH2ALT<1:0>(1,2)		SH1ALT<1:0>(1,2)		SH0ALT<1:0>(1,2)	
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SH5MOD<1:0>		SH4MOD<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SH3MOD<1:0>		SH2MOD<1:0>		SH1MOD<1:0>		SH0MOD<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-24 **SH4ALT<1:0>:** Analog Input to Dedicated S&H 4 (SH4) Select bits(1,2)
- 11 = Reserved
- 10 = Reserved
- 01 = Alternate input AN49
- 00 = Default Class 1 input AN4

bit 23-22 **SH3ALT<1:0>:** Analog Input to Dedicated S&H 3 (SH3) Select bits(1,2)
- 11 = Reserved
- 10 = Reserved
- 01 = Alternate input AN48
- 00 = Default Class 1 input AN3

bit 21-20 **SH2ALT<1:0>:** Analog Input to Dedicated S&H 2 (SH2) Select bits(1,2)
- 11 = Reserved
- 10 = Reserved
- 01 = Alternate input AN47
- 00 = Default Class 1 input AN2

bit 19-18 **SH1ALT<1:0>:** Analog Input to Dedicated S&H 1 (SH1) Select bits(1,2)
- 11 = Reserved
- 10 = Reserved
- 01 = Alternate input AN46
- 00 = Default Class 1 input AN1

bit 17-16 **SH0ALT<1:0>:** Analog Input to Dedicated S&H 0 (SH0) Select bits(1,2)
- 11 = Reserved
- 10 = Reserved
- 01 = Alternate input AN45
- 00 = Default Class 1 input AN0

bit 15-12 **Unimplemented:** Read as '0'

Note 1: Alternate inputs are only available for Class 1 Inputs.

2: When an alternate input is selected (SHxALT<1:0> ≠ 0), the data, status, and control registers for the default Class 1 input are still used. Selecting an alternate input changes the physical input source only.

REGISTER 29-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN27	MSEL27<1:0>		FSEL27<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN26	MSEL26<1:0>		FSEL26<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN25	MSEL25<1:0>		FSEL25<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN24	MSEL24<1:0>		FSEL24<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN27:** Filter 27 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL27<1:0>:** Filter 27 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL27<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN26:** Filter 26 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL26<1:0>:** Filter 26 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL26<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

bit 6 **VLANPAD:** VLAN Pad Enable bit(1,2)
1 = The MAC will pad all short frames to 64 bytes and append a valid CRC
0 = The MAC does not perform padding of short frames

bit 5 **PADENABLE:** Pad/CRC Enable bit(1,3)
1 = The MAC will pad all short frames
0 = The frames presented to the MAC have a valid length

bit 4 **CRCENABLE:** CRC Enable1 bit
1 = The MAC will append a CRC to every frame whether padding was required or not. Must be set if the PADENABLE bit is set.
0 = The frames presented to the MAC have a valid CRC

bit 3 **DELAYCRC:** Delayed CRC bit
This bit determines the number of bytes, if any, of proprietary header information that exist on the front of the IEEE 802.3 frames.
1 = Four bytes of header (ignored by the CRC function)
0 = No proprietary header

bit 2 **HUGEFRM:** Huge Frame enable bit
1 = Frames of any length are transmitted and received
0 = Huge frames are not allowed for receive or transmit

bit 1 **LENGTHCK:** Frame Length checking bit
1 = Both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the transmit/receive statistics vector.
0 = Length/Type field check is not performed

bit 0 **FULLDPLX:** Full-Duplex Operation bit
1 = The MAC operates in Full-Duplex mode
0 = The MAC operates in Half-Duplex mode

Note 1: Table 30-6 provides a description of the pad function based on the configuration of this register.
2: This bit is ignored if the PADENABLE bit is cleared.
3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note:	Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

TABLE 30-6: PAD OPERATION

Type	AUTOPAD	VLANPAD	PADENABLE	Action
Any	x	x	0	No pad, check CRC
Any	0	0	1	Pad to 60 Bytes, append CRC
Any	x	1	1	Pad to 64 Bytes, append CRC
Any	1	0	1	If untagged: Pad to 60 Bytes, append CRC If VLAN tagged: Pad to 64 Bytes, append CRC

31.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

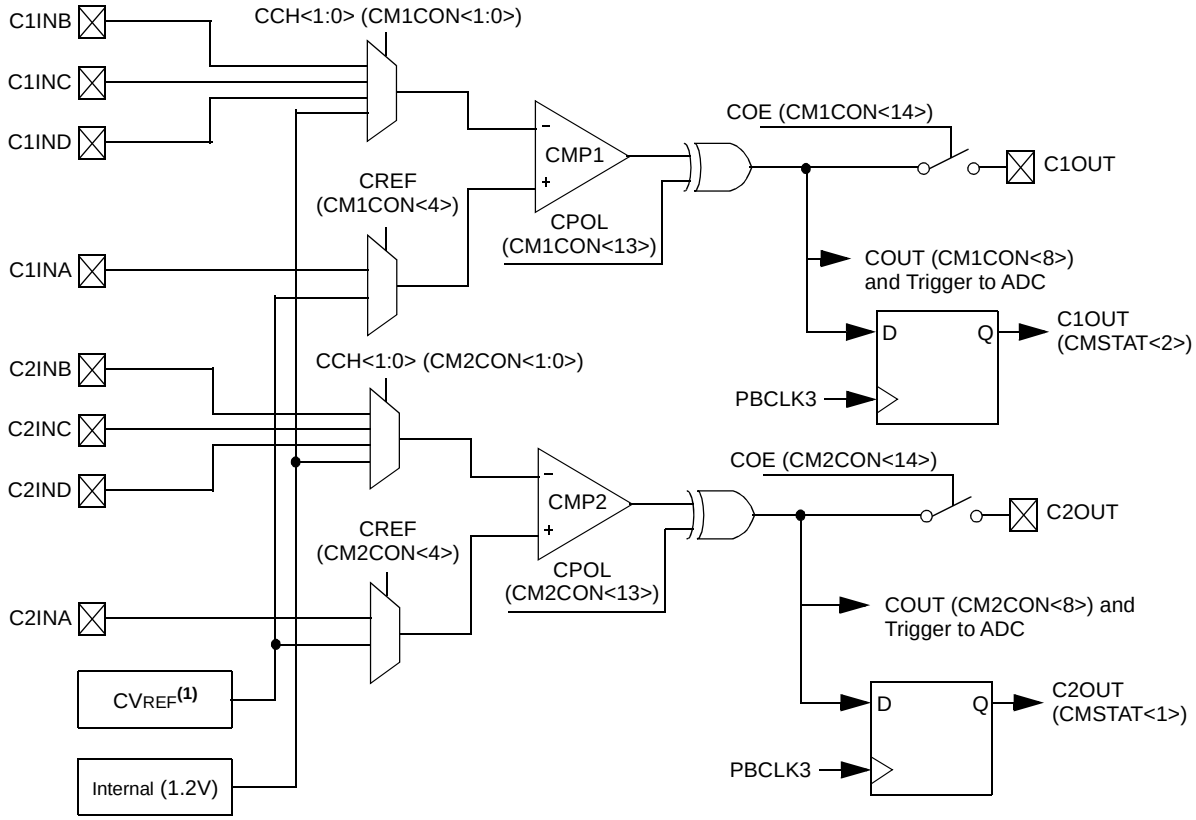
The Analog Comparator module consists of two comparators that can be configured in a variety of ways.

Key features of the Analog Comparator module are:

- Differential inputs
- Rail-to-rail operation
- Selectable output polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference
  - Comparator voltage reference (CV_{REF})
- Selectable interrupt generation

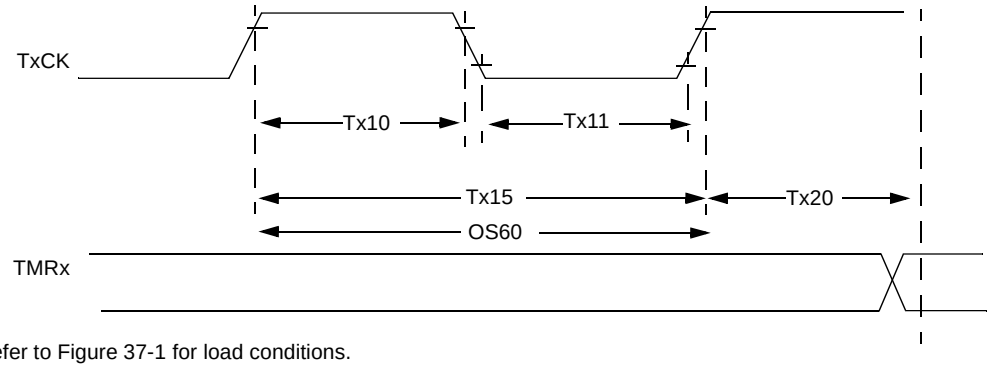
A block diagram of the comparator module is illustrated in Figure 31-1.

FIGURE 31-1: COMPARATOR BLOCK DIAGRAM



Note 1: Internally connected. See **Section 32.0 "Comparator Voltage Reference (CV_{REF})"** for more information.

FIGURE 37-6: TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 37-1 for load conditions.

TABLE 37-25: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(2)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 20 ns or 2 TPBCLK3)/N] + 30 ns	—	—	ns	VDD > 2.7V (**Note 3**)
				[(Greater of 20 ns or 2 TPBCLK3)/N] + 50 ns	—	—	ns	VDD < 2.7V (**Note 3**)
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V
				50	—	—	ns	VDD < 2.7V
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	50	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPBCLK3	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 2)**	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 2)**	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

TABLE 37-38: ADC1 MODULE SPECIFICATIONS

AC CHARACTERISTICS(5,6)			Standard Operating Conditions (see Notes 3,5): 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.3	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.2	—	AVDD	V	VREFH = VREF+ (**Note 1**)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 1.2	V	(**Note 1**)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	1.2	—	AVDD	V	(**Note 4**)
AD08 AD08a	IREF	Current Drain	— —	100 .002	150 1	µA µA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Range	– VREFH 0	— —	VREFH + VREFH	V V	Differential Single-ended
AD14	VINCM	Common Mode Input Voltage	AVSS + VREF/2	—	AVDD – VREF/2	V	—
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	200	Ω	(**Note 1**) For minimum sampling time
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Nonlinearity	—	±2	—	LSb	VINL = VREF- = VREFL = 0V, VREF+ = VREFH = 2.5V
AD22c	DNL	Differential Nonlinearity	—	±2	—	LSb	VINL = VREF- = VREFL = 0V, VREF+ = VREFH = 2.5V
AD23c	GERR	Gain Error	—	±8	—	LSb	VINL = VREF- = VREFL = 0V, VREF+ = VREFH = 2.5V
AD24c	EOFF	Offset Error	—	±10	—	LSb	VINL = VREF- = 0V, AVDD = 2.5V
AD25e	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	48	—	> 54	dB	(**Note 2**)
AD34b	ENOB	Effective Number of bits	8	—	9	bits	(**Note 2**)

Note 1: These parameters are not characterized or tested in manufacturing.

2: Characterized with a 1 kHz sine wave.

3: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

4: The BOOST (AD1CON2<6>) bit must be set to '1' when VREF ≤ 1.8V.

5: Specifications are based on adherence to the requirements listed in **28.1 "ADC Configuration Requirements"**.

6: External precision VREF+ and VREF- must be used at all times.