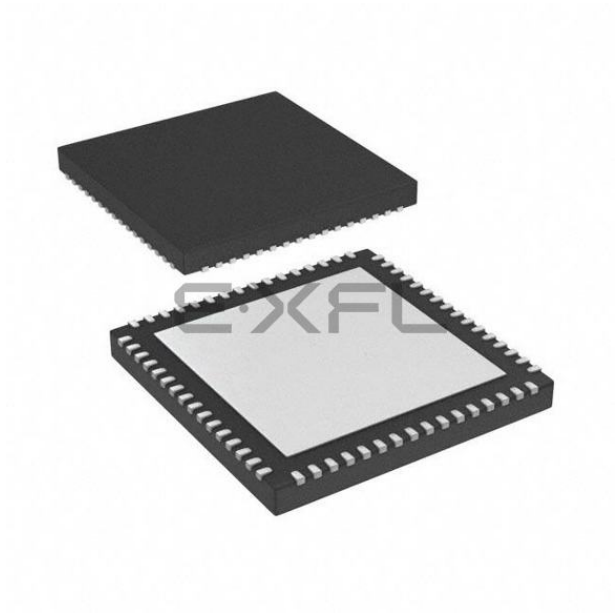
Microchip Technology - PIC32MZ2048ECH064T-I/MR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ech064t-i-mr

NOTES:

TABLE 4-3: BOOT FLASH 2 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC6_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF2DEVCFG3	31:0	**Note:** See Table 34-2 for the bit descriptions.																xxxx
FF44	ABF2DEVCFG2	31:0																	xxxx
FF48	ABF2DEVCFG1	31:0																	xxxx
FF4C	ABF2DEVCFG0	31:0																	xxxx
FF50	ABF2DEVCP3	31:0																	xxxx
FF54	ABF2DEVCP2	31:0																	xxxx
FF58	ABF2DEVCP1	31:0																	xxxx
FF5C	ABF2DEVCP0	31:0																	xxxx
FF60	ABF2DEVSIGN3	31:0																	xxxx
FF64	ABF2DEVSIGN2	31:0																	xxxx
FF68	ABF2DEVSIGN1	31:0																	xxxx
FF6C	ABF2DEVSIGN0	31:0																	xxxx
FF70	ABF2SEQ3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF74	ABF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF78	ABF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF7C	ABF2SEQ0	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFC0	BF2DEVCFG3	31:0	**Note:** See Table 34-1 for the bit descriptions.																xxxx
FFC4	BF2DEVCFG2	31:0																	xxxx
FFC8	BF2DEVCFG1	31:0																	xxxx
FFCC	BF2DEVCFG0	31:0																	xxxx
FFD0	BF2DEVCP3	31:0																	xxxx
FFD4	BF2DEVCP2	31:0																	xxxx
FFD8	BF2DEVCP1	31:0																	xxxx
FFDC	BF2DEVCP0	31:0																	xxxx
FFE0	BF2DEVSIGN3	31:0																	xxxx
FFE4	BF2DEVSIGN2	31:0																	xxxx
FFE8	BF2DEVSIGN1	31:0																	xxxx
FFEC	BF2DEVSIGN0	31:0																	xxxx
FFF0	BF2SEQ3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFF4	BF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFF8	BF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFFC	BF2SEQ0	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

REGISTER 4-4: SBTxELOG2: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 2 ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	GROUP<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-3 **Unimplemented:** Read as '0'

bit 1-0 **GROUP<1:0>:** Requested Permissions Group bits
11 = Group 3
10 = Group 2
01 = Group 1
00 = Group 0

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-5: SBTxECON: SYSTEM BUS TARGET 'x' ERROR CONTROL REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ERRP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ERRP:** Error Control bit
1 = Report protection group violation errors
0 = Do not report protection group violation errors

bit 23-0 **Unimplemented:** Read as '0'

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0568	OFF010	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
056C	OFF011	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0570	OFF012	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0574	OFF013	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0578	OFF014	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
057C	OFF015	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0580	OFF016	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0584	OFF017	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0588	OFF018	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
058C	OFF019	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0590	OFF020	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0594	OFF021	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0598	OFF022	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
059C	OFF023	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05A0	OFF024	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0718	OFF118(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
071C	OFF119	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0720	OFF120	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0724	OFF121	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0728	OFF122	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
072C	OFF123	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0730	OFF124	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0734	OFF125(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0738	OFF126(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
073C	OFF127(2,4,8)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0740	OFF128	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0744	OFF129	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0748	OFF130	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
074C	OFF131	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0750	OFF132	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 7-3: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	SRIPL<2:0>		
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SIRQ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits for Single Vector Mode bits
111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits
11111111-00000000 = The last interrupt request number serviced by the CPU

REGISTER 7-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits
Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

TABLE 12-2: OUTPUT PIN SELECTION (CONTINUED)

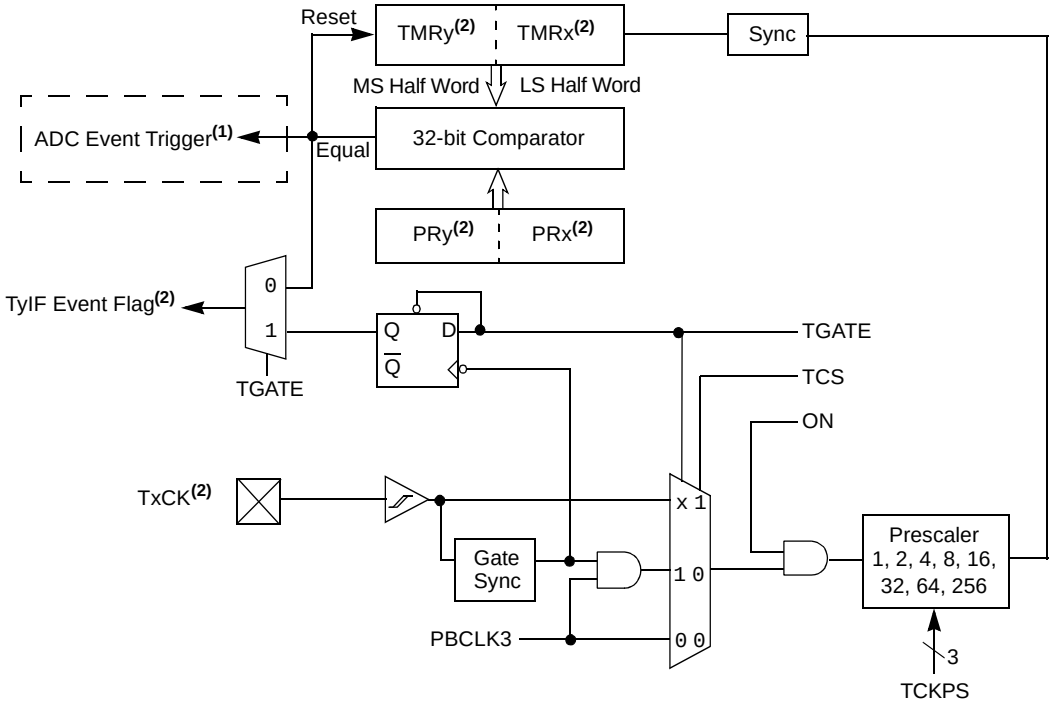
RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD1	RPD1R	RPD1R<3:0>	0000 = No Connect 0001 = U1RTS 0010 = U2TX 0011 = U5RTS 0100 = U6TX 0101 = Reserved 0110 = SS2 0111 = Reserved 1000 = SDO4 1001 = Reserved 1010 = SDO6(1) 1011 = OC2 1100 = OC1 1101 = OC9 1110 = Reserved 1111 = C2TX(3)
RPG9	RPG9R	RPG9R<3:0>	
RPB14	RPB14R	RPB14R<3:0>	
RPD0	RPD0R	RPD0R<3:0>	
RPB6	RPB6R	RPB6R<3:0>	
RPD5	RPD5R	RPD5R<3:0>	
RPB2	RPB2R	RPB2R<3:0>	
RPF3	RPF3R	RPF3R<3:0>	
RPF13(1)	RPF13R(1)	RPF13R<3:0>(1)	
RPC2(1)	RPC2R(1)	RPC2R<3:0>(1)	
RPE8(1)	RPE8R(1)	RPE8R<3:0>(1)	
RPF2(1)	RPF2R(1)	RPF2R<3:0>(1)	

Note 1: This selection is not available on 64-pin devices.

2: This selection is not available on 64-pin or 100-pin devices.

3: This selection is not available on devices without a CAN module.

FIGURE 14-2: TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9 BLOCK DIAGRAM (32-BIT)



Note 1: ADC event trigger is available only on the Timer2/3 and TImer4/5 pairs.
2: In this diagram, 'x' represents Timer2, 4, 6, or 8, and 'y' represents Timer3, 5, 7, or 9.

REGISTER 24-4: EBIFTRPD: EXTERNAL BUS INTERFACE FLASH TIMING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	TRPD<11:8>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRPD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-0 **TRPD<11:0>:** Flash Timing bits

These bits define the number of clock cycles to wait after resetting the external Flash memory before any read/write access.

REGISTER 25-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CAL<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAL<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	—	—	RTCCLKSEL<1:0>		RTC OUTSEL<1>(2)
7:0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0
	RTC OUTSEL<0>(2)	RTC CLKON(5)	—	—	RTC WREN(3)	RTC SYNC	HALFSEC(4)	RTCOE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** Real-Time Clock Drift Calibration bits, which contain a signed 10-bit integer value
0111111111 = Maximum positive adjustment, adds 511 real-time clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 real-time clock pulse every one minute
0000000000 = No adjustment
1111111111 = Minimum negative adjustment, subtracts 1 real-time clock pulse every one minute
•
•
•
1000000000 = Maximum negative adjustment, subtracts 512 real-time clock pulses every one minute

bit 15 **ON:** RTCC On bit(1)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Disables RTCC operation when CPU enters Idle mode
0 = Continue normal operation when CPU enters Idle mode

bit 12-11 **Unimplemented:** Read as '0'

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).
5: This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

Note: This register is reset only on a Power-on Reset (POR).

REGISTER 28-11: AD1CMPCONn: ADC1 DIGITAL COMPARATOR CONTROL REGISTER 'n' ('n' = 1, 2, 3, 4, 5, OR 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	AINID<4:0>				
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN(1)	DCMPED	IEBTWN(1)	IEHIHI(1)	IEHILO(1)	IELOHI(1)	IELOLO(1)

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **AINID<4:0>:** Analog Input Identification (ID) bits

When a digital comparator event occurs, these read-only bits contain the analog input identification number. AINID = ANx, where 'x' = 0-31.

bit 7 **ENDCMP:** Digital Comparator Enable bit

1 = Digital Comparator is enabled
0 = Digital Comparator is not enabled, and the DCMPED status bit is cleared

bit 6 **DCMPGIEN:** Digital Comparator Global ADC Interrupt Enable bit(1)

1 = A Digital Comparator Event (DCMPED transitions from '0' to '1') will generate a Global ADC interrupt.
0 = A Digital Comparator Event will not generate a Global ADC interrupt.

bit 5 **DCMPED:** Digital Comparator Event Detected Status bit

1 = This bit is set by the digital comparator hardware when a comparison event is detected. An interrupt will be generated if the appropriate bit in the IECx register is set or if enabled for the ADC Global interrupt in the DCMPGIEN bit.
0 = This bit is cleared by reading the AINID<4:0> bits or when the ADC module is disabled

bit 4 **IEBTWN:** Between Low/High Digital Comparator Event bit(1)

1 = Generate a digital comparator event when ADCMPLO<15:0> ≤ DATA<31:0> < ADCMPHI<15:0>
0 = Do not generate a digital comparator event

bit 3 **IEHIHI:** High/High Digital Comparator Event bit(1)

1 = Generate a Digital Comparator Event when ADCMPHI<15:0> ≤ DATA<31:0>
0 = Do not generate a digital comparator event when ADCMPHI<15:0> ≤ DATA<31:0>

bit 2 **IEHILO:** High/Low Digital Comparator Event bit(1)

1 = Generate a Digital Comparator Event when DATA<31:0> < ADCMPHI<15:0>
0 = Do not generate a digital comparator event when DATA<31:0> < ADCMPHI<15:0>

bit 1 **IELOHI:** Low/High Digital Comparator Event bit(1)

1 = Generate a Digital Comparator Event when ADCMPLO<15:0> ≤ DATA<31:0>
0 = Do not generate a digital comparator event when ADCMPLO<15:0> ≤ DATA<31:0>

bit 0 **IELOLO:** Low/Low Digital Comparator Event bit(1)

1 = Generate a Digital Comparator Event when DATA<31:0> < ADCMPLO<15:0>
0 = Do not generate a digital comparator event when DATA<31:0> < ADCMPLO<15:0>

Note 1: Changing these bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

REGISTER 34-3: DEVCFG0/ADEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	—	EJTAGBEN	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	—	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>	
7:0	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN(1)	DEBUG<1:0>	

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '0'

bit 30 **EJTAGBEN:** EJTAG Boot Enable bit
- 1 = Normal EJTAG functionality
- 0 = Reduced EJTAG functionality

bit 29-15 **Reserved:** Write as '1'

bit 14-12 **DBGPER<2:0>:** Debug Mode CPU Access Permission bits
- 1xx = Allow CPU access to Permission Group 2 permission regions
- x1x = Allow CPU access to Permission Group 1 permission regions
- xx1 = Allow CPU access to Permission Group 0 permission regions
- 0xx = Deny CPU access to Permission Group 2 permission regions
- x0x = Deny CPU access to Permission Group 1 permission regions
- xx0 = Deny CPU access to Permission Group 0 permission regions

When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** Write as '1'

bit 10 **FSLEEP:** Flash Sleep Mode bit
- 1 = Flash is powered down when the device is in Sleep mode
- 0 = Flash power down is controlled by the VREGS bit (PWRCON<1>)

bit 9-8 **FECCCON<1:0>:** Dynamic Flash ECC Configuration bits

Upon a device Reset, the value of these bits is copied to the ECCCON<1:0> bits (CFGCON<5:4>).
- 11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
- 10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
- 01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
- 00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

bit 7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit
- 1 = Boot code and Exception code is MIPS32®
  (ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
- 0 = Boot code and Exception code is microMIPS™
  (ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit
- 1 = Trace features in the CPU are enabled
- 0 = Trace features in the CPU are disabled

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

REGISTER 34-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits

111 = FRC divided by FRCDIV<2:0> bits (FRCDIV)
110 = Reserved
101 = LPRC
100 = SOSC
011 = Reserved
010 = POSC (HS, EC)
001 = SPLL
000 = FRC divided by FRCDIV<2:0> bits (FRCDIV)

37.1 DC Characteristics

TABLE 37-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comment
			PIC32MZ EC Devices	
DC5	2.3V-3.6V	-40°C to +85°C	200 MHz	—

Note 1: Overall functional device operation at $V_{BORMIN} < V_{DD} < V_{DDMIN}$ is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below V_{DDMIN}. Refer to parameter BO10 in Table 37-5 for BOR values.

TABLE 37-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - S\ I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = S\ (\{V_{DD} - V_{OH}\} \times I_{OH}) + S\ (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 37-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN (9x9x0.9 mm)	θ_{JA}	28	—	°C/W	**1**
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θ_{JA}	49	—	°C/W	**1**
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θ_{JA}	43	—	°C/W	**1**
Package Thermal Resistance, 100-pin TQFP (14x14x1 mm)	θ_{JA}	40	—	°C/W	**1**
Package Thermal Resistance, 124-pin VTLA (9x9x0.9 mm)	θ_{JA}	30	—	°C/W	**1**
Package Thermal Resistance, 144-pin TQFP (16x16x1 mm)	θ_{JA}	42	—	°C/W	**1**
Package Thermal Resistance, 144-pin LQFP (20x20x1.4 mm)	θ_{JA}	39	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	—
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

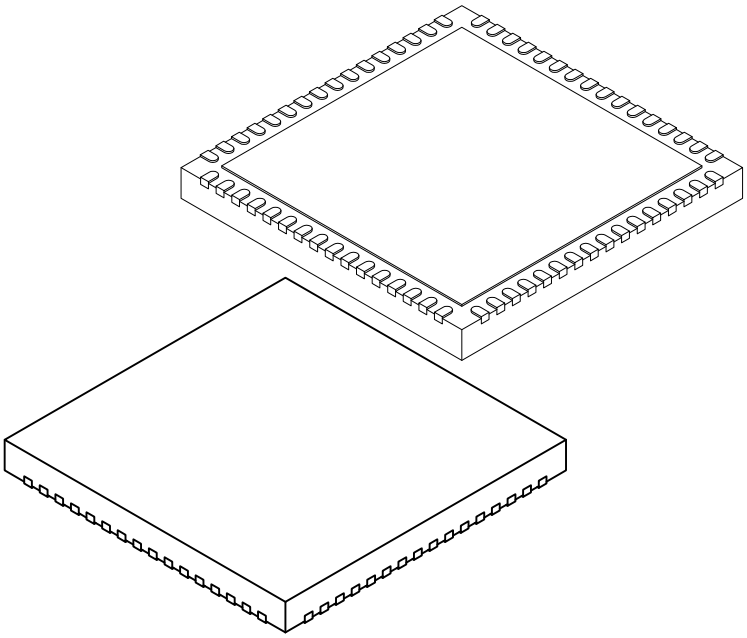
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 10 pF load on all SPIx pins.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.70 x 7.70 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.60	7.70	7.80
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.60	7.70	7.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

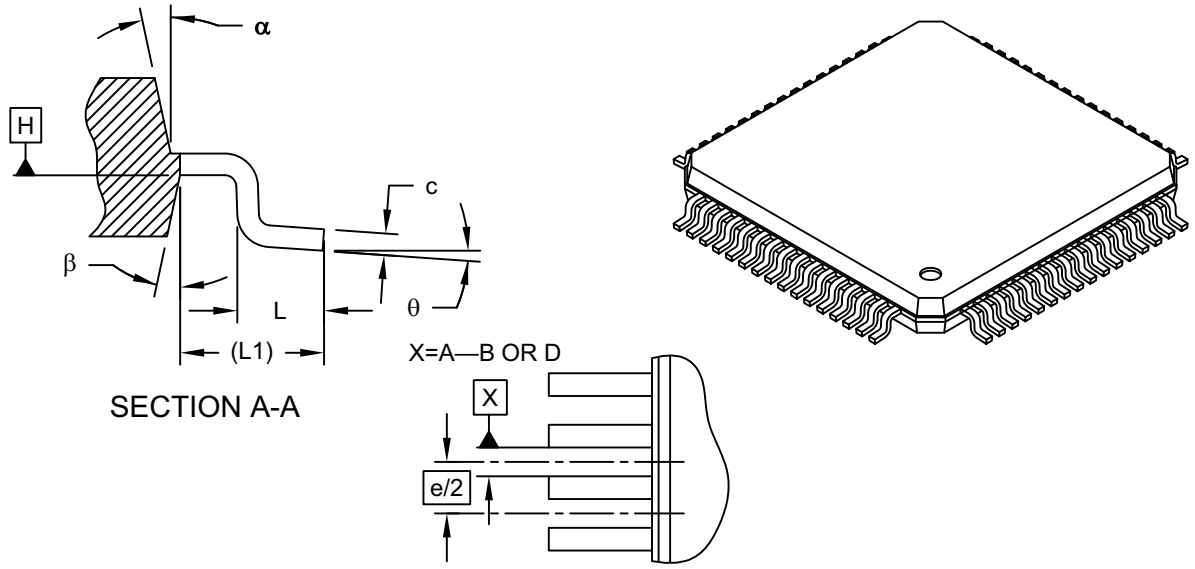
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-213B Sheet 2 of 2

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

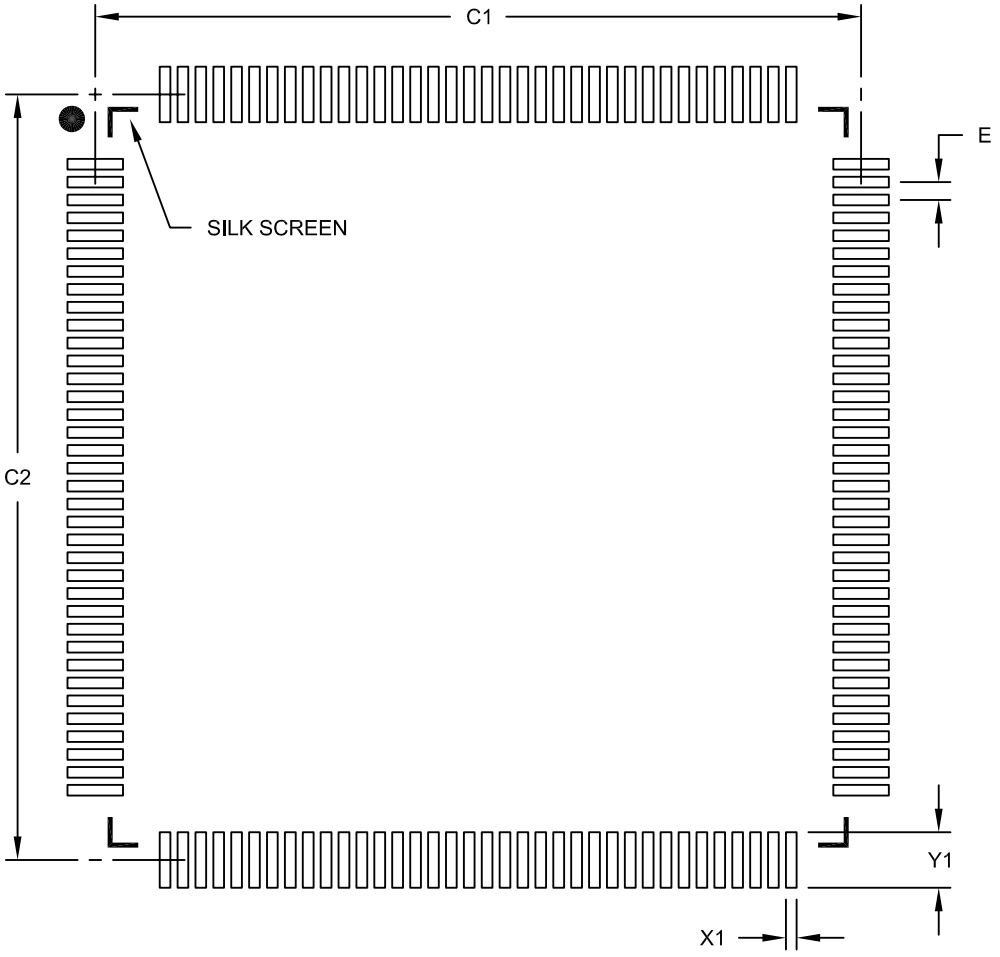
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

144-Lead Plastic Low Profile Quad Flatpack (PL) - 20x20x1.40 mm Body [LQFP]
2.00 mm Footprint

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		21.40	
Contact Pad Spacing	C2		21.40	
Contact Pad Width (X144)	X1			0.30
Contact Pad Length (X144)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2044B

A.8 Flash Programming

The PIC32MZ family of devices incorporates a new Flash memory technology. Applications ported from PIC32MX5XX/6XX/7XX devices that take advantage of Run-time Self Programming will need to adjust the Flash programming steps to incorporate these changes.

Table A-9 lists the differences (indicated by **Bold** type) that will affect software migration.

TABLE A-9: FLASH PROGRAMMING DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
Program Flash Write Protection	
On PIC32MX devices, the Program Flash write-protect bits are part of the Flash Configuration words (DEVCFG0). PWP<**7**:0> (**DEVCFG0<19:12>**) 11111111 = Disabled 11111110 = 0xBD000FFF 11111101 = 0xBD001FFF 11111100 = 0xBD002FFF 11111011 = 0xBD003FFF 11111010 = 0xBD004FFF 11111001 = 0xBD005FFF 11111000 = 0xBD006FFF 11110111 = 0xBD007FFF 11110110 = 0xBD008FFF 11110101 = 0xBD009FFF 11110100 = 0xBD00AFFF 11110011 = 0xBD00BFFF 11110010 = 0xBD00CFFF 11110001 = 0xBD00DFFF 11110000 = 0xBD00EFFF 11101111 = 0xBD00FFFF • • • 01111111 = 0xBD07FFFF	On PIC32MZ devices, the write-protect register is contained separately as the NVMPWP register. It has been expanded to 24 bits, and now represents the address below, which all Flash memory is protected. Note that the lower 14 bits are forced to zero, so that all memory locations in the page are protected. PWP<**23**:0> (**NVMPWP<23:0>**) Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>. When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.
Code Protection	
On PIC32MX devices, code protection is enabled by the CP (**DEVCFG**<28>) bit.	On PIC32MZ devices, code protection is enabled by the CP (**DEVCP0**<28>) bit.
Boot Flash Write Protection	
On PIC32MX devices, Boot Flash write protection is enable by the **BWP (DEVCFG<24>)** bit and protects the entire Boot Flash memory.	On PIC32MZ devices, Boot Flash write protection is divided into pages and is enable by the **LBWPx** and **UBWPx** bits in the **NVMBWP** register.
Low-Voltage Detect Status	
LVDSTAT (NVMCON<11>) 1 = Low-voltage event is active 0 = Low-voltage event is not active	The LVDSTAT bit is not available in PIC32MZ devices.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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