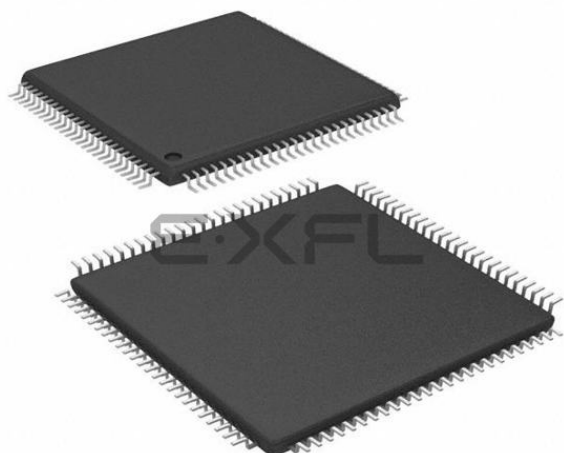




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ech100-i-pf

PIC32MZ Embedded Connectivity (EC) Family

Device Pin Tables

TABLE 2: PIN NAMES FOR 64-PIN DEVICES

64-PIN QFN ⁽⁴⁾ AND TQFP (TOP VIEW)			
PIC32MZ0512EC(E/F/K)064 PIC32MZ1024EC(G/H/M)064 PIC32MZ1024EC(E/F/K)064 PIC32MZ2048EC(G/H/M)064			
		64	1
		QFN ⁽⁴⁾	TQFP ¹
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN17/ETXEN/RPE5/PMD5/RE5	33	VBUS
2	AN16/ETXD0/PMD6/RE6	34	VUSB3V3
3	AN15/ETXD1/PMD7/RE7	35	Vss
4	AN14/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN13/C1INC/RPG7/SDA4/PMA4/RG7	37	D+
6	AN12/C2IND/RPG8/SCL4/PMA3/RG8	38	RPF3/USBID/RF3
7	Vss	39	VDD
8	VDD	40	Vss
9	MCLR	41	RPF4/SDA5/PMA9/RF4
10	AN11/C2INC/RPG9/PMA2/RG9	42	RPF5/SCL5/PMA8/RF5
11	AN45/C1INA/RPB5/RB5	43	AERXD0/ETXD2/RPD9/SDA1/PMCS2/PMA15/RD9
12	AN4/C1INB/RB4	44	ECOL/RPD10/SCL1/SCK4/RD10
13	AN3/C2INA/RPB3/RB3	45	AERXCLK/AEREFCLK/ECRS/RPD11/PMCS1/PMA14/RD11
14	AN2/C2INB/RPB2/RB2	46	AERXD1/ETXD3/RPD0/RTCC/INT0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN46/RPB6/RB6	49	EMDIO/AEMDIO/RPD1/SCK1/RD1
18	PGED2/AN47/RPB7/RB7	50	ETXERR/AETXEN/RPD2/SDA3/RD2
19	AVDD	51	AERXERR/ETXCLK/RPD3/SCL3/RD3
20	AVss	52	SQICS0/RPD4/PMWR/RD4
21	AN48/RPB8/PMA10/RB8	53	SQICS1/RPD5/PMRD/RD5
22	AN49/RPB9/PMA7/RB9	54	VDD
23	TMS/CVREFOUT/AN5/RPB10/PMA13/RB10	55	Vss
24	TDO/AN6/PMA12/RB11	56	ERXD3/AETXD1/RPF0/RF0
25	Vss	57	TRCLK/SQICLK/ERXD2/AETXD0/RPF1/RF1
26	VDD	58	TRD0/SQID0/ERXD1/PMD0/RE0
27	TCK/AN7/PMA11/RB12	59	Vss
28	TDI/AN8/RB13	60	VDD
29	AN9/RPB14/SCK3/PMA1/RB14	61	TRD1/SQID1/ERXD0/PMD1/RE1
30	AN10/EMDC/AEMDC/RPB15/OCFB/PMA0/RB15	62	TRD2/SQID2/ERXDV/ECRSDV/AECRSDV/PMD2/RE2
31	OSC1/CLK1/RC12	63	TRD3/SQID3/ERXCLK/EREFCLK/RPE3/PMD3/RE3
32	OSC2/CLK0/RC15	64	AN18/ERXERR/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 “Peripheral Pin Select (PPS)”** for restrictions.
 - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.
 - 4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-13: EBI PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
EBIOE	—	9	A7	13	O	—	External Bus Interface Output Enable
EBIRDY1	—	60	B34	86	I	ST	External Bus Interface Ready Input
EBIRDY2	—	58	A39	84	I	ST	
EBIRDY3	—	57	B45	116	I	ST	
EBIRP	—	—	—	45	O	—	External Bus Interface Flash Reset Pin
EBIWE	—	8	B5	12	O	—	External Bus Interface Write Enable

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-18: ALTERNATE ETHERNET MII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
AERXD0	—	18	—	—	I	ST	Alternate Ethernet Receive Data 0
AERXD1	—	19	—	—	I	ST	Alternate Ethernet Receive Data 1
AERXD2	—	28	—	—	I	ST	Alternate Ethernet Receive Data 2
AERXD3	—	29	—	—	I	ST	Alternate Ethernet Receive Data 3
AERXERR	—	1	—	—	I	ST	Alternate Ethernet Receive Error Input
AERXDV	—	12	—	—	I	ST	Alternate Ethernet Receive Data Valid
AERXCLK	—	16	—	—	I	ST	Alternate Ethernet Receive Clock
AETXD0	—	47	—	—	O	—	Alternate Ethernet Transmit Data 0
AETXD1	—	48	—	—	O	—	Alternate Ethernet Transmit Data 1
AETXD2	—	44	—	—	O	—	Alternate Ethernet Transmit Data 2
AETXD3	—	43	—	—	O	—	Alternate Ethernet Transmit Data 3
AETXERR	—	35	—	—	O	—	Alternate Ethernet Transmit Error
AECOL	—	42	—	—	I	ST	Alternate Ethernet Collision Detect
AECRS	—	41	—	—	I	ST	Alternate Ethernet Carrier Sense
AETXCLK	—	66	—	—	I	ST	Alternate Ethernet Transmit Clock
AEMDC	—	70	—	—	O	—	Alternate Ethernet Management Data Clock
AEMDIO	—	71	—	—	I/O	—	Alternate Ethernet Management Data
AETXEN	—	67	—	—	O	—	Alternate Ethernet Transmit Enable

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

TABLE 1-19: ALTERNATE ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
AERXD0	43	18	—	—	I	ST	Alternate Ethernet Receive Data 0
AERXD1	46	19	—	—	I	ST	Alternate Ethernet Receive Data 1
AERXERR	51	1	—	—	I	ST	Alternate Ethernet Receive Error Input
AETXD0	57	47	—	—	O	—	Alternate Ethernet Transmit Data 0
AETXD1	56	48	—	—	O	—	Alternate Ethernet Transmit Data 1
AEMDC	30	70	—	—	O	—	Alternate Ethernet Management Data Clock
AEMDIO	49	71	—	—	I/O	—	Alternate Ethernet Management Data
AETXEN	50	67	—	—	O	—	Alternate Ethernet Transmit Enable
AEREFCLK	45	16	—	—	I	ST	Alternate Ethernet Reference Clock
AECRS	62	12	—	—	I	ST	Alternate Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits																All Reset
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF1DEVCFG3	31:0	Note: See Table 34-2 for the bit descriptions.																XXXX
FF44	ABF1DEVCFG2	31:0																	XXXX
FF48	ABF1DEVCFG1	31:0																	XXXX
FF4C	ABF1DEVCFG0	31:0																	XXXX
FF50	ABF1DEVCP3	31:0																	XXXX
FF54	ABF1DEVCP2	31:0																	XXXX
FF58	ABF1DEVCP1	31:0																	XXXX
FF5C	ABF1DEVCP0	31:0																	XXXX
FF60	ABF1DEVSIGN3	31:0																	XXXX
FF64	ABF1DEVSIGN2	31:0																	XXXX
FF68	ABF1DEVSIGN1	31:0																	XXXX
FF6C	ABF1DEVSIGN0	31:0																	XXXX
FF70	ABF1SEQ3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FF74	ABF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FF78	ABF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FF7C	ABF1SEQ0	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX
FFC0	BF1DEVCFG3	31:0	Note: See Table 34-1 for the bit descriptions.																XXXX
FFC4	BF1DEVCFG2	31:0																	XXXX
FFC8	BF1DEVCFG1	31:0																	XXXX
FFCC	BF1DEVCFG0	31:0																	XXXX
FFD0	BF1DEVCP3	31:0																	XXXX
FFD4	BF1DEVCP2	31:0																	XXXX
FFD8	BF1DEVCP1	31:0																	XXXX
FFDC	BF1DEVCP0	31:0																	XXXX
FFE0	BF1DEVSIGN3	31:0																	XXXX
FFE4	BF1DEVSIGN2	31:0																	XXXX
FFE8	BF1DEVSIGN1	31:0																	XXXX
FFEC	BF1DEVSIGN0	31:0																	XXXX
FFF0	BF1SEQ3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFF4	BF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFF8	BF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFFC	BF1SEQ0	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 4-10: SYSTEM BUS TARGET 2 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
8820	SBT2ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000	
8824	SBT2ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000	
8828	SBT2ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT2ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT2ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT2REG0	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8850	SBT2RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8858	SBT2WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8860	SBT2REG1	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8870	SBT2RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8878	SBT2WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8880	SBT2REG2	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8890	SBT2RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8898	SBT2WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

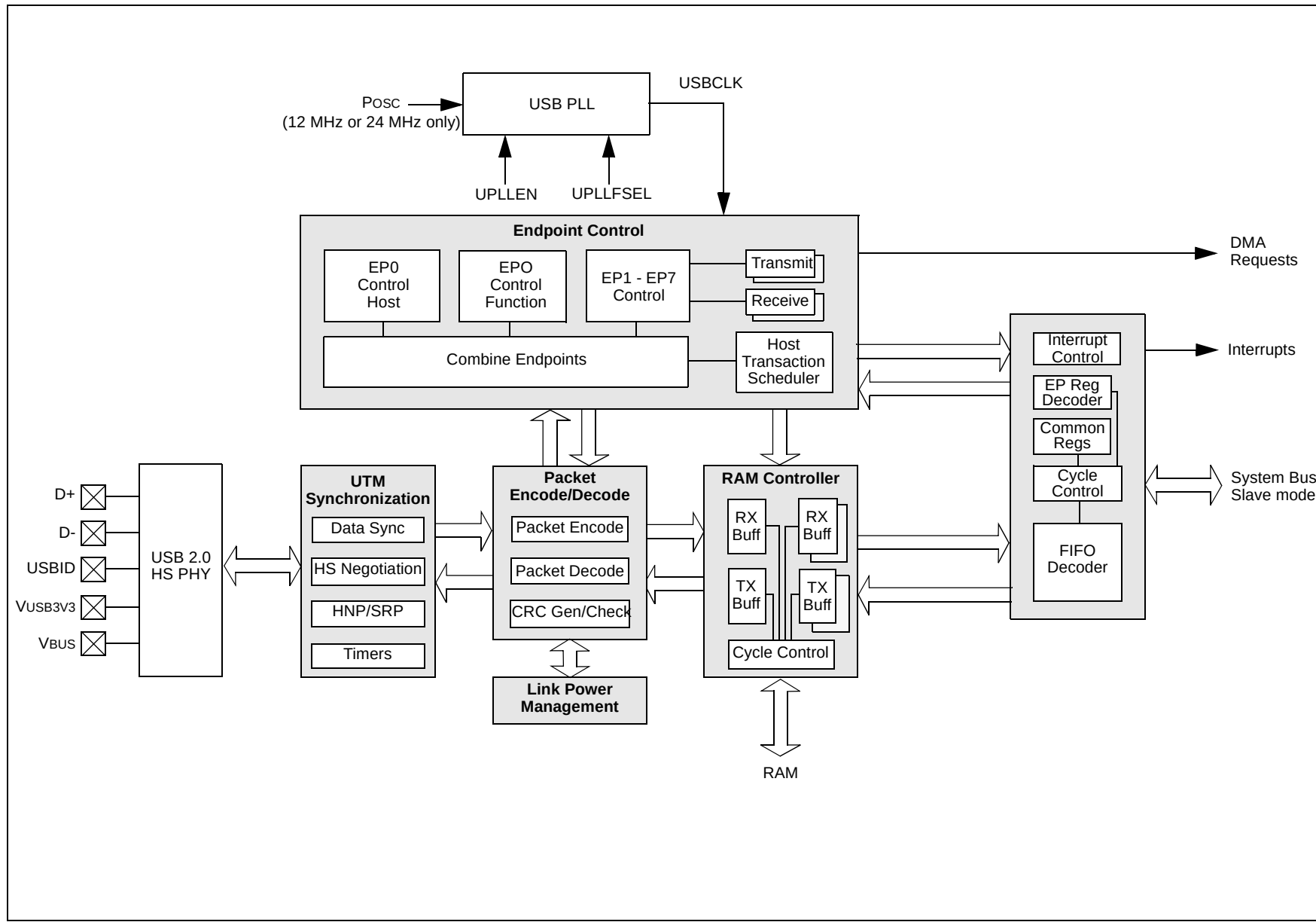
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 10-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF**: Channel Destination Done Interrupt Flag bit
1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
0 = No interrupt is pending
- bit 4 **CHDHIF**: Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending
- bit 3 **CHBCIF**: Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending
- bit 2 **CHCCIF**: Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending
- bit 1 **CHTAIF**: Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending
- bit 0 **CHERIF**: Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected
 Either the source or the destination address is invalid.
0 = No interrupt is pending

FIGURE 11-1: PIC32MZ EC FAMILY USB INTERFACE DIAGRAM



PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R-0	R/W-0
	AUTOCLR	ISO AUTORQ	DMAREQEN	DISNYET PIDERR	DMAREQMD	— DATATWEN	— DATATGGL	INCOMPRX
23:16	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0, HC	R-0, HS	R/W-0, HS	R-0, HSC	R/W-0, HS
	CLRDT	SENTSTALL RXSTALL	SENDSTALL REQPKT	FLUSH	DATAERR DERRNAKT	OVERRUN ERROR	FIFOFULL	RXPKTRDY
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					RXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXMAXP<7:0>							

Legend:	HC = Hardware Clearable	HS = Hardware Settable
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 31 **AUTOCLR:** RXPKTRDY Automatic Clear Control bit
- 1 = RXPKTRDY will be automatically cleared when a packet of RXMAXP bytes has been unloaded from the RX FIFO. When packets of less than the maximum packet size are unloaded, RXPKTRDY will have to be cleared manually. When using a DMA to unload the RX FIFO, data is read from the RX FIFO in 4-byte chunks regardless of the RXMAXP.
- 0 = No automatic clearing of RXPKTRDY
- This bit should not be set for high-bandwidth Isochronous endpoints.
- bit 30 **ISO:** Isochronous Endpoint Control bit (*Device mode*)
- 1 = Enable the RX endpoint for Isochronous transfers
- 0 = Enable the RX endpoint for Bulk/Interrupt transfers
- AUTORQ:** Automatic Packet Request Control bit (*Host mode*)
- 1 = REQPKT will be automatically set when RXPKTRDY bit is cleared.
- 0 = No automatic packet request
- This bit is automatically cleared when a short packet is received.
- bit 29 **DMAREQEN:** DMA Request Enable Control bit
- 1 = Enable DMA requests for the RX endpoint.
- 0 = Disable DMA requests for the RX endpoint.
- bit 28 **DISNYET:** Disable NYET Handshakes Control/PID Error Status bit (*Device mode*)
- 1 = In Bulk/Interrupt transactions, disables the sending of NYET handshakes. All successfully received RX packets are ACKed including at the point at which the FIFO becomes full.
- 0 = Normal operation.
- In Bulk/Interrupt transactions, this bit only has any effect in Hi-Speed mode, in which mode it should be set for all Interrupt endpoints.
- PIDERR:** PID Error Status bit (*Host mode*)
- 1 = In ISO transactions, this indicates a PID error in the received packet.
- 0 = No error
- bit 27 **DMAREQMD:** DMA Request Mode Selection bit
- 1 = DMA Request Mode 1
- 0 = DMA Request Mode 0

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXDPB	RXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXDPB	TXFIFOSZ<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	TXEDMA	RXEDMA
7:0	R-1	R-0	R-0	R-0	R-0	R-0	R/W-0, HC	R/W-0
	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **RXDPB:** RX Endpoint Double-packet Buffering Control bit

1 = Double-packet buffer is supported. This doubles the size set in RXFIFOSZ.

0 = Double-packet buffer is not supported

bit 27-24 **RXFIFOSZ<3:0>:** RX Endpoint FIFO Packet Size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved

•
•
•

1010 = Reserved

1001 = 4096 bytes

1000 = 2048 bytes

0111 = 1024 bytes

0110 = 512 bytes

0101 = 256 bytes

0100 = 128 bytes

0011 = 64 bytes

0010 = 32 bytes

0001 = 16 bytes

0000 = 8 bytes

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **TXDPB:** TX Endpoint Double-packet Buffering Control bit

1 = Double-packet buffer is supported. This doubles the size set in TXFIFOSZ.

0 = Double-packet buffer is not supported

TABLE 12-13: PORTF REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TRISF5	TRISF4	TRISF3	—	TRISF1	TRISF0	003B
0520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	RF5	RF4	RF3	—	RF1	RF0	xxxx
0530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	LATF5	LATF4	LATF3	—	LATF1	LATF0	xxxx
0540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ODCF5	ODCF4	ODCF3	—	ODCF1	ODCF0	0000
0550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CNPUF5	CNPUF4	CNPUF3	—	CNPUF1	CNPUF0	0000
0560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CNPDF5	CNPDF4	CNPDF3	—	CNPDF1	CNPDF0	0000
0570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CNIEF5	CNIEF4	CNIEF3	—	CNIEF1	CNIEF0	0000
0590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CN STATF5	CN STATF4	CN STATF3	—	CN STATF1	CN STATF0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 26-1: CEVER: CRYPTO ENGINE REVISION, VERSION, AND ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
REVISION<7:0>								
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VERSION<7:0>								
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ID<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ID<7:0>								

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **REVISION<7:0>**: Crypto Engine Revision bits

bit 23-16 **VERSION<7:0>**: Crypto Engine Version bits

bit 15-0 **ID<15:0>**: Crypto Engine Identification bits

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B0B8	AD1DATA0	31:16	ADC Output Register 0 <31:16>																0000
		15:0	ADC Output Register 0 <15:0>																0000
B0BC	AD1DATA1	31:16	ADC Output Register 1 <31:16>																0000
		15:0	ADC Output Register 1 <15:0>																0000
B0C0	AD1DATA2	31:16	ADC Output Register 2 <31:16>																0000
		15:0	ADC Output Register 2 <15:0>																0000
B0C4	AD1DATA3	31:16	ADC Output Register 3 <31:16>																0000
		15:0	ADC Output Register 3 <15:0>																0000
B0C8	AD1DATA4	31:16	ADC Output Register 4 <31:16>																0000
		15:0	ADC Output Register 4 <15:0>																0000
B0CC	AD1DATA5	31:16	ADC Output Register 5 <31:16>																0000
		15:0	ADC Output Register <15:0>																0000
B0D0	AD1DATA6	31:16	ADC Output Register 6 <31:16>																0000
		15:0	ADC Output Register 6 <15:0>																0000
B0D4	AD1DATA7	31:16	ADC Output Register 7 <31:16>																0000
		15:0	ADC Output Register 7 <15:0>																0000
B0D8	AD1DATA8	31:16	ADC Output Register 8 <31:16>																0000
		15:0	ADC Output Register 8 <15:0>																0000
B0DC	AD1DATA9	31:16	ADC Output Register 9 <31:16>																0000
		15:0	ADC Output Register 9 <15:0>																0000
B0E0	AD1DATA10	31:16	ADC Output Register 10 <31:16>																0000
		15:0	ADC Output Register 10 <15:0>																0000
B0E4	AD1DATA11	31:16	ADC Output Register 11 <31:16>																0000
		15:0	ADC Output Register 11 <15:0>																0000
B0E8	AD1DATA12	31:16	ADC Output Register 12 <31:16>																0000
		15:0	ADC Output Register 12 <15:0>																0000
B0EC	AD1DATA13	31:16	ADC Output Register 13 <31:16>																0000
		15:0	ADC Output Register 13 <15:0>																0000
B0F0	AD1DATA14	31:16	ADC Output Register 14 <31:16>																0000
		15:0	ADC Output Register 14 <15:0>																0000
B0F4	AD1DATA15	31:16	ADC Output Register 15 <31:16>																0000
		15:0	ADC Output Register 15 <15:0>																0000
B0F8	AD1DATA16	31:16	ADC Output Register 16 <31:16>																0000
		15:0	ADC Output Register 16 <15:0>																0000
B0FC	AD1DATA17	31:16	ADC Output Register 17 <31:16>																0000
		15:0	ADC Output Register 17<15:0>																0000
B100	AD1DATA18	31:16	ADC Output Register 18 <31:16>																0000
		15:0	ADC Output Register18 <15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 29-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **FLTEN23:** Filter 23 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0
- bit 23 **FLTEN22:** Filter 22 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENN) bit is '0'.

TABLE 30-5: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2110	ETH FRMTXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMTXOKCNT<15:0>																0000
2120	ETH SCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SCOLFRMCNT<15:0>																0000
2130	ETH MCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MCOLFRMCNT<15:0>																0000
2140	ETH FRMRXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMRXOKCNT<15:0>																0000
2150	ETH FCSERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FCSERRCNT<15:0>																0000
2160	ETH ALGNERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALGNERRCNT<15:0>																0000
2200	EMAC1 CFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN	—	—	—	LOOPBACK	TXPAUSE	RXPAUSE	PASSALL	RXENABLE	0000
2210	EMAC1 CFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	EXCESS DFR	BP NOBKOFF	NOBKOFF	—	—	LONGPRE	PUREPRE	AUTOPAD	VLANPAD	PAD ENABLE	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX	4082
2220	EMAC1 IPGT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0012
2230	EMAC1 IPGR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	NB2BIPKTGP1<6:0>							—	NB2BIPKTGP2<6:0>							0C12
2240	EMAC1 CLRT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CWINDOW<5:0>						—	—	—	—	RETX<3:0>				370F
2250	EMAC1 MAXF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MACMAXF<15:0>																05EE
2260	EMAC1 SUPP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RESET RMII	—	—	SPEED RMII	—	—	—	—	—	—	—	—	1000
2270	EMAC1 TEST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	TESTBP	TESTPAUSE	SHRTQNTA	0000
2280	EMAC1 MCFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RESET MGMT	—	—	—	—	—	—	—	—	—	CLKSEL<3:0>				NOPRE	SCANINC	0020
2290	EMAC1 MCMD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCAN	READ	0000
22A0	EMAC1 MADR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PHYADDR<4:0>					—	—	—	REGADDR<4:0>					0100

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

Note 2: Reset values default to the factory programmed value.

31.1 Comparator Control Registers

TABLE 31-1: COMPARATOR REGISTER MAP

Virtual Address (BF84_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>	—	—	CREF	—	—	CCH<1:0>	—	00C3
C010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>	—	—	CREF	—	—	CCH<1:0>	—	00C3
C060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

NOTES:

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FIGURE 37-5: EXTERNAL RESET TIMING CHARACTERISTICS

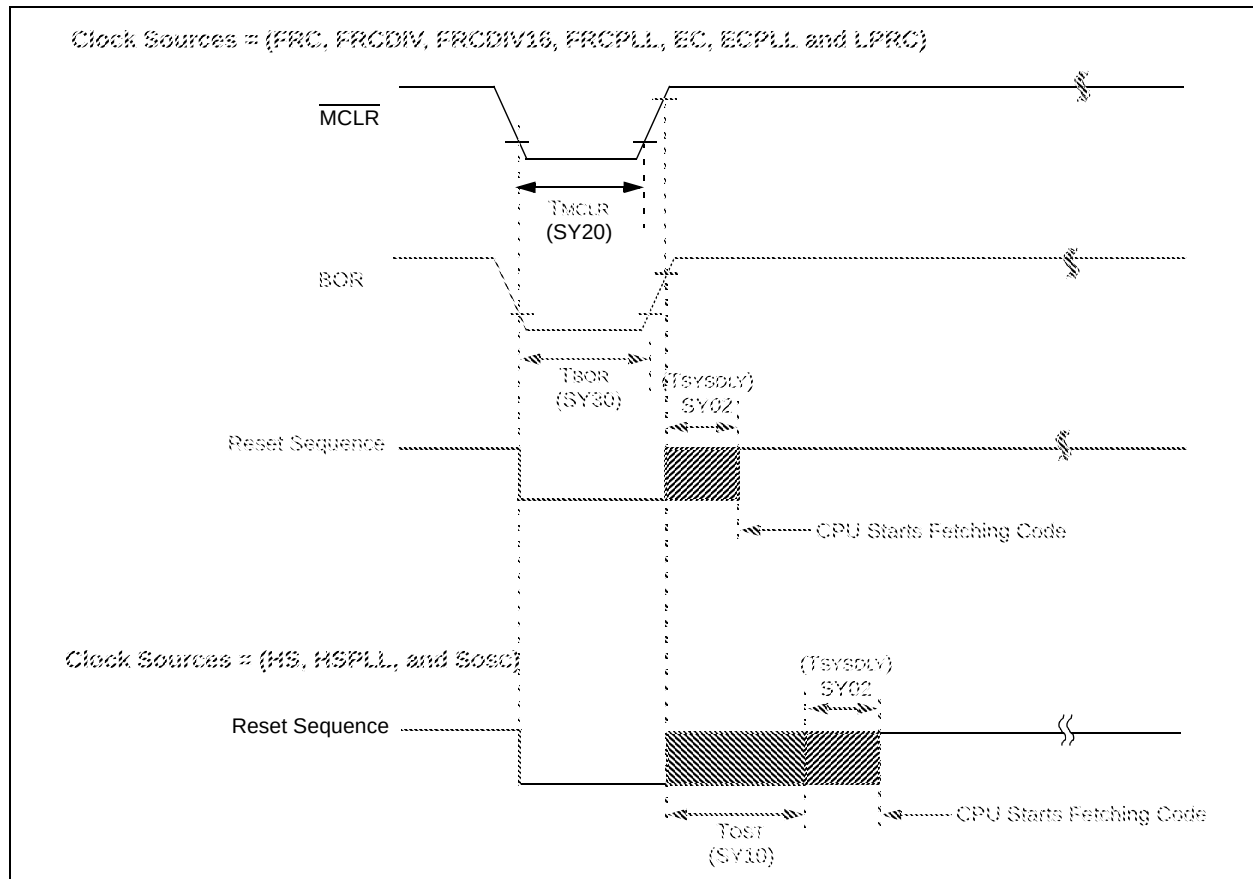


TABLE 37-24: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	—
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	—	$1 \mu\text{s} +$ 8 SYSCLK cycles	—	—	—
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	μs	—
SY30	TBOR	BOR Pulse Width (low)	—	1	—	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Characterized by design but not tested.

PIC32MZ Embedded Connectivity (EC) Family

FIGURE 37-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

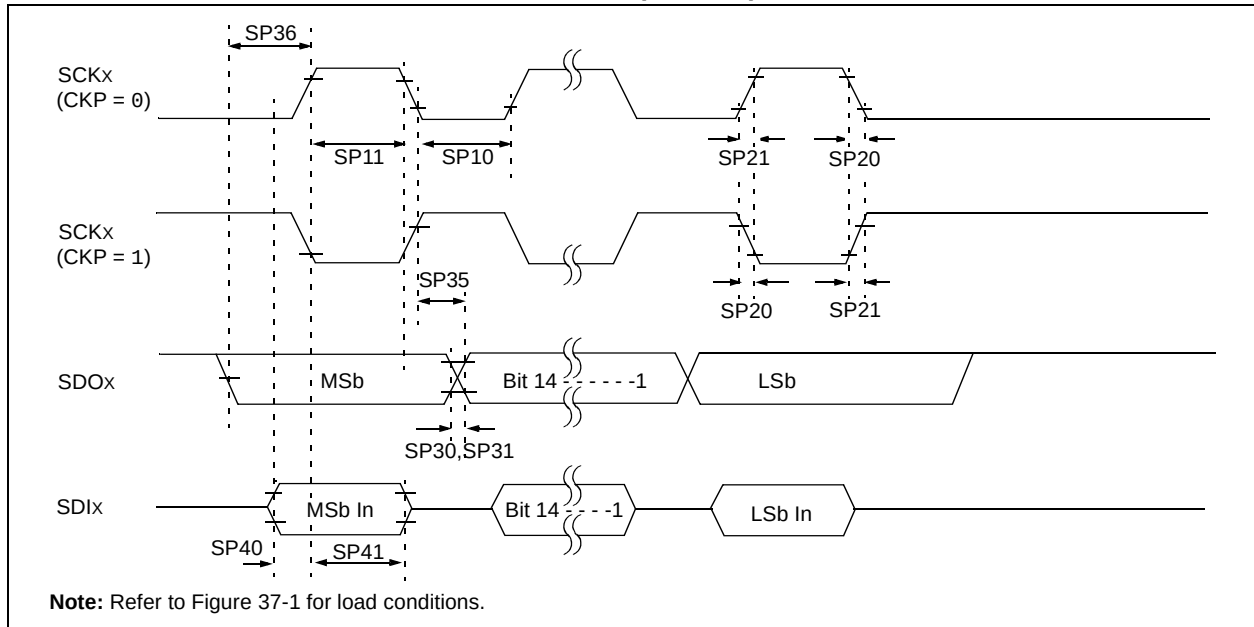


TABLE 37-31: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time (Note 3)	T _{SCK} /2	—	—	ns	—
SP11	Tsch	SCKx Output High Time (Note 3)	T _{SCK} /2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	V _{DD} > 2.7V
			—	—	10	ns	V _{DD} < 2.7V
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	7	—	—	ns	—
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	7	—	—	ns	V _{DD} > 2.7V
			10	—	—	ns	V _{DD} < 2.7V
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	V _{DD} > 2.7V
			10	—	—	ns	V _{DD} < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

Note 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Note 3: The minimum clock period for SCKx is 20 ns. Therefore, the clock generated in Master mode must not violate this specification.

Note 4: Assumes 10 pF load on all SPIx pins.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM21	Tr:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode	—	300	ns	
			(Note 2)				
IM25	Tsu:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode	100	—	ns	
			(Note 2)				
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode	0	0.3	μs	
			(Note 2)				
IM30	Tsu:STA	Start Condition Setup Time	100 kHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	
			1 MHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	
			(Note 2)				
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	
			1 MHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	
			(Note 2)				
IM33	Tsu:STO	Stop Condition Setup Time	100 kHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	
			1 MHz mode	$TPBCLK2 * (BRG + 2)$	—	μs	
			(Note 2)				
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$TPBCLK2 * (BRG + 2)$	—	ns	—
			400 kHz mode	$TPBCLK2 * (BRG + 2)$	—	ns	
			1 MHz mode	$TPBCLK2 * (BRG + 2)$	—	ns	
			(Note 2)				
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode	—	350	ns	—
			(Note 2)				
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode	0.5	—	μs	
			(Note 2)				
IM50	Cb	Bus Capacitive Loading		—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See Note 3

Note 1: BRG is the value of the I²C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

PIC32MZ Embedded Connectivity (EC) Family

A.10 Package Differences

In general, PIC32MZ devices are mostly pin compatible with PIC32MX5XX/6XX/7XX devices; however, some pins are not. In particular, the VDD and VSS pins have been added and moved to different pins. In addition, I/O functions that were on fixed pins now will largely be on remappable pins.

TABLE A-11: PACKAGE DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
VCAP Pin	
On PIC32MX devices, an external capacitor is required between a VCAP pin and GND, which provides a filtering capacitor for the internal voltage regulator. A low-ESR capacitor (typically 10 μ F) is required on the VCAP pin.	On PIC32MZ devices, this requirement has been removed. No VCAP pin.
VDD and VSS Pins	
VDD on 64-pin packages: 10, 26, 38, 57 VDD on 100-pin packages: 2, 16, 37, 46, 62, 86	There are more VDD pins on PIC32MZ devices, and many are located on different pins. VDD on 64-pin packages: 8, 26, 39, 54, 60 VDD on 100-pin packages: 14, 37, 46, 62, 74, 83, 93
VSS on 64-pin packages: 9, 25, 41 VSS on 100-pin packages: 15, 36, 45, 65, 75	There are more VSS pins on PIC32MZ devices, and many are located on different pins. VSS on 64-pin packages: 7, 25, 35, 40, 55, 59 VSS on 100-pin packages: 13, 36, 45, 53, 63, 75, 84, 92
PPS I/O Pins	
All peripheral functions are fixed as to what pin upon which they operate.	Peripheral functions on PIC32MZ devices are now routed through a PPS module, which routes the signals to the desired pins. When migrating software, it is necessary to initialize the PPS I/O functions in order to get the signal to and from the correct pin. PPS functionality for the following peripherals: • CAN • UART • SPI (except SCK) • Input Capture • Output Compare • External Interrupt (except INT0) • Timer Clocks (except Timer1) • Reference Clocks (except REFCLK2)