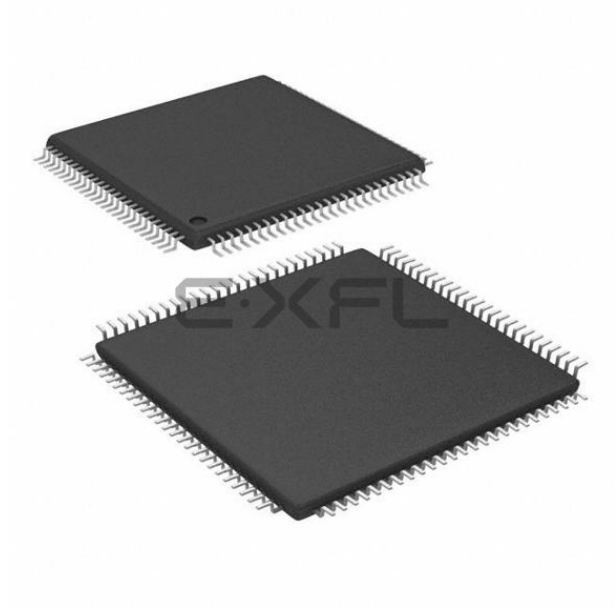
Microchip Technology - PIC32MZ2048ECH100T-I/PF Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ech100t-i-pf

TABLE 5: PIN NAMES FOR 144-PIN DEVICES

144-PIN LQFP AND TQFP (TOP VIEW)

PIC32MZ0512EC(E/F/K)144
PIC32MZ1024EC(G/H/M)144
PIC32MZ1024EC(E/F/K)144
PIC32MZ2048EC(G/H/M)144

144

1

Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	AN23/RG15	37	PGEC2/AN46/RPB6/RB6
2	EBIA5/AN34/PMA5/RA5	38	PGED2/AN47/RPB7/RB7
3	EBID5/AN17/RPE5/PMD5/RE5	39	VREF-/CVREF-/AN27/RA9
4	EBID6/AN16/PMD6/RE6	40	VREF+/CVREF+/AN28/RA10
5	EBID7/AN15/PMD7/RE7	41	AVDD
6	EBIA6/AN22/RPC1/PMA6/RC1	42	AVSS
7	AN35/ETXD0/RJ8	43	AN38/ETXD2/RH0
8	AN36/ETXD1/RJ9	44	AN39/ETXD3/RH1
9	$\overline{\text{EBIBS0}}$/RJ12	45	$\overline{\text{EBIRP}}$/RH2
10	$\overline{\text{EBIBS1}}$/RJ10	46	RH3
11	EBIA12/AN21/RPC2/PMA12/RC2	47	EBIA10/AN48/RPB8/PMA10/RB8
12	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	48	EBIA7/AN49/RPB9/PMA7/RB9
13	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	49	CVREFOUT/AN5/RPB10/RB10
14	AN14/C1IND/RPG6/SCK2/RG6	50	AN6/RB11
15	AN13/C1INC/RPG7/SDA4/RG7	51	EBIA1/PMA1/RK1
16	AN12/C2IND/RPG8/SCL4/RG8	52	EBIA3/PMA3/RK2
17	VSS	53	EBIA17/RK3
18	VDD	54	VSS
19	EBIA16/RK0	55	VDD
20	$\overline{\text{MCLR}}$	56	TCK/AN29/RA1
21	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	57	TDI/AN30/RPF13/SCK5/RF13
22	TMS/AN24/RA0	58	TDO/AN31/RPF12/RF12
23	AN25/RPE8/RE8	59	AN7/RB12
24	AN26/RPE9/RE9	60	AN8/RB13
25	AN45/C1INA/RPB5/RB5	61	AN9/RPB14/SCK3/RB14
26	AN4/C1INB/RB4	62	AN10/RPB15/OCFB/RB15
27	AN37/ERXCLK/EREFCLK/RJ11	63	VSS
28	EBIA13/PMA13/RJ13	64	VDD
29	EBIA11/PMA11/RJ14	65	AN40/ERXERR/RH4
30	EBIA0/PMA0/RJ15	66	AN41/ERXD1/RH5
31	AN3/C2INA/RPB3/RB3	67	AN42/ERXD2/RH6
32	VSS	68	EBIA4/PMA4/RH7
33	VDD	69	AN32/RPD14/RD14
34	AN2/C2INB/RPB2/RB2	70	AN33/RPD15/SCK6/RD15
35	PGEC1/AN1/RPB1/RB1	71	OSC1/CLKI/RC12
36	PGED1/AN0/RPB0/RB0	72	OSC2/CLKO/RC15

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-7: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Timer1 through Timer9							
T1CK	48	73	A49	106	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar							
RTCC	46	71	A48	104	O	—	Real-Time Clock Alarm/Seconds Output

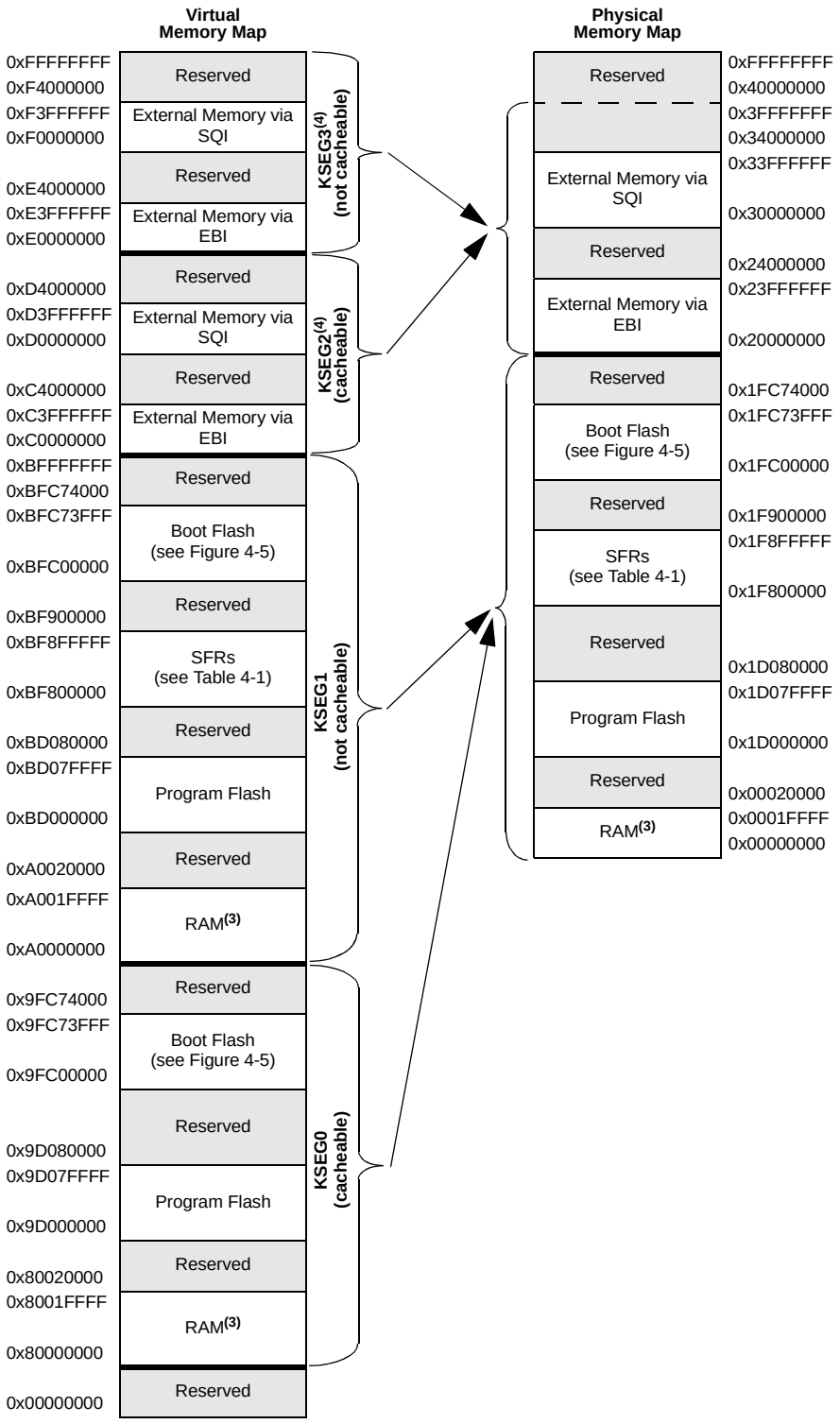
Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-8: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Universal Asynchronous Receiver Transmitter 1							
U1RX	PPS	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	PPS	O	—	UART1 Transmit
U1CTS	PPS	PPS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2							
U2RX	PPS	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	PPS	O	—	UART2 Transmit
U2CTS	PPS	PPS	PPS	PPS	I	ST	UART2 Clear To Send
U2RTS	PPS	PPS	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3							
U3RX	PPS	PPS	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	PPS	PPS	O	—	UART3 Transmit
U3CTS	PPS	PPS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4							
U4RX	PPS	PPS	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	PPS	PPS	O	—	UART4 Transmit
U4CTS	PPS	PPS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5							
U5RX	PPS	PPS	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	PPS	PPS	O	—	UART5 Transmit
U5CTS	PPS	PPS	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS	PPS	PPS	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6							
U6RX	PPS	PPS	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	PPS	PPS	O	—	UART6 Transmit
U6CTS	PPS	PPS	PPS	PPS	I	ST	UART6 Clear to Send
U6RTS	PPS	PPS	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY(1,2)



Note 1: Memory areas are not shown to scale.
2: The Cache, MMU, and TLB are initialized by compiler start-up code.
3: RAM memory is divided into two equal banks: RAM Bank 1 and RAM Bank 2 on a half boundary.
4: The MMU must be enabled and the TLB must be set up to access this segment.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05E0	OFF040	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E4	OFF041	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E8	OFF042	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05EC	OFF043	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F0	OFF044	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F8	OFF046	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05FC	OFF047	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0600	OFF048	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0604	OFF049	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0608	OFF050	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
060C	OFF051	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0610	OFF052	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0614	OFF053	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0618	OFF054	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
061C	OFF055	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 11-12: USBFIFOx: USB FIFO DATA REGISTER 'x' ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** USB Transmit/Receive FIFO Data bits

Writes to this register loads data into the TxFIFO for the corresponding endpoint. Reading from this register unloads data from the RxFIFO for the corresponding endpoint.

Transfers may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all transfers associated with one packet must be of the same width so that data is consistently byte-, word- or double-word aligned. The last transfer may contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized

When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit

1 = External clock from T1CKI pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

REGISTER 20-4: SQI1CON: SQI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **DASSERT:** Chip Select Assert bit
1 = Chip Select is deasserted after transmission or reception of the specified number of bytes
0 = Chip Select is not deasserted after transmission or reception of the specified number of bytes

bit 21-20 **DEVSEL<1:0>:** SQI Device Select bits
11 = Reserved
10 = Reserved
01 = Select Device 1
00 = Select Device 0

bit 19-18 **LANEMODE<1:0>:** SQI Lane Mode Select bits
11 = Reserved
10 = Quad Lane mode
01 = Dual Lane mode
00 = Single Lane mode

bit 17-16 **CMDINIT<1:0>:** Command Initiation Mode Select bits
If it is Transmit, commands are initiated based on a write to the transmit register or the contents of TX FIFO. If CMDINIT is Receive, commands are initiated based on reads to the read register or RX FIFO availability.
11 = Reserved
10 = Receive
01 = Transmit
00 = Idle

bit 15-0 **TXRXCOUNT<15:0>:** Transmit/Receive Count bits
These bits specify the total number of bytes to transmit or received (based on CMDINIT)

REGISTER 20-10: SQI1TXDATA: SQI TRANSMIT DATA BUFFER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **TXDATA<31:0>:** Transmit Command Data bits

Data is loaded into this register before being transmitted. Just prior to the beginning of a data transfer, the data in TXDATA is loaded into the shift register (SFDR).

Multiple writes to TXDATA can occur even while a transfer is already in progress. There can be a maximum of eight commands that can be queued.

REGISTER 20-11: SQI1RXDATA: SQI RECEIVE DATA BUFFER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **RXDATA<31:0>:** Receive Data Buffer bits

At the end of a data transfer, the data in the shift register is loaded into the RXDATA register. This register works like a FIFO. The depth of the receive buffer is eight words. These bits indicate the starting write block address for an erase operation.

REGISTER 20-22: SQI1INTSEN: SQI INTERRUPT SIGNAL ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	PKT DONEISE	BD DONEISE	CON THRISE
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10 **PKTDONEISE:** Receive Error Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 9 **BDDONEISE:** Transmit Error Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 8 **CONTHRISE:** Control Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 7 **CONEMPTYISE:** Control Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 6 **CONFULLISE:** Control Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 5 **RXTHRISE:** Receive Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 4 **RXFULLISE:** Receive Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 3 **RXEMPTYISE:** Receive Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 2 **TXTHRISE:** Transmit Buffer Threshold Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 1 **TXFULLISE:** Transmit Buffer Full Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

bit 0 **TXEMPTYISE:** Transmit Buffer Empty Interrupt Signal Enable bit
- 1 = Interrupt signal is enabled
- 0 = Interrupt signal is disabled

REGISTER 28-1: AD1CON1: ADC1 CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FILTRDLY<4:0>					STRGSRC<4:2>		
23:16	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	STRGSRC<1:0>		—	—	—	EIE<2:0>(1)		
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0
	ADCEN(2,4)	—	ADSIDL	—	FRACT	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **FILTRDLY<4:0>:** Oversampling Digital Filter Delay bits
Specifies the sampling time for subsequent automatic triggers when using the Oversampling Digital Filter. Sample time is 1.5 + FILTRDLY<4:0> TAD.
11111 = Sample time is 32.5 TAD
11110 = Sample time is 31.5 TAD
•
•
•
00001 = Sample time is 2.5 TAD
00000 = Sample time is 1.5 TAD

bit 26-22 **STRGSRC<4:0>:** Scan Trigger Source Select bits
11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 COUT(3)
01011 = Comparator 1 COUT(3)
01010 = OCMP5(3)
01001 = OCMP3(3)
01000 = OCMP1(3)
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0
00011 = Reserved
00010 = Reserved
00001 = Global software trigger (GSWTRG)
00000 = No trigger

Note 1: The early interrupt feature should not be used if polling any of the ARDY bits to determine if the conversion is complete. Early interrupts should be used only when all results from the ADC module are retrieved using an individual interrupt routine to fetch ADC results.

2: The ADCEN bit should be set only after the ADC module has been configured. Changing ADC Configuration bits when ADCEN = 1, will result in unpredictable behavior. When ADCEN = 0, the ADC clocks are disabled, the internal control logic is reset, and all status flags used by the module are cleared. However, the SFRs are available for reading and writing.

3: The rising edge of the module output signal triggers an ADC conversion. See Figure 18-1 in **Section 18.0 "Output Compare"** and Figure 31-1 in **Section 31.0 "Comparator"** for more information.

4: See **28.1 "ADC Configuration Requirements"** for detailed ADC calibration information.

Note: The ADC module is not available for normal operations until the ADCRDY bit (AD1CON2<31>) is set.

REGISTER 28-1: AD1CON1: ADC1 CONTROL REGISTER 1 (CONTINUED)

bit 21-19 **Unimplemented:** Read as '0'

bit 18-16 **EIE<2:0>:** Early Interrupt Enable bits(1)
These bits select the number of clocks prior to the actual arrival of valid data when the associated ARDYx bit is set. Since the ARDYx bit triggers an interrupt, these bits allow for early interrupt generation.
111 = The data ready bit, ARDYx, is set 7 TAD clocks prior to when the data is ready
110 = The data ready bit, ARDYx, is set 6 TAD clocks prior to when the data is ready
101 = The data ready bit, ARDYx, is set 5 TAD clocks prior to when the data is ready
100 = The data ready bit, ARDYx, is set 4 TAD clocks prior to when the data is ready
011 = The data ready bit, ARDYx, is set 3 TAD clocks prior to when the data is ready
010 = The data ready bit, ARDYx, is set 2 TAD clocks prior to when the data is ready
001 = The data ready bit, ARDYx, is set 1 TAD clock prior to when the data is ready
000 = The data ready bit, ARDYx, when the data is ready

bit 15 **ADCEN:** ADC Operating Mode bit(2,4)
1 = ADC module is enabled
0 = ADC module is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **FRACT:** Fractional Data Output Format bit
1 = Fractional
0 = Integer

bit 10-0 **Unimplemented:** Read as '0'

Note 1: The early interrupt feature should not be used if polling any of the ARDY bits to determine if the conversion is complete. Early interrupts should be used only when all results from the ADC module are retrieved using an individual interrupt routine to fetch ADC results.

2: The ADCEN bit should be set only after the ADC module has been configured. Changing ADC Configuration bits when ADCEN = 1, will result in unpredictable behavior. When ADCEN = 0, the ADC clocks are disabled, the internal control logic is reset, and all status flags used by the module are cleared. However, the SFRs are available for reading and writing.

3: The rising edge of the module output signal triggers an ADC conversion. See Figure 18-1 in **Section 18.0 "Output Compare"** and Figure 31-1 in **Section 31.0 "Comparator"** for more information.

4: See **28.1 "ADC Configuration Requirements"** for detailed ADC calibration information.

Note:	The ADC module is not available for normal operations until the ADCRDY bit (AD1CON2<31>) is set.

REGISTER 28-4: AD1IMOD: ADC1 INPUT MODE CONTROL REGISTER (CONTINUED)

bit 11-10 **SH5MOD<1:0>:** Input Configuration for S&H 5 (SH5) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 9-8 **SH4MOD<1:0>:** Input Configuration for S&H 4 (SH4) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 7-6 **SH3MOD<1:0>:** Input Configuration for S&H 3 (SH3) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 5-4 **SH2MOD<1:0>:** Input Configuration for S&H 2 (SH2) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 3-2 **SH1MOD<1:0>:** Input Configuration for S&H 1 (SH1) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

bit 1-0 **SH0MOD<1:0>:** Input Configuration for S&H 0 (SH0) Select bits
11 = Differential inputs, two's complement (signed) data output
10 = Differential inputs, unipolar encoded (unsigned) data output
01 = Single ended inputs, two's complement (signed) data output
00 = Single ended inputs, unipolar encoded (unsigned) data output

Note 1: Alternate inputs are only available for Class 1 Inputs.
2: When an alternate input is selected (SHxALT<1:0> ≠ 0), the data, status, and control registers for the default Class 1 input are still used. Selecting an alternate input changes the physical input source only.

REGISTER 28-18: AD1DATAn: ADC1 DATA OUTPUT REGISTER ('n' = 0 through 44)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** Data Output Value bits (formatted as specified by the SHxMOD<1:0> bits for the associated S&H circuits and the FRACT bit)

Note: AD1DATAn = ANx, where 'x' and 'n' =0-42, AD1DATA 43 = IVREF, and AD1DATA44 = IVTEMP.

34.3 On-Chip Voltage Regulator

The core and digital logic for all PIC32MZ EC devices is designed to operate at a nominal 1.8V. To simplify system designs, devices in the PIC32MZ EC family incorporate an on-chip regulator providing the required core logic voltage from VDD.

34.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

34.3.2 ON-CHIP REGULATOR AND BOR

PIC32MZ EC devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 37.1 "DC Characteristics"**.

34.4 On-chip Temperature Sensor

PIC32MZ EC devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **Section 37.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **Section 28.0 "Pipelined Analog-to-Digital Converter (ADC)"** for more information).

34.5 Programming and Diagnostics

PIC32MZ EC devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 34-1: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS

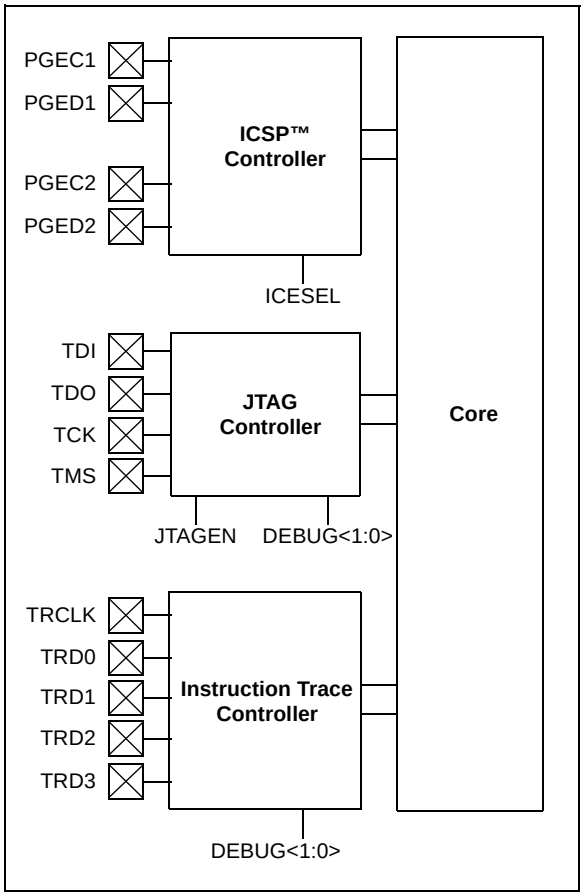


FIGURE 37-30: EJTAG TIMING CHARACTERISTICS

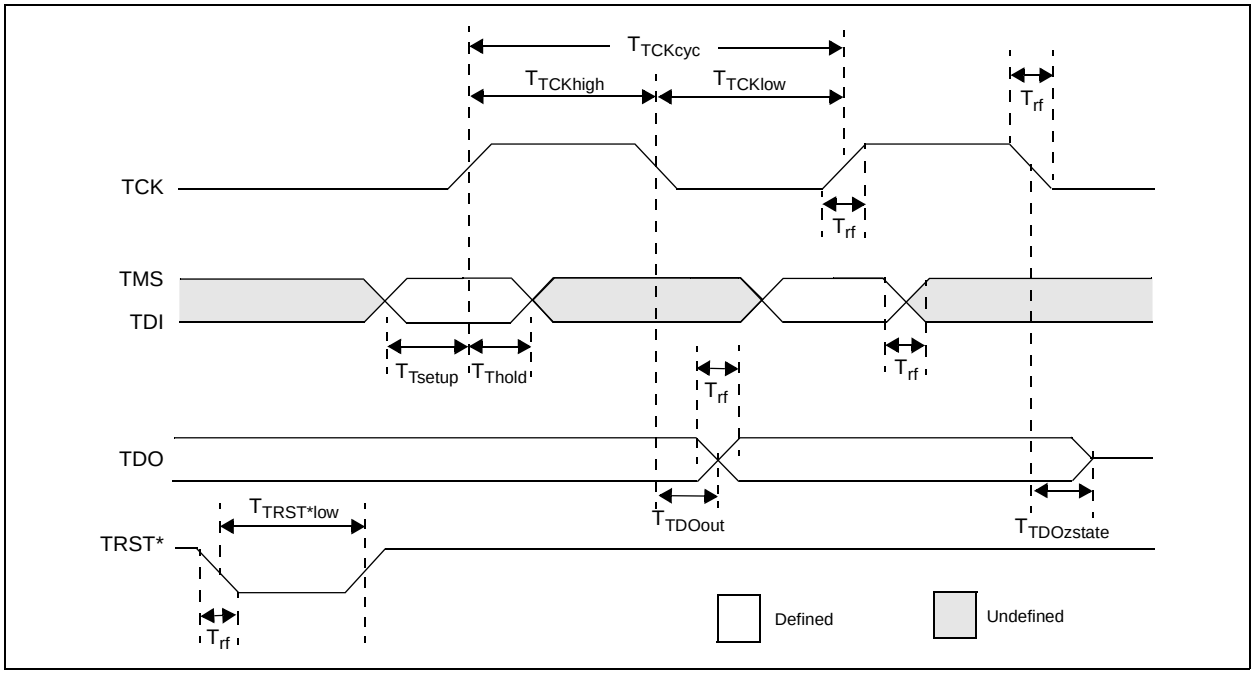


TABLE 37-48: EJTAG TIMING REQUIREMENTS

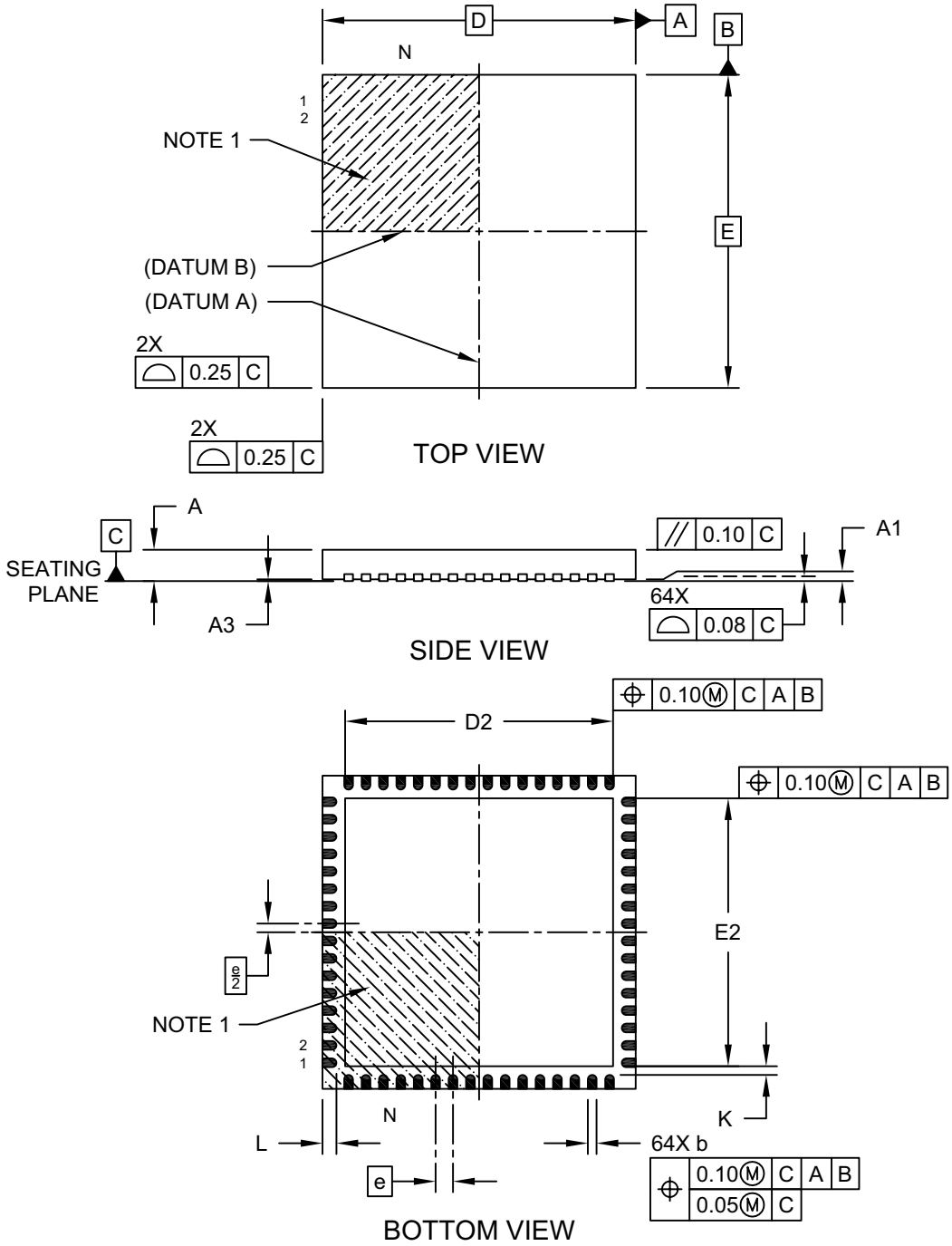
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	**Symbol**	**Description(1)**	**Min.**	**Max.**	**Units**	**Conditions**
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

39.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.70 x 7.70 Exposed Pad [QFN]

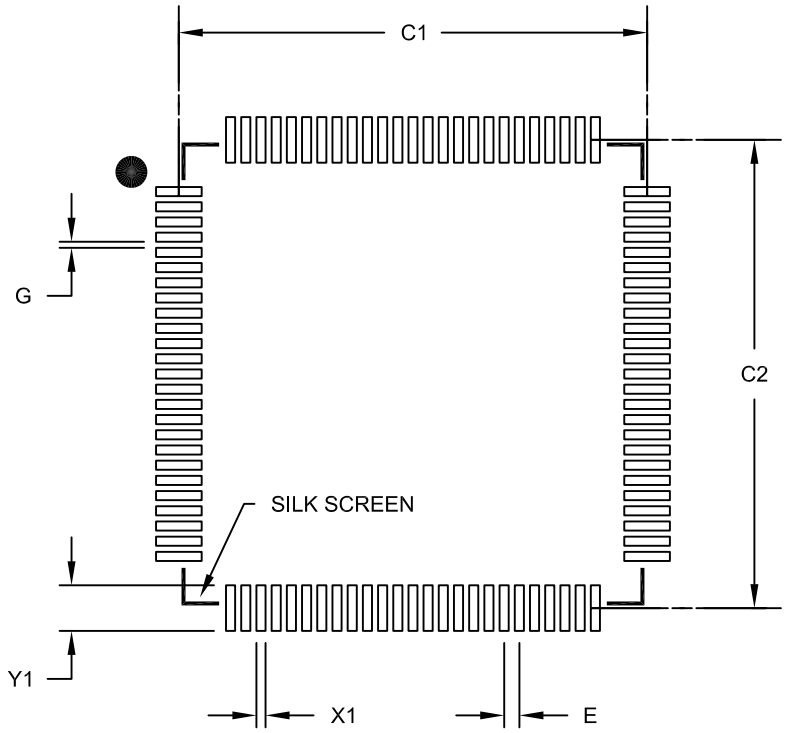
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-213B Sheet 1 of 2

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

A.2 Analog-to-Digital Converter (ADC)

The PIC32MZ family of devices has a new Pipelined ADC module that replaces the 10-bit ADC module in PIC32MX5XX/6XX/7XX devices; therefore, the use of **Bold** type to show differences is *not* used in the following table. Note that not all register differences are described in this section; however, the key feature differences are listed in Table A-3.

TABLE A-3: ADC DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
Clock Selection and Operating Frequency (TAD)	
On PIC32MX devices, the ADC clock was derived from either the FRC or from the PBCLK. ADRC (AD1CON3<15>) 1 = FRC clock 0 = Clock derived from Peripheral Bus Clock (PBCLK)	On PIC32MZ devices, the three possible sources of the ADC clock are FRC, REFCLKO3, and SYSCLK. ADCSEL<1:0> (AD1CON1<9:8>) 11 = FRC 10 = REFCLKO3 01 = SYSCLK 00 = Reserved
On PIC32MX devices, if the ADC clock was derived from the PBCLK, that frequency was divided further down, with a maximum divisor of 512, and a minimum divisor of two. ADCS<7:0> (AD1CON3<7:0>) 11111111 = 512 * TPB = TAD • • • 00000001 = 4 * TPB = TAD 00000000 = 2 * TPB = TAD	On PIC32MZ devices, any ADC clock source can be divided down, with a maximum divisor of 254. The input clock can also be fed directly to the ADC. ADCDIV<6:0> (AD1CON1<6:0>) 1111111 = 254 * TQ = TAD • • • 0000011 = 6 * TQ = TAD 0000010 = 4 * TQ = TAD 0000001 = 2 * TQ = TAD 0000000 = TQ = TAD
Scan Trigger Source	
On PIC32MX devices, there are four sources that can trigger a scan conversion in the ADC module: Auto, Timer3, INT0, and clearing the SAMP bit. SSRC<2:0> (AD1CON1<7:5>) 111 = Auto convert 110 = Reserved 101 = Reserved 100 = Reserved 011 = Reserved 010 = Timer3 period match 001 = Active transition on INT0 pin 000 = Clearing SAMP bit	On PIC32MZ devices, the list of sources for triggering a scan conversion has been expanded to include the comparators, Output Compare, and two additional Timers. In addition, trigger sources can be simulated by setting the RQCNVRT (AD1CON3<29>) bit. STRGSRC<4:0> (AD1CON1<26:22>) 11111 = Reserved • • • 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 00011 = Reserved 00010 = Reserved 00001 = Global software trigger (GSWTRG) 00000 = No trigger

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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