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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ech144-i-pl

PIC32MZ Embedded Connectivity (EC) Family

NOTES:

TABLE 4-13: SYSTEM BUS TARGET 5 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
9420	SBT5ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>				0000
9424	SBT5ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>			0000
9428	SBT5ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9430	SBT5ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9438	SBT5ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9440	SBT5REG0	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
9450	SBT5RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
9458	SBT5WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
9460	SBT5REG1	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
9470	SBT5RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
9478	SBT5WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
9480	SBT5REG2	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
9490	SBT5RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
9498	SBT5WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
0600	NVMCON ⁽⁴⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	SWAP	—	—	—	NVMOP<3:0>				0000	
0610	NVMKEY	31:16	NVMKEY<31:0>																0000	
		15:0																	0000	
0620	NVMADDR ⁽⁴⁾	31:16	NVMADDR<31:0>																0000	
		15:0																	0000	
0630	NVMDATA0	31:16	NVMDATA0<31:0>																0000	
		15:0																	0000	
0640	NVMDATA1	31:16	NVMDATA1<31:0>																0000	
		15:0																	0000	
0650	NVMDATA2	31:16	NVMDATA2<31:0>																0000	
		15:0																	0000	
0660	NVMDATA3	31:16	NVMDATA3<31:0>																0000	
		15:0																	0000	
0670	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000	
		15:0																	0000	
0680	NVMPWP ⁽⁴⁾	31:16	PWPLOCK	—	—	—	—	—	—	—	PWP<23:16>									8000
		15:0	PWP<15:0>																0000	
0690	NVMBWP ⁽⁴⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	LBWPLOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPLOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1240	RCON	31:16	—	—	—	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	—	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR	0000
1250	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
1260	RNMICON	31:16	—	—	—	—	—	—	DMTO	WDTO	SWNMI	—	—	—	—	—	CF	WDTS	0000
		15:0	—	—	—	—	—	—	—	—	NMICNT<7:0>								0000
1270	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VREGS	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

10.1 DMA Control Registers

TABLE 10-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	0000	
1010	DMASTAT	31:16	RDWR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	DMACH<2:0>			0000	
1020	DMAADDR	31:16	DMAADDR<31:0>															0000	
		15:0	DMAADDR<31:0>															0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 10-2: DMA CRC REGISTER MAP

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
1030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>		0000
1040	DCRCDATA	31:16	DCRCDATA<31:0>															0000
		15:0																0000
1050	DCRCXOR	31:16	DCRCXOR<31:0>															0000
		15:0																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 VBUSERRIE	R/W-0 SESSRQIE	R/W-0 DISCONIE	R/W-0 CONNIE	R/W-0 SOFIE	R/W-1 RESETIE	R/W-1 RESUMEIE	R/W-0 SUSPIE
23:16	R-0, HS VBUSERRIF	R-0, HS SESSRQIF	R-0, HS DISCONIF	R-0, HS CONNIF	R-0, HS SOFIF	R-0, HS RESETIF	R-0, HS RESUMEIF	R-0, HS SUSPIF
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/W-1 EP7RXIE	R/W-1 EP6RXIE	R/W-1 EP5RXIE	R/W-1 EP4RXIE	R/W-1 EP3RXIE	R/W-1 EP2RXIE	R/W-1 EP1RXIE	U-0 —

Legend:

R = Readable bit

-n = Value at POR

HS = Hardware Settable

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **VBUSERRIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled
- bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled
- bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled
- bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled
- bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled
- bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled
- bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled
- bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled
- bit 23 **VBUSERRIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt
- bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected
- bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected
- bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

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REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXDPB	RXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXDPB	TXFIFOSZ<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	TXEDMA	RXEDMA
7:0	R-1	R-0	R-0	R-0	R-0	R-0	R/W-0, HC	R/W-0
	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **RXDPB:** RX Endpoint Double-packet Buffering Control bit

1 = Double-packet buffer is supported. This doubles the size set in RXFIFOSZ.

0 = Double-packet buffer is not supported

bit 27-24 **RXFIFOSZ<3:0>:** RX Endpoint FIFO Packet Size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved

•
•
•

1010 = Reserved

1001 = 4096 bytes

1000 = 2048 bytes

0111 = 1024 bytes

0110 = 512 bytes

0101 = 256 bytes

0100 = 128 bytes

0011 = 64 bytes

0010 = 32 bytes

0001 = 16 bytes

0000 = 8 bytes

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **TXDPB:** TX Endpoint Double-packet Buffering Control bit

1 = Double-packet buffer is supported. This doubles the size set in TXFIFOSZ.

0 = Double-packet buffer is not supported

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REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 0 **SESSION:** Active Session Control/Status bit

'A' device:

 1 = Start a session

 0 = End a session

'B' device:

 1 = (Read) Session has started or is in progress, (Write) Initiate the Session Request Protocol

 0 = When USB module is in Suspend mode, clearing this bit will cause a software disconnect

Clearing this bit when the USB module is not suspended will result in undefined behavior.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 12-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[pin name]R Value to RPN Pin Selection
INT1	INT1R	INT1R<3:0>	0000 = RPD1 0001 = RPG9 0010 = RPB14 0011 = RPD0 0100 = Reserved 0101 = RPB6 0110 = RPD5 0111 = RPB2 1000 = RPF3 1001 = RPF13 ⁽¹⁾ 1010 = No Connect 1011 = RPF2 ⁽¹⁾ 1100 = RPC2 ⁽¹⁾ 1101 = RPE8 ⁽¹⁾ 1110 = Reserved 1111 = Reserved
T4CK	T4CKR	T4CKR<3:0>	
T9CK	T9CKR	T9CKR<3:0>	
IC1	IC1R	IC1R<3:0>	
IC6	IC6R	IC6R<3:0>	
U3CTS	U3CTSR	U3CTSR<3:0>	
U4RX	U4RXR	U4RXR<3:0>	
U6RX	U6RXR	U6RXR<3:0>	
SS2	SS2R	SS2R<3:0>	
SDI6 ⁽¹⁾	SDI6R ⁽¹⁾	SDI6R<3:0> ⁽¹⁾	
OCFA	OCFAR	OCFAR<3:0>	
REFCLKI3	REFCLKI3R	REFCLKI3R<3:0>	

Note 1: This selection is not available on 64-pin devices.

2: This selection is not available on 64-pin or 100-pin devices.

3: This selection is not available on devices without a CAN module.

TABLE 12-21: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14DC	SS6R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS6R<3:0>				0000
14E0	C1RXR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C1RXR<3:0>				0000
14E4	C2RXR ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C2RXR<3:0>				0000
14E8	REFCLKI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI1R<3:0>				0000
14F0	REFCLKI3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI3R<3:0>				0000
14F4	REFCLKI4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI4R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
2: This register is not available on devices without a CAN module.

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REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9) (CONTINUED)

- bit 2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit⁽¹⁾
 1 = External clock from TxCK pin
 0 = Internal peripheral clock
- bit 0 **Unimplemented:** Read as '0'

- Note 1:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.
- 2:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.
- 3:** This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

PIC32MZ Embedded Connectivity (EC) Family

17.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Input Capture”** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

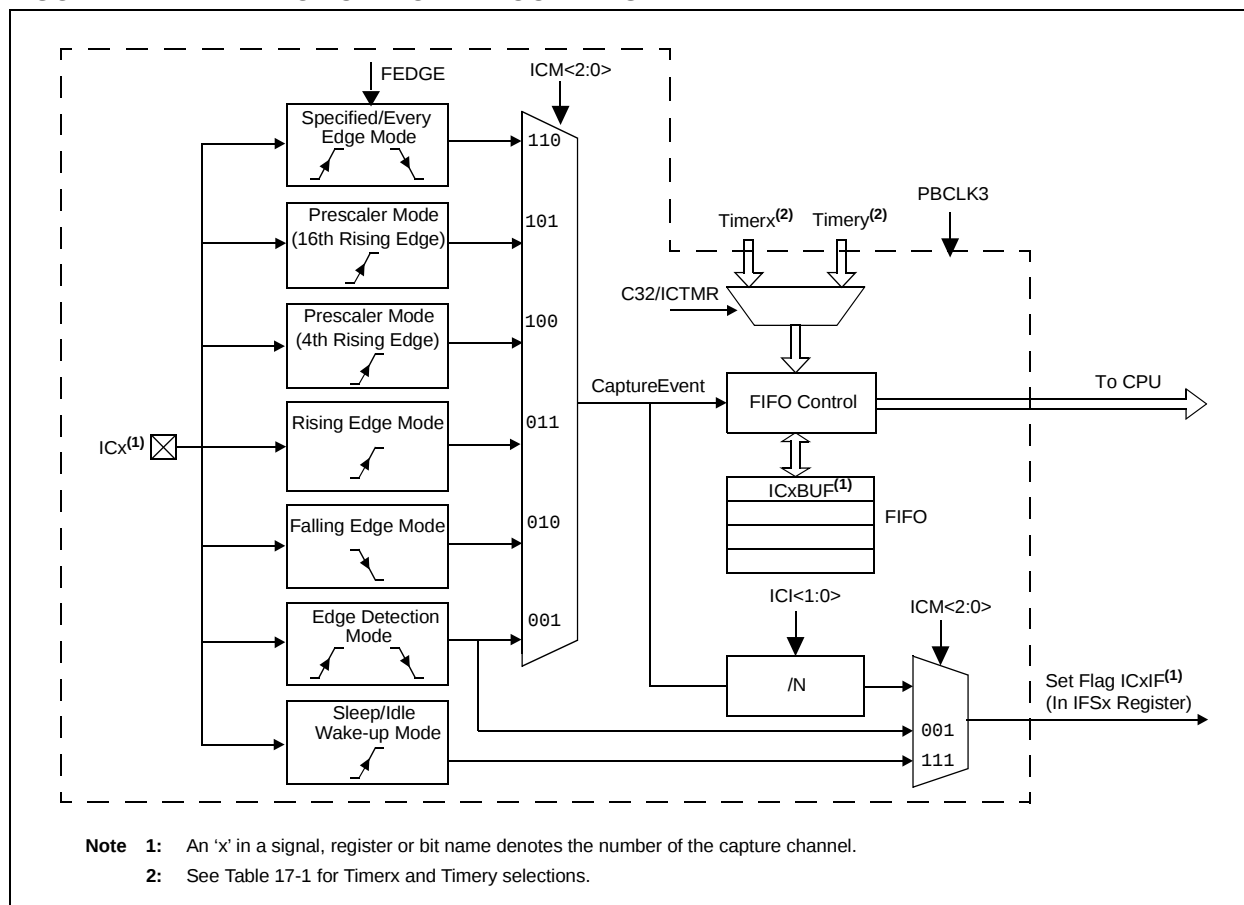
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 17-1: INPUT CAPTURE BLOCK DIAGRAM



25.1 RTCC Control Registers

TABLE 25-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0	
0C00	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000	
		15:0	ON	—	SIDL	—	—	RTCCLKSEL<1:0>		RTCOUSEL<1:0>		RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTC0E	0000	
0C10	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>					ARPT<7:0>							0000	
0C20	RTCTIME	31:16	—	—	HR10<1:0>			HR01<3:0>				—	MIN10<2:0>			MIN01<3:0>				xxxx
		15:0	—	SEC10<2:0>					SEC01<3:0>				—	—	—	—	—	—	—	xx00
0C30	RTCDATE	31:16	YEAR10<3:0>					YEAR01<3:0>				—	—	—	MONTH10	MONTH01<3:0>				xxxx
		15:0	—	—	DAY10<1:0>			DAY01<3:0>				—	—	—	—	—	WDAY01<2:0>			xx00
0C40	ALRMTIME	31:16	—	—	HR10<1:0>			HR01<3:0>				—	MIN10<2:0>			MIN01<3:0>				xxxx
		15:0	—	SEC10<2:0>					SEC01<3:0>				—	—	—	—	—	—	—	xx00
0C50	ALRMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MONTH10	MONTH01<3:0>				00xx	
		15:0	—	—	DAY10<1:0>			DAY01<3:0>				—	—	—	—	—	WDAY01<2:0>			xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

27.0 RANDOM NUMBER GENERATOR (RNG)

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. “Crypto Engine (CE) and Random Number Generator (RNG)”** (DS60001246), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Random Number Generator (RNG) core implements a thermal noise-based, True Random Number Generator (TRNG) and a cryptographically secure Pseudo-Random Number Generator (PRNG).

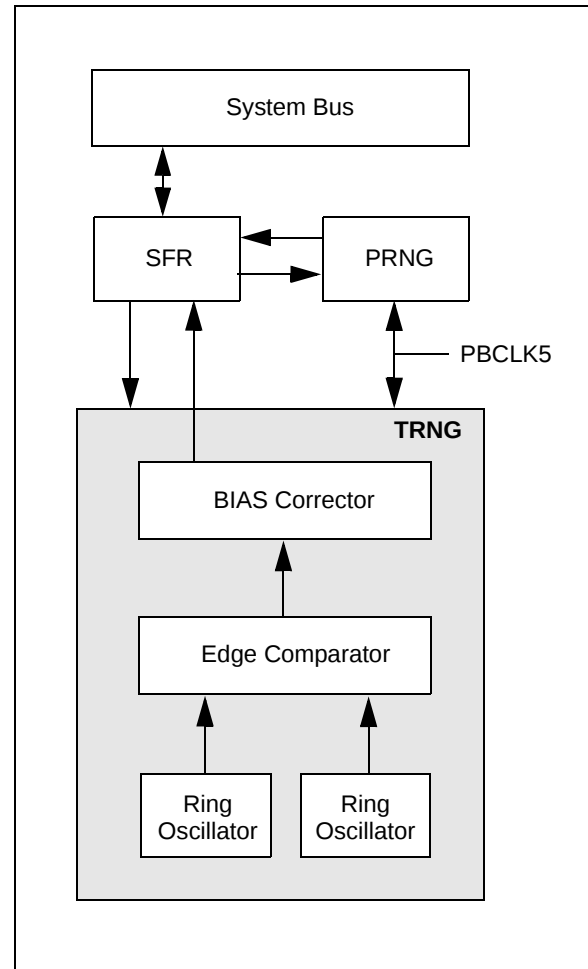
The TRNG uses multiple ring oscillators and the inherent thermal noise of integrated circuits to generate true random numbers that can initialize the PRNG.

The PRNG is a flexible LSFR, which is capable of manifesting a maximal length LFSR of up to 64-bits.

The following are some of the key features of the Random Number Generator:

- TRNG:
 - Up to 25 Mbps of random bits
 - Multi-Ring Oscillator based design
 - Built-in Bias Corrector
- PRNG:
 - LSFR-based
 - Up to 64-bit polynomial length
 - Programmable polynomial
 - TRNG can be seed value

TABLE 27-1: RANDOM NUMBER GENERATOR BLOCK DIAGRAM



PIC32MZ Embedded Connectivity (EC) Family

REGISTER 27-1: RNGVER: RANDOM NUMBER GENERATOR VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **ID<15:0>**: Block Identification bits

bit 15-8 **VERSION<7:0>**: Block Version bits

bit 7-0 **REVISION<7:0>**: Block Revision bits

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 29-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN7	MSEL7<1:0>		FSEL7<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN6	MSEL6<1:0>		FSEL6<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN5	MSEL5<1:0>		FSEL5<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN4	MSEL4<1:0>		FSEL4<4:0>				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **FLTEN7:** Filter 7 Enable bit

- 1 = Filter is enabled
- 0 = Filter is disabled

bit 30-29 **MSEL7<1:0>:** Filter 7 Mask Select bits

- 11 = Acceptance Mask 3 selected
- 10 = Acceptance Mask 2 selected
- 01 = Acceptance Mask 1 selected
- 00 = Acceptance Mask 0 selected

bit 28-24 **FSEL7<4:0>:** FIFO Selection bits

- 11111 = Message matching filter is stored in FIFO buffer 31
- 11110 = Message matching filter is stored in FIFO buffer 30
- .
- .
- .
- 00001 = Message matching filter is stored in FIFO buffer 1
- 00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN6:** Filter 6 Enable bit

- 1 = Filter is enabled
- 0 = Filter is disabled

bit 22-21 **MSEL6<1:0>:** Filter 6 Mask Select bits

- 11 = Acceptance Mask 3 selected
- 10 = Acceptance Mask 2 selected
- 01 = Acceptance Mask 1 selected
- 00 = Acceptance Mask 0 selected

bit 20-16 **FSEL6<4:0>:** FIFO Selection bits

- 11111 = Message matching filter is stored in FIFO buffer 31
- 11110 = Message matching filter is stored in FIFO buffer 30
- .
- .
- .
- 00001 = Message matching filter is stored in FIFO buffer 1
- 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

TABLE 30-5: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2110	ETH FRMTXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMTXOKCNT<15:0>																0000
2120	ETH SCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SCOLFRMCNT<15:0>																0000
2130	ETH MCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MCOLFRMCNT<15:0>																0000
2140	ETH FRMRXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMRXOKCNT<15:0>																0000
2150	ETH FCSERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FCSERRCNT<15:0>																0000
2160	ETH ALGNERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALGNERRCNT<15:0>																0000
2200	EMAC1 CFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN	—	—	—	LOOPBACK	TXPAUSE	RXPAUSE	PASSALL	RXENABLE	0000
2210	EMAC1 CFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	EXCESS DFR	BP NOBKOFF	NOBKOFF	—	—	LONGPRE	PUREPRE	AUTOPAD	VLANPAD	PAD ENABLE	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX	4082
2220	EMAC1 IPGT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0012
2230	EMAC1 IPGR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	NB2BIPKTGP1<6:0>							—	NB2BIPKTGP2<6:0>							0C12
2240	EMAC1 CLRT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CWINDOW<5:0>							—	—	—	RETX<3:0>				370F
2250	EMAC1 MAXF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MACMAXF<15:0>																05EE
2260	EMAC1 SUPP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RESET RMII	—	—	SPEED RMII	—	—	—	—	—	—	—	—	1000
2270	EMAC1 TEST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	TESTBP	TESTPAUSE	SHRTQNTA	0000
2280	EMAC1 MCFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RESET MGMT	—	—	—	—	—	—	—	—	—	CLKSEL<3:0>				NOPRE	SCANINC	0020
2290	EMAC1 MCMD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCAN	READ	0000
22A0	EMAC1 MADR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PHYADDR<4:0>					—	—	—	REGADDR<4:0>					0100

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
- 2: Reset values default to the factory programmed value.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 30-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)

bit 7 **AUTOFC:** Automatic Flow Control bit

1 = Automatic Flow Control enabled

0 = Automatic Flow Control disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **MANFC:** Manual Flow Control bit

1 = Manual Flow Control is enabled

0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every $128 * PTV < 15:0 > / 2$ TX clock cycles until the bit is cleared.

Note: For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **BUFCDEC:** Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

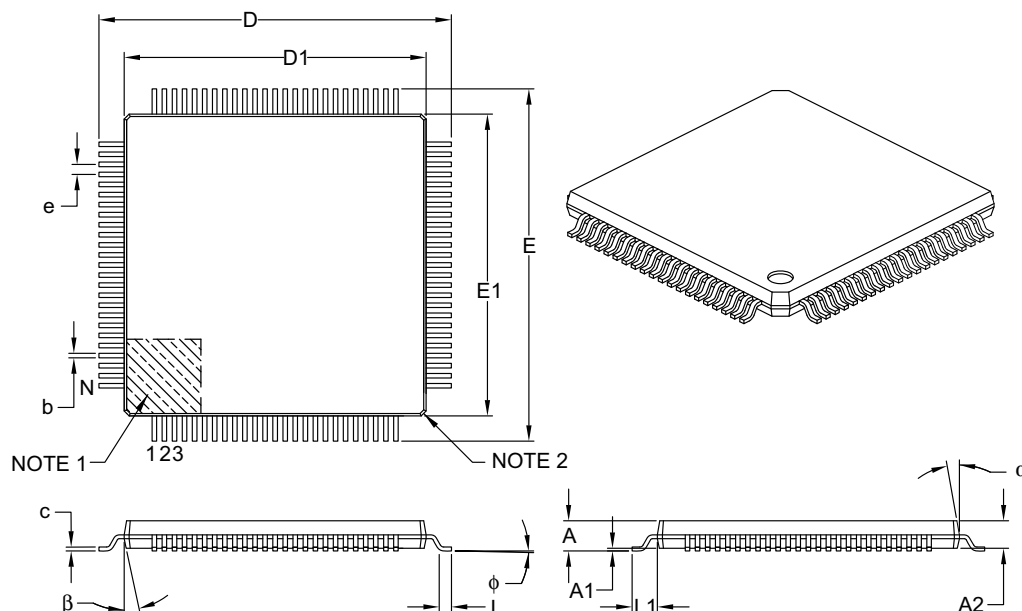
This bit is only used for RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

PIC32MZ Embedded Connectivity (EC) Family

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		100		
Lead Pitch	e		0.40 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	ϕ		0°	3.5°	7°
Overall Width	E		14.00 BSC		
Overall Length	D		14.00 BSC		
Molded Package Width	E1		12.00 BSC		
Molded Package Length	D1		12.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.13	0.18	0.23
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B