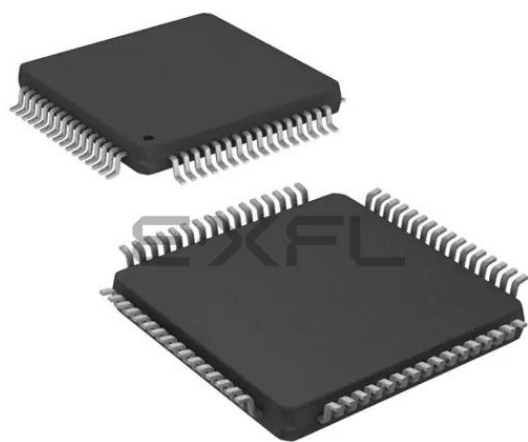




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, Ethernet, I ² C, SPI, SSI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecm064-i-pt

PIC32MZ Embedded Connectivity (EC) Family

NOTES:

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTA							
RA0	—	17	A11	22	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	B21	56	I/O	ST	
RA2	—	59	A41	85	I/O	ST	
RA3	—	60	B34	86	I/O	ST	
RA4	—	61	A42	87	I/O	ST	
RA5	—	2	B1	2	I/O	ST	
RA6	—	89	A61	129	I/O	ST	
RA7	—	90	B51	130	I/O	ST	
RA9	—	28	B15	39	I/O	ST	
RA10	—	29	A20	40	I/O	ST	
RA14	—	66	B37	95	I/O	ST	
RA15	—	67	A45	96	I/O	ST	
PORTB							
RB0	16	25	A18	36	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	A17	35	I/O	ST	
RB2	14	23	A16	34	I/O	ST	
RB3	13	22	A14	31	I/O	ST	
RB4	12	21	A13	26	I/O	ST	
RB5	11	20	B11	25	I/O	ST	
RB6	17	26	B14	37	I/O	ST	
RB7	18	27	A19	38	I/O	ST	
RB8	21	32	B18	47	I/O	ST	
RB9	22	33	A23	48	I/O	ST	
RB10	23	34	B19	49	I/O	ST	
RB11	24	35	A24	50	I/O	ST	
RB12	27	41	A27	59	I/O	ST	
RB13	28	42	B23	60	I/O	ST	
RB14	29	43	A28	61	I/O	ST	
RB15	30	44	B24	62	I/O	ST	
PORTC							
RC1	—	6	B3	6	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	A6	11	I/O	ST	
RC3	—	8	B5	12	I/O	ST	
RC4	—	9	A7	13	I/O	ST	
RC12	31	49	B28	71	I/O	ST	
RC13	47	72	B41	105	I/O	ST	
RC14	48	73	A49	106	I/O	ST	
RC15	32	50	A33	72	I/O	ST	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-12: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PMA0	30	44	B24	30	I/O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA1	29	43	A28	51	I/O	TTL/ST	Parallel Master Port Address bit 1 Input (Buffered Slave modes) and Output (Master modes)
PMA2	10	16	B9	21	O	—	Parallel Master Port Address (Demultiplexed Master modes)
PMA3	6	12	B7	52	O	—	
PMA4	5	11	A8	68	O	—	
PMA5	4	2	B1	2	O	—	
PMA6	16	6	B3	6	O	—	
PMA7	22	33	A23	48	O	—	
PMA8	42	65	A44	91	O	—	
PMA9	41	64	B36	90	O	—	
PMA10	21	32	B18	47	O	—	
PMA11	27	41	A27	29	O	—	
PMA12	24	7	A6	11	O	—	
PMA13	23	34	B19	28	O	—	
PMA14	45	61	A42	87	O	—	
PMA15	43	68	B38	97	O	—	
PMCS1	45	61	A42	87	O	—	Parallel Master Port Chip Select 1 Strobe
PMCS2	43	68	B38	97	O	—	Parallel Master Port Chip Select 2 Strobe
PMD0	58	91	B52	135	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	61	94	A64	138	I/O	TTL/ST	
PMD2	62	98	A66	142	I/O	TTL/ST	
PMD3	63	99	B56	143	I/O	TTL/ST	
PMD4	64	100	A67	144	I/O	TTL/ST	
PMD5	1	3	A3	3	I/O	TTL/ST	
PMD6	2	4	B2	4	I/O	TTL/ST	
PMD7	3	5	A4	5	I/O	TTL/ST	
PMD8	—	88	B50	128	I/O	TTL/ST	
PMD9	—	87	A60	127	I/O	TTL/ST	
PMD10	—	86	B49	125	I/O	TTL/ST	
PMD11	—	85	A59	124	I/O	TTL/ST	
PMD12	—	79	B43	112	I/O	TTL/ST	
PMD13	—	80	A54	113	I/O	TTL/ST	
PMD14	—	77	B42	110	I/O	TTL/ST	
PMD15	—	78	A53	111	I/O	TTL/ST	
PMALL	30	44	B24	30	O	—	Parallel Master Port Address Latch Enable Low Byte (Multiplexed Master modes)
PMALH	29	43	A28	51	O	—	Parallel Master Port Address Latch Enable High Byte (Multiplexed Master modes)
PMRD	53	9	A7	13	O	—	Parallel Master Port Read Strobe
PMWR	52	8	B5	12	O	—	Parallel Master Port Write Strobe

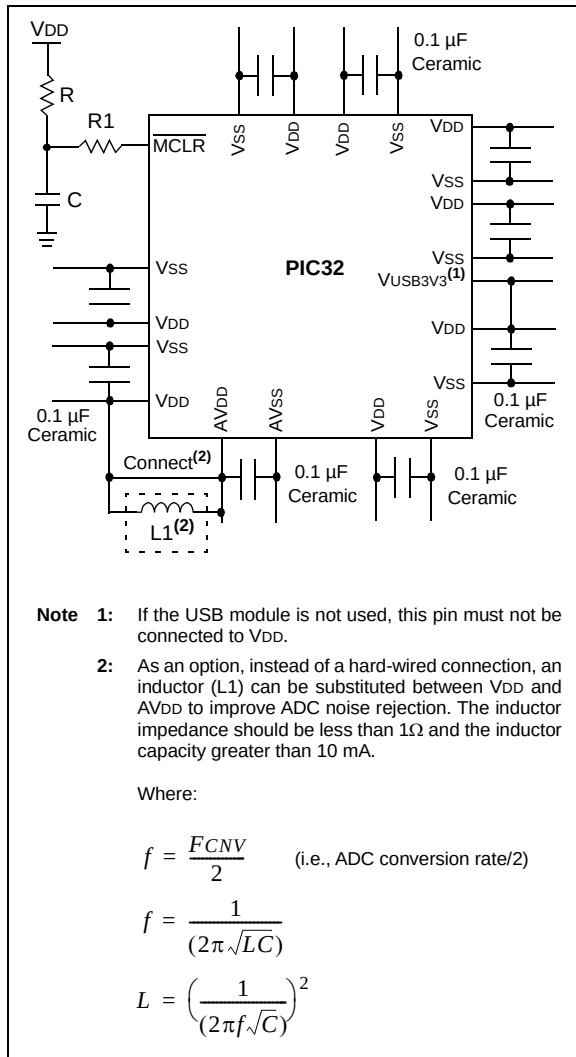
Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input

PIC32MZ Embedded Connectivity (EC) Family

Note: The PIC32MZ EC family of devices require a unique VDD ramp-up time. Please refer to parameter DC17 in Table 37-4 of **37.0 “Electrical Characteristics”** before finalizing regulator design.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 μF to 47 μF . This capacitor should be located as close to the device as possible.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

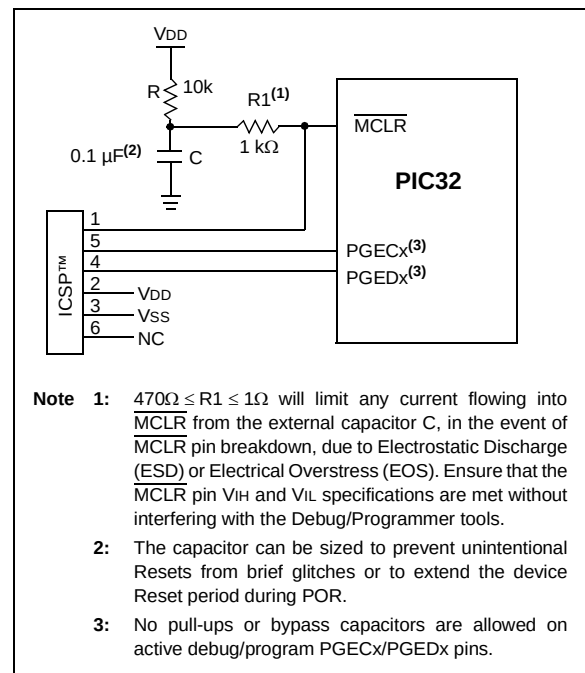
- Device Reset
- Device programming and debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS(1,2,3)



PIC32MZ Embedded Connectivity (EC) Family

TABLE 3-3: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
23	Debug	EJTAG debug register.
	TraceControl	EJTAG trace control.
	TraceControl2	EJTAG trace control 2.
	UserTraceData1	EJTAG user trace data 1 register.
	TraceBPC	EJTAG trace breakpoint register.
	Debug2	Debug control/exception status 1.
24	DEPC	Program counter at last debug exception.
	UserTraceData2	EJTAG user trace data 2 register.
25	PerfCtl0	Performance counter 0 control.
	PerfCnt0	Performance counter 0.
	PerfCtl1	Performance counter 1 control.
	PerfCnt1	Performance counter 1.
26	ErrCtl	Software test enable of way-select and data RAM arrays for I-Cache and D-Cache (microAptiv MPU only).
27	Reserved	Reserved in the PIC32 core.
28	TagLo/DataLo	Low-order portion of cache tag interface (microAptiv MPU only).
29	Reserved	Reserved in the PIC32 core.
30	ErrorEPC	Program counter at last error exception.
31	DeSave	Debug exception save.

TABLE 4-10: SYSTEM BUS TARGET 2 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
8820	SBT2ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000	
8824	SBT2ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000	
8828	SBT2ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT2ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT2ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT2REG0	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8850	SBT2RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8858	SBT2WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8860	SBT2REG1	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8870	SBT2RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8878	SBT2WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8880	SBT2REG2	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8890	SBT2RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX
8898	SBT2WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
0600	NVMCON ⁽⁴⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	SWAP	—	—	—	NVMOP<3:0>				0000	
0610	NVMKEY	31:16	NVMKEY<31:0>																0000	
		15:0																	0000	
0620	NVMADDR ⁽⁴⁾	31:16	NVMADDR<31:0>																0000	
		15:0																	0000	
0630	NVMDATA0	31:16	NVMDATA0<31:0>																0000	
		15:0																	0000	
0640	NVMDATA1	31:16	NVMDATA1<31:0>																0000	
		15:0																	0000	
0650	NVMDATA2	31:16	NVMDATA2<31:0>																0000	
		15:0																	0000	
0660	NVMDATA3	31:16	NVMDATA3<31:0>																0000	
		15:0																	0000	
0670	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000	
		15:0																	0000	
0680	NVMPWP ⁽⁴⁾	31:16	PWPLOCK	—	—	—	—	—	—	—	PWP<23:16>									8000
		15:0	PWP<15:0>																0000	
0690	NVMBWP ⁽⁴⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	LBWPLOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPLOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Parallel Master Port Error	_PMP_ERROR_VECTOR	129	OFF129<17:1>	IFS4<1>	IEC4<1>	IPC32<12:10>	IPC32<9:8>	Yes
Comparator 1 Interrupt	_COMPARATOR_1_VECTOR	130	OFF130<17:1>	IFS4<2>	IEC4<2>	IPC32<20:18>	IPC32<17:16>	No
Comparator 2 Interrupt	_COMPARATOR_2_VECTOR	131	OFF131<17:1>	IFS4<3>	IEC4<3>	IPC32<28:26>	IPC32<25:24>	No
USB General Event	_USB1_VECTOR	132	OFF132<17:1>	IFS4<4>	IEC4<4>	IPC33<4:2>	IPC33<1:0>	Yes
USB DMA Event	_USB1_DMA_VECTOR	133	OFF133<17:1>	IFS4<5>	IEC4<5>	IPC33<12:10>	IPC33<9:8>	Yes
DMA Channel 0	_DMA0_VECTOR	134	OFF134<17:1>	IFS4<6>	IEC4<6>	IPC33<20:18>	IPC33<17:16>	No
DMA Channel 1	_DMA1_VECTOR	135	OFF135<17:1>	IFS4<7>	IEC4<7>	IPC33<28:26>	IPC33<25:24>	No
DMA Channel 2	_DMA2_VECTOR	136	OFF136<17:1>	IFS4<8>	IEC4<8>	IPC34<4:2>	IPC34<1:0>	No
DMA Channel 3	_DMA3_VECTOR	137	OFF137<17:1>	IFS4<9>	IEC4<9>	IPC34<12:10>	IPC34<9:8>	No
DMA Channel 4	_DMA4_VECTOR	138	OFF138<17:1>	IFS4<10>	IEC4<10>	IPC34<20:18>	IPC34<17:16>	No
DMA Channel 5	_DMA5_VECTOR	139	OFF139<17:1>	IFS4<11>	IEC4<11>	IPC34<28:26>	IPC34<25:24>	No
DMA Channel 6	_DMA6_VECTOR	140	OFF140<17:1>	IFS4<12>	IEC4<12>	IPC35<4:2>	IPC35<1:0>	No
DMA Channel 7	_DMA7_VECTOR	141	OFF141<17:1>	IFS4<13>	IEC4<13>	IPC35<12:10>	IPC35<9:8>	No
SPI2 Fault	_SPI2_FAULT_VECTOR	142	OFF142<17:1>	IFS4<14>	IEC4<14>	IPC35<20:18>	IPC35<17:16>	Yes
SPI2 Receive Done	_SPI2_RX_VECTOR	143	OFF143<17:1>	IFS4<15>	IEC4<15>	IPC35<28:26>	IPC35<25:24>	Yes
SPI2 Transfer Done	_SPI2_TX_VECTOR	144	OFF144<17:1>	IFS4<16>	IEC4<16>	IPC36<4:2>	IPC36<1:0>	Yes
UART2 Fault	_UART2_FAULT_VECTOR	145	OFF145<17:1>	IFS4<17>	IEC4<17>	IPC36<12:10>	IPC36<9:8>	Yes
UART2 Receive Done	_UART2_RX_VECTOR	146	OFF146<17:1>	IFS4<18>	IEC4<18>	IPC36<20:18>	IPC36<17:16>	Yes
UART2 Transfer Done	_UART2_TX_VECTOR	147	OFF147<17:1>	IFS4<19>	IEC4<19>	IPC36<28:26>	IPC36<25:24>	Yes
I2C2 Bus Collision Event ⁽²⁾	_I2C2_BUS_VECTOR	148	OFF148<17:1>	IFS4<20>	IEC4<20>	IPC37<4:2>	IPC37<1:0>	Yes
I2C2 Slave Event ⁽²⁾	_I2C2_SLAVE_VECTOR	149	OFF149<17:1>	IFS4<21>	IEC4<21>	IPC37<12:10>	IPC37<9:8>	Yes
I2C2 Master Event ⁽²⁾	_I2C2_MASTER_VECTOR	150	OFF150<17:1>	IFS4<22>	IEC4<22>	IPC37<20:18>	IPC37<17:16>	Yes
Control Area Network 1	_CAN1_VECTOR	151	OFF151<17:1>	IFS4<23>	IEC4<23>	IPC37<28:26>	IPC37<25:24>	Yes
Control Area Network 2	_CAN2_VECTOR	152	OFF152<17:1>	IFS4<24>	IEC4<24>	IPC38<4:2>	IPC38<1:0>	Yes
Ethernet Interrupt	_ETHERNET_VECTOR	153	OFF153<17:1>	IFS4<25>	IEC4<25>	IPC38<12:10>	IPC38<9:8>	Yes
SPI3 Fault	_SPI3_FAULT_VECTOR	154	OFF154<17:1>	IFS4<26>	IEC4<26>	IPC38<20:18>	IPC38<17:16>	Yes
SPI3 Receive Done	_SPI3_RX_VECTOR	155	OFF155<17:1>	IFS4<27>	IEC4<27>	IPC38<28:26>	IPC38<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EC Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

- bit 26 **DATATWEN:** Data Toggle Write Enable Control bit (*Host mode*)
1 = DATATGGL can be written
0 = DATATGGL is not writable
- bit 25 **DATATGGL:** Data Toggle bit (*Host mode*)
When read, this bit indicates the current state of the endpoint data toggle.
If DATATWEN = 1, this bit may be written with the required setting of the data toggle.
If DATATWEN = 0, any value written to this bit is ignored.
- bit 24 **INCOMPRX:** Incomplete Packet Status bit
1 = The packet in the RX FIFO during a high-bandwidth Isochronous/Interrupt transfer is incomplete because parts of the data were not received
0 = Written by then software to clear this bit
In anything other than Isochronous transfer, this bit will always return '0'.
- bit 23 **CLRDT:** Clear Data Toggle Control bit
1 = Reset the endpoint data toggle to '0'
0 = Leave endpoint data toggle alone
- bit 22 **SENTSTALL:** STALL Handshake Status bit (*Device mode*)
1 = STALL handshake is transmitted
0 = Written by the software to clear this bit
- RXSTALL:** STALL Handshake Receive Status bit (*Host mode*)
1 = A STALL handshake has been received. An interrupt is generated.
0 = Written by the software to clear this bit
- bit 21 **SENDSTALL:** STALL Handshake Control bit (*Device mode*)
1 = Issue a STALL handshake
0 = Terminate stall condition
- REQPKT:** IN Transaction Request Control bit (*Host mode*)
1 = Request an IN transaction.
0 = No request
This bit is cleared when RXPKT RDY is set.
- bit 20 **FLUSH:** Flush FIFO Control bit
1 = Flush the next packet to be read from the endpoint RX FIFO. The FIFO pointer is reset and the RXPKT RDY bit is cleared. This should only be used when RXPKT RDY is set. If the FIFO is double-buffered, FLUSH may need to be set twice to completely clear the FIFO.
0 = Normal FIFO operation
This bit is automatically cleared.
- bit 19 **DATAERR:** Data Packet Error Status bit (*Device mode*)
1 = The data packet has a CRC or bit-stuff error.
0 = No data error
This bit is cleared when RXPKT RDY is cleared. This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns '0'.
- DERRNAKT:** Data Error/NAK Time-out Status bit (*Host mode*)
1 = The data packet has a CRC or bit-stuff error. In Bulk mode, the RX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK limit.
0 = No data or NAK time-out error

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-24: USBxRPC: USB ENDPOINT 'x' REQUEST PACKET COUNT REGISTER (HOST MODE ONLY) ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RQPKTCNT<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RQPKTCNT<7:0>								

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RQPKTCNT<15:0>:** Request Packet Count bits

Sets the number of packets of size MAXP that are to be transferred in a block transfer. This register is only available in *Host mode* when AUTOREQ is set.

REGISTER 11-25: USBDPBFD: USB DOUBLE PACKET BUFFER DISABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R/W-0 EP7TXD	R/W-0 EP6TXD	R/W-0 EP5TXD	R/W-0 EP4TXD	R/W-0 EP3TXD	R/W-0 EP2TXD	R/W-0 EP1TXD	U-0 —
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/W-0 EP7RXD	R/W-0 EP6RXD	R/W-0 EP5RXD	R/W-0 EP4RXD	R/W-0 EP3RXD	R/W-0 EP2RXD	R/W-0 EP1RXD	U-0 —

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-17 **EP7TXD:EP1TXD:** TX Endpoint 'x' Double Packet Buffer Disable bits

1 = TX double packet buffering is disabled for endpoint 'x'

0 = TX double packet buffering is enabled for endpoint 'x'

bit 16 **Unimplemented:** Read as '0'

bit 15-1 **EP7RXD:EP1RXD:** RX Endpoint 'x' Double Packet Buffer Disable bits

1 = RX double packet buffering is disabled for endpoint 'x'

0 = RX double packet buffering is enabled for endpoint 'x'

bit 0 **Unimplemented:** Read as '0'

TABLE 12-7: PORTD REGISTER MAP FOR 124-PIN AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD14	ANSD13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	—	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FEFF
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	—	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	—	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	—	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	—	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	—	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	—	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	—	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 18-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4A00	OC6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4A10	OC6R	31:16	OC6R<31:0>																xxxx
		15:0																	xxxx
4A20	OC6RS	31:16	OC6RS<31:0>																xxxx
		15:0																	xxxx
4C00	OC7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4C10	OC7R	31:16	OC7R<31:0>																xxxx
		15:0																	xxxx
4C20	OC7RS	31:16	OC7RS<31:0>																xxxx
		15:0																	xxxx
4E00	OC8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4E10	OC8R	31:16	OC8R<31:0>																xxxx
		15:0																	xxxx
4E20	OC8RS	31:16	OC8RS<31:0>																xxxx
		15:0																	xxxx
5000	OC9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5010	OC9R	31:16	OC9R<31:0>																xxxx
		15:0																	xxxx
5020	OC9RS	31:16 15:0	OC9RS<31:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 23-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0> ⁽¹⁾		WAITM<3:0> ⁽¹⁾				WAITE<1:0> ⁽¹⁾	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)

1 = Port is busy

0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

11 = Reserved, do not use

10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> = 11 (Addressable Slave mode only)

01 = Interrupt generated at the end of the read/write cycle

00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits

11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)

10 = Decrement ADDR<15:0> and ADDR<14> by 1 every read/write cycle⁽²⁾

01 = Increment ADDR<15:0> and ADDR<14> by 1 every read/write cycle⁽²⁾

00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit

1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer

0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits

11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<15:0>)⁽³⁾

10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, and PMD<15:0>)⁽³⁾

01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCSx, PMD<7:0>, and PMA<1:0>)

00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCSx, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits⁽¹⁾

11 = Data wait of 4 TPBCLK2; multiplexed address phase of 4 TPBCLK2

10 = Data wait of 3 TPBCLK2; multiplexed address phase of 3 TPBCLK2

01 = Data wait of 2 TPBCLK2; multiplexed address phase of 2 TPBCLK2

00 = Data wait of 1 TPBCLK2; multiplexed address phase of 1 TPBCLK2 (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK2 cycle for a write operation; WAITB = 1 TPBCLK2 cycle, WAITE = 0 TPBCLK2 cycles for a read operation.

2: Address bits 14 and 15 are not subject to auto-increment/decrement if configured as Chip Select.

3: The PMD<15:8> bits are not active if the MODE16 bit = 1.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 29-3: CiINT: CAN INTERRUPT REGISTER (CONTINUED)

- bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred
- bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred
- bit 12 **SERRIF:** System Error Interrupt Flag bit⁽¹⁾
1 = A system error occurred (typically an illegal address was presented to the System Bus)
0 = A system error has not occurred
- bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred
- bit 10-4 **Unimplemented:** Read as '0'
- bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred
- bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred
- bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending
- bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

Note 1: This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CiCON<15>).

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 30-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<7:0>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-24 **PMM<31:24>**: Pattern Match Mask 3 bits
bit 23-16 **PMM<23:16>**: Pattern Match Mask 2 bits
bit 15-8 **PMM<15:8>**: Pattern Match Mask 1 bits
bit 7-0 **PMM<7:0>**: Pattern Match Mask 0 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 30-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<39:32>							

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-24 **PMM<63:56>**: Pattern Match Mask 7 bits
bit 23-16 **PMM<55:48>**: Pattern Match Mask 6 bits
bit 15-8 **PMM<47:40>**: Pattern Match Mask 5 bits
bit 7-0 **PMM<39:32>**: Pattern Match Mask 4 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 30-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	B2BIPKTGP<6:0>						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 μ s (in 100 Mbps) or 9.6 μ s (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

PIC32MZ Embedded Connectivity (EC) Family

33.3 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 33-1 for more information.

Note: Disabling a peripheral module while its ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TABLE 33-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS⁽¹⁾

Peripheral	PMDx bit Name	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Input Capture 6	IC6MD	PMD3<5>
Input Capture 7	IC7MD	PMD3<6>
Input Capture 8	IC8MD	PMD3<7>
Input Capture 9	IC9MD	PMD3<8>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Output Compare 6	OC6MD	PMD3<21>
Output Compare 7	OC7MD	PMD3<22>
Output Compare 8	OC8MD	PMD3<23>
Output Compare 9	OC9MD	PMD3<24>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
Timer6	T6MD	PMD4<5>
Timer7	T7MD	PMD4<6>
Timer8	T8MD	PMD4<7>
Timer9	T9MD	PMD4<8>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MZ EC Family Features"** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 34-3: DEVCFG0/ADEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0 —	R/P EJTAGBEN	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
15:8	r-1 —	R/P —	R/P —	R/P —	r-1 —	R/P FSLEEP	R/P FECCCON<1:0>	R/P —
7:0	r-1 —	R/P BOOTISA	R/P TRCEN	R/P —	R/P —	R/P JTAGEN ⁽¹⁾	R/P —	R/P DEBUG<1:0>

Legend:

R = Readable bit

-n = Value at POR

r = Reserved bit

W = Writable bit

'1' = Bit is set

P = Programmable bit

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31 **Reserved:** Write as '0'

bit 30 **EJTAGBEN:** EJTAG Boot Enable bit

1 = Normal EJTAG functionality

0 = Reduced EJTAG functionality

bit 29-15 **Reserved:** Write as '1'

bit 14-12 **DBGPER<2:0>:** Debug Mode CPU Access Permission bits

1xx = Allow CPU access to Permission Group 2 permission regions

x1x = Allow CPU access to Permission Group 1 permission regions

xx1 = Allow CPU access to Permission Group 0 permission regions

0xx = Deny CPU access to Permission Group 2 permission regions

x0x = Deny CPU access to Permission Group 1 permission regions

xx0 = Deny CPU access to Permission Group 0 permission regions

When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** Write as '1'

bit 10 **FSLEEP:** Flash Sleep Mode bit

1 = Flash is powered down when the device is in Sleep mode

0 = Flash power down is controlled by the VREGS bit (PWRCON<1>)

bit 9-8 **FECCCON<1:0>:** Dynamic Flash ECC Configuration bits

Upon a device Reset, the value of these bits is copied to the ECCCON<1:0> bits (CFGCON<5:4>).

11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)

10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)

01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)

00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

bit 7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit

1 = Boot code and Exception code is MIPS32[®]

(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)

0 = Boot code and Exception code is microMIPS[™]

(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit

1 = Trace features in the CPU are enabled

0 = Trace features in the CPU are disabled

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-45: ETHERNET MODULE SPECIFICATIONS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Characteristic	Min.	Typ.	Max.	Units	Conditions
MIIM Timing Requirements						
ET1	MDC Duty Cycle	40	—	60	%	—
ET2	MDC Period	400	—	—	ns	—
ET3	MDIO Output Setup and Hold	10	—	10	ns	See Figure 37-24
ET4	MDIO Input Setup and Hold	0	—	300	ns	See Figure 37-25
MII Timing Requirements						
ET5	TX Clock Frequency	—	25	—	MHz	—
ET6	TX Clock Duty Cycle	35	—	65	%	—
ET7	ETXDx, ETEN, ETXERR Output Delay	0	—	25	ns	See Figure 37-26
ET8	RX Clock Frequency	—	25	—	MHz	—
ET9	RX Clock Duty Cycle	35	—	65	%	—
ET10	ERXDx, ERXDV, ERXERR Setup and Hold	10	—	30	ns	See Figure 37-27
RMII Timing Requirements						
ET11	Reference Clock Frequency	—	50	—	MHz	—
ET12	Reference Clock Duty Cycle	35	—	65	%	—
ET13	ETXDx, ETEN, Setup and Hold	2	—	16	ns	—
ET14	ERXDx, ERXDV, ERXERR Setup and Hold	2	—	16	ns	—

FIGURE 37-24: MDIO SOURCED BY THE PIC32 DEVICE

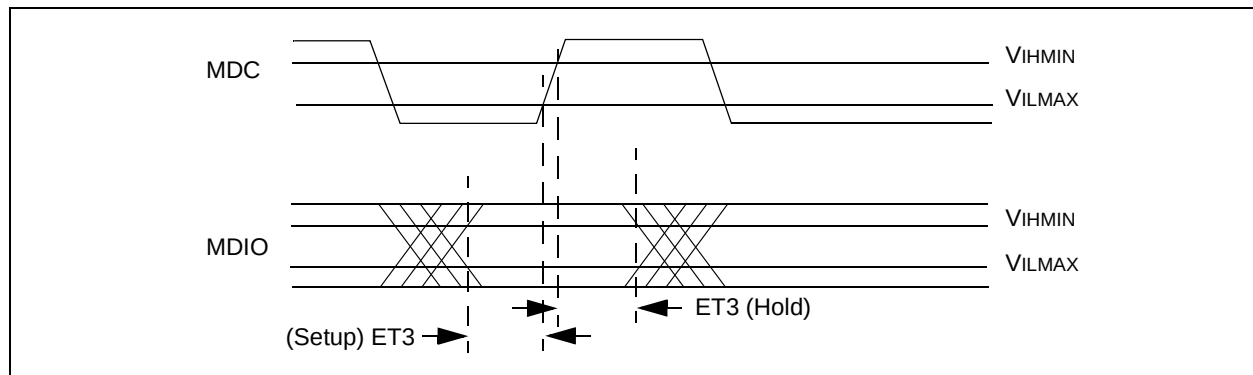
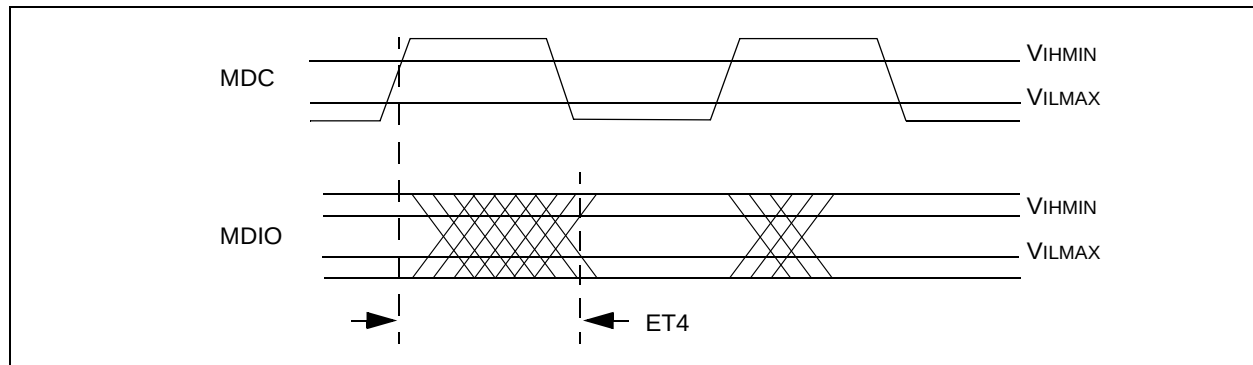


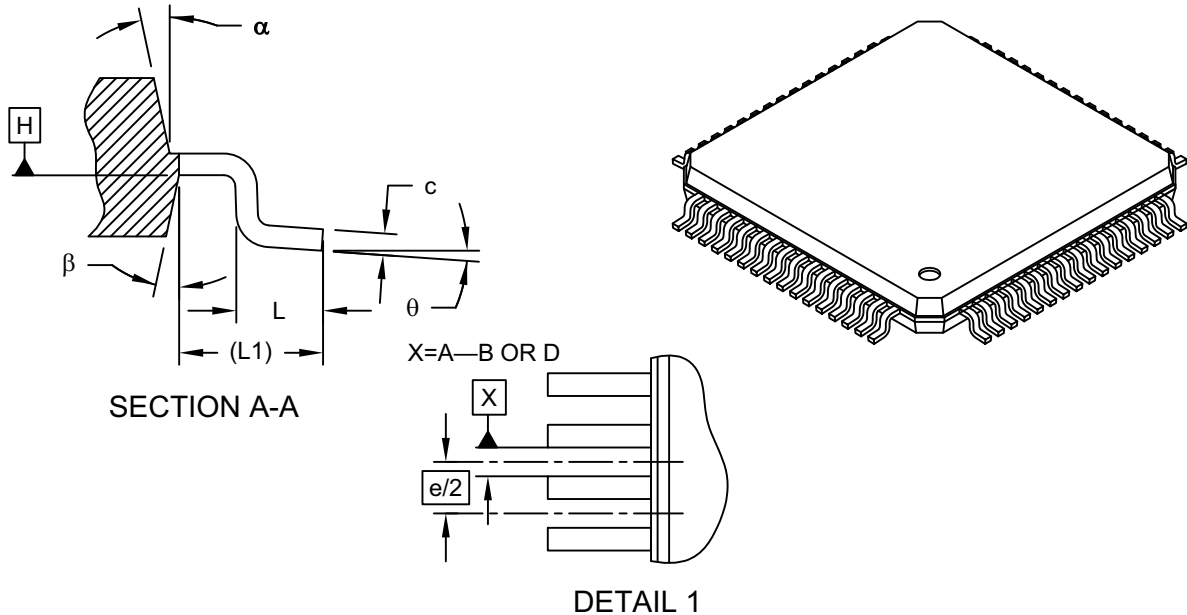
FIGURE 37-25: MDIO SOURCED BY THE PHY



PIC32MZ Embedded Connectivity (EC) Family

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	64		
Lead Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	phi	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	alpha	11°	12°	13°
Mold Draft Angle Bottom	beta	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2