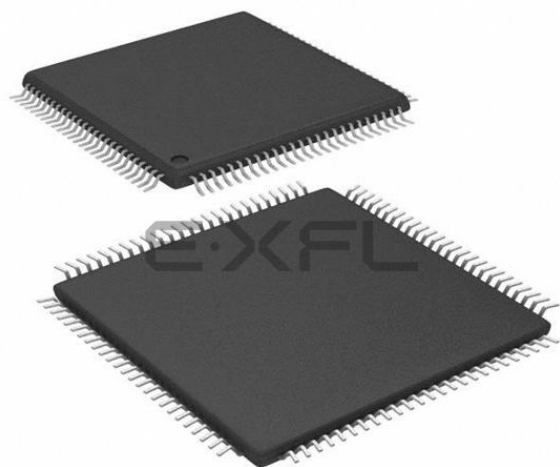




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Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecm100t-i-pt

PIC32MZ Embedded Connectivity (EC) Family

1.0 DEVICE OVERVIEW

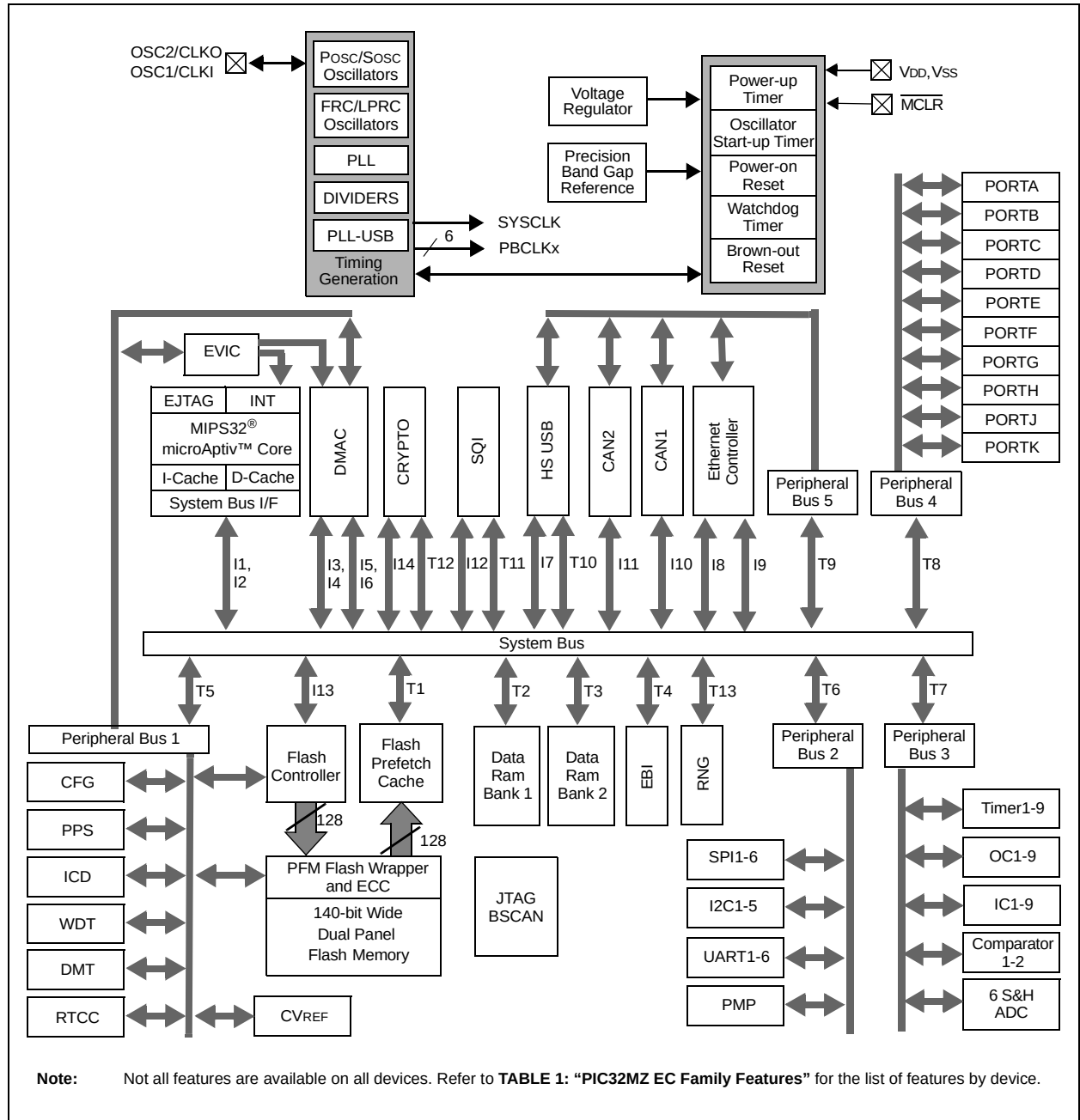
Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents provided in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This data sheet contains device-specific information for PIC32MZ Embedded Connectivity (EC) devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ EC family of devices.

Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 2 through Table 5).

FIGURE 1-1: PIC32MZ EC FAMILY BLOCK DIAGRAM



PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTA							
RA0	—	17	A11	22	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	B21	56	I/O	ST	
RA2	—	59	A41	85	I/O	ST	
RA3	—	60	B34	86	I/O	ST	
RA4	—	61	A42	87	I/O	ST	
RA5	—	2	B1	2	I/O	ST	
RA6	—	89	A61	129	I/O	ST	
RA7	—	90	B51	130	I/O	ST	
RA9	—	28	B15	39	I/O	ST	
RA10	—	29	A20	40	I/O	ST	
RA14	—	66	B37	95	I/O	ST	
RA15	—	67	A45	96	I/O	ST	
PORTB							
RB0	16	25	A18	36	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	A17	35	I/O	ST	
RB2	14	23	A16	34	I/O	ST	
RB3	13	22	A14	31	I/O	ST	
RB4	12	21	A13	26	I/O	ST	
RB5	11	20	B11	25	I/O	ST	
RB6	17	26	B14	37	I/O	ST	
RB7	18	27	A19	38	I/O	ST	
RB8	21	32	B18	47	I/O	ST	
RB9	22	33	A23	48	I/O	ST	
RB10	23	34	B19	49	I/O	ST	
RB11	24	35	A24	50	I/O	ST	
RB12	27	41	A27	59	I/O	ST	
RB13	28	42	B23	60	I/O	ST	
RB14	29	43	A28	61	I/O	ST	
RB15	30	44	B24	62	I/O	ST	
PORTC							
RC1	—	6	B3	6	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	A6	11	I/O	ST	
RC3	—	8	B5	12	I/O	ST	
RC4	—	9	A7	13	I/O	ST	
RC12	31	49	B28	71	I/O	ST	
RC13	47	72	B41	105	I/O	ST	
RC14	48	73	A49	106	I/O	ST	
RC15	32	50	A33	72	I/O	ST	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

PIC32MZ Embedded Connectivity (EC) Family

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents provided in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Note: The PIC32MZ EC family of devices require a unique VDD ramp-up time. Please refer to parameter DC17 in Table 37-4 of 37.0 “**Electrical Characteristics**” before finalizing regulator design.

Getting started with the PIC32MZ EC family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see 2.2 “**Decoupling Capacitors**”)
- All AVDD and AVSS pins, even if the ADC module is not used (see 2.2 “**Decoupling Capacitors**”)
- MCLR pin (see 2.3 “**Master Clear (MCLR) Pin**”)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming (ICSP™) and debugging purposes (see 2.4 “**ICSP Pins**”)
- OSC1 and OSC2 pins, when external oscillator source is used (see 2.7 “**External Oscillator Pins**”)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 μF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF . Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μF in parallel with 0.001 μF .
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

TABLE 4-14: SYSTEM BUS TARGET 6 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
9820	SBT6ELOG1	31:16	MULTI	—	—	—	CODE<3:0>			—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000
9824	SBT6ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9828	SBT6ECON	31:16	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9830	SBT6ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9838	SBT6ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9840	SBT6REG0	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx
9850	SBT6RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
9858	SBT6WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
9860	SBT6REG1	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx
9870	SBT6RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
9878	SBT6WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 4-16: SYSTEM BUS TARGET 8 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
A020	SBT8ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>				0000
A024	SBT8ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>			0000
A028	SBT8ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
A030	SBT8ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A038	SBT8ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A040	SBT8REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx	
A050	SBT8RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A058	SBT8WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A060	SBT8REG1	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx	
A070	SBT8RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A078	SBT8WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

bit 10-8 **NOSC<2:0>**: New Oscillator Selection bits

111 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

110 = Reserved

101 = Internal Low-Power RC (LPRC) Oscillator

100 = Secondary Oscillator (Sosc)

011 = Reserved

010 = Primary Oscillator (Posc) (HS or EC)

001 = System PLL (SPLL)

000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK**: Clock Selection Lock Enable bit

1 = Clock and PLL selections are locked

0 = Clock and PLL selections are not locked and may be modified

bit 6 **ULOCK**: USB PLL Lock Status bit

1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied

0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled

bit 5 **SLOCK**: System PLL Lock Status bit

1 = System PLL module is in lock or module start-up timer is satisfied

0 = System PLL module is out of lock, start-up timer is running or system PLL is disabled

bit 4 **SLPEN**: Sleep Mode Enable bit

1 = Device will enter Sleep mode when a WAIT instruction is executed

0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF**: Clock Fail Detect bit

1 = FSCM has detected a clock failure

0 = No clock failure has been detected

bit 2 **Unimplemented**: Read as '0'

bit 1 **SOSCEN**: Secondary Oscillator (Sosc) Enable bit

1 = Enable Secondary Oscillator

0 = Disable Secondary Oscillator

bit 0 **OSWEN**: Oscillator Switch Enable bit⁽¹⁾

1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits

0 = Oscillator switch is complete

Note 1: The reset value for this bit depends on the setting of the IESO (DEVCFG1<7>) bit. When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0, HS EP7TXIF	R-0, HS EP6TXIF	R-0, HS EP5TXIF	R-0, HS EP4TXIF	R-0, HS EP3TXIF	R-0, HS EP2TXIF	R-0, HS EP1TXIF	R-0, HS EP0IF
15:8	R/W-0 ISOUPD	R/W-0 SOFTCONN	R/W-1 HSEN	R-0, HS HSMODE	R-0 RESET	R/W-0 RESUME	R-0, HC SUSPMODE	R/W-0 SUSPEN
	—	—						
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	FUNC<6:0>						
	—	—	—	—	—	—	—	—

Legend:	HS = Hardware Settable	HC = Hardware Clearable
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-17 **EP7TXIF:EP1TXIF:** Endpoint 'n' TX Interrupt Flag bit
 1 = Endpoint has a transmit interrupt to be serviced
 0 = No interrupt event

bit 16 **EP0IF:** Endpoint 0 Interrupt bit
 1 = Endpoint 0 has an interrupt to be serviced
 0 = No interrupt event

All EPxTX and EP0 bits are cleared when the byte is read. Therefore, these bits must be read independently from the remaining bits in this register to avoid accidental clearing.

bit 15 **ISOUPD:** ISO Update bit (*Device mode only; unimplemented in Host mode*)
 1 = USB module will wait for a SOF token from the time TXPKTRDY is set before sending the packet
 0 = No change in behavior

This bit only affects endpoints performing isochronous transfers when in *Device mode*. This bit is unimplemented in *Host mode*.

bit 14 **SOFTCONN:** Soft Connect/Disconnect Feature Selection bit
 1 = The USB D+/D- lines are enabled and active
 0 = The USB D+/D- lines are disabled and are tri-stated
 This bit is only available in *Device mode*.

bit 13 **HSEN:** Hi-Speed Enable bit
 1 = The USB module will negotiate for Hi-Speed mode when the device is reset by the hub
 0 = Module only operates in Full-Speed mode

bit 12 **HSMODE:** Hi-Speed Mode Status bit
 1 = Hi-Speed mode successfully negotiated during USB reset
 0 = Module is not in Hi-Speed mode

In *Device mode*, this bit becomes valid when a USB reset completes. In *Host mode*, it becomes valid when the RESET bit is cleared.

bit 11 **RESET:** Module Reset Status bit
 1 = Reset signaling is present on the bus
 0 = Normal module operation

In *Device mode*, this bit is read-only. In *Host mode*, this bit is read/write.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 12-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD1	RPD1R	RPD1R<3:0>	0000 = No Connect 0001 = U1RTS 0010 = U2TX 0011 = U5RTS 0100 = U6TX 0101 = Reserved 0110 = SS2 0111 = Reserved 1000 = SDO4 1001 = Reserved 1010 = SDO6 ⁽¹⁾ 1011 = OC2 1100 = OC1 1101 = OC9 1110 = Reserved 1111 = C2TX ⁽³⁾
RPG9	RPG9R	RPG9R<3:0>	
RPB14	RPB14R	RPB14R<3:0>	
RPD0	RPD0R	RPD0R<3:0>	
RPB6	RPB6R	RPB6R<3:0>	
RPD5	RPD5R	RPD5R<3:0>	
RPB2	RPB2R	RPB2R<3:0>	
RPF3	RPF3R	RPF3R<3:0>	
RPF13 ⁽¹⁾	RPF13R ⁽¹⁾	RPF13R<3:0> ⁽¹⁾	
RPC2 ⁽¹⁾	RPC2R ⁽¹⁾	RPC2R<3:0> ⁽¹⁾	
RPE8 ⁽¹⁾	RPE8R ⁽¹⁾	RPE8R<3:0> ⁽¹⁾	
RPF2 ⁽¹⁾	RPF2R ⁽¹⁾	RPF2R<3:0> ⁽¹⁾	

Note 1: This selection is not available on 64-pin devices.

2: This selection is not available on 64-pin or 100-pin devices.

3: This selection is not available on devices without a CAN module.

TABLE 12-15: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	—	—	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 12-17: PORTH REGISTER MAP FOR 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0700	ANSELH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0073
0710	TRISH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISH15	TRISH14	TRISH13	TRISH12	TRISH11	TRISH10	TRISH9	TRISH8	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	FFFF
0720	PORTH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RH15	RH14	RH13	RH12	RH11	RH10	RH9	RH8	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	xxxx
0730	LATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATH15	LATH14	LATH13	LATH12	LATH11	LATH10	LATH9	LATH8	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	xxxx
0740	ODCH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCH15	ODCH14	ODCH13	ODCH12	ODCH11	ODCH10	ODCH9	ODCH8	ODCH7	ODCH6	ODCH5	ODCH4	ODCH3	ODCH2	ODCH1	ODCH0	0000
0750	CNPUH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUH15	CNPUH14	CNPUH13	CNPUH12	CNPUH11	CNPUH10	CNPUH9	CNPUH8	CNPUH7	CNPUH6	CNPUH5	CNPUH4	CNPUH3	CNPUH2	CNPUH1	CNPUH0	0000
0760	CNPDH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDH15	CNPDH14	CNPDH13	CNPDH12	CNPDH11	CNPDH10	CNPDH9	CNPDH8	CNPDH7	CNPDH6	CNPDH5	CNPDH4	CNPDH3	CNPDH2	CNPDH1	CNPDH0	0000
0770	CNCONH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0780	CNENH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEH15	CNIEH14	CNIEH13	CNIEH12	CNIEH11	CNIEH10	CNIEH9	CNIEH8	CNIEH7	CNIEH6	CNIEH5	CNIEH4	CNIEH3	CNIEH2	CNIEH1	CNIEH0	0000
0790	CNSTATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATH15	CN STATH14	CN STATH13	CN STATH12	CN STATH11	CN STATH10	CN STATH9	CN STATH8	CN STATH7	CN STATH6	CN STATH5	CN STATH4	CN STATH3	CN STATH2	CN STATH1	CN STATH0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

TABLE 12-18: PORTJ REGISTER MAP FOR 124-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	ANSELJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ANSJ11	—	ANSJ9	ANSJ8	—	—	—	—	—	—	—	—	0B00
0810	TRISJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRISJ11	—	TRISJ9	TRISJ8	—	—	—	TRISJ4	—	TRISJ2	TRISJ1	TRISJ0	0B17
0820	PORTJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RJ11	—	RJ9	RJ8	—	—	—	RJ4	—	RJ2	RJ1	RJ0	xxxx
0830	LATJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LATJ11	—	LATJ9	LATJ8	—	—	—	LATJ4	—	LATJ2	LATJ1	LATJ0	xxxx
0840	ODCJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ODCJ11	—	ODCJ9	ODCJ8	—	—	—	ODCJ4	—	ODCJ2	ODCJ1	ODCJ0	0000
0850	CNPUJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNPUJ11	—	CNPUJ9	CNPUJ8	—	—	—	CNPUJ4	—	CNPUJ2	CNPUJ1	CNPUJ0	0000
0860	CNPDJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNPDJ11	—	CNPDJ9	CNPDJ8	—	—	—	CNPDJ4	—	CNPDJ2	CNPDJ1	CNPDJ0	0000
0870	CNCONJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0880	CNENJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CNIEJ11	—	CNIEJ9	CNIEJ8	—	—	—	CNIEJ4	—	CNIEJ2	CNIEJ1	CNIEJ0	0000
0890	CNSTATJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CN STATJ11	—	CN STATJ9	CN STATJ8	—	—	—	CN STATJ4	—	CN STATJ2	CN STATJ1	CN STATJ0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:

1 = External clock input is synchronized

0 = External clock input is not synchronized

When TCS = 0:

This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit

1 = External clock from T1CKI pin

0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON ⁽¹⁾	—	SIDL ⁽²⁾	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE ⁽¹⁾	TCKPS<2:0> ⁽¹⁾			T32 ⁽³⁾	—	TCS ⁽¹⁾	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit⁽¹⁾

1 = Module is enabled

0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit⁽²⁾

1 = Discontinue operation when device enters Idle mode

0 = Continue operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽¹⁾

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits⁽¹⁾

111 = 1:256 prescale value

110 = 1:64 prescale value

101 = 1:32 prescale value

100 = 1:16 prescale value

011 = 1:8 prescale value

010 = 1:4 prescale value

001 = 1:2 prescale value

000 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timer Mode Select bit⁽³⁾

1 = Odd numbered and even numbered timers form a 32-bit timer

0 = Odd numbered and even numbered timers form a separate 16-bit timer

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

TABLE 18-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4A00	OC6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4A10	OC6R	31:16	OC6R<31:0>																xxxx
		15:0																	xxxx
4A20	OC6RS	31:16	OC6RS<31:0>																xxxx
		15:0																	xxxx
4C00	OC7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4C10	OC7R	31:16	OC7R<31:0>																xxxx
		15:0																	xxxx
4C20	OC7RS	31:16	OC7RS<31:0>																xxxx
		15:0																	xxxx
4E00	OC8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4E10	OC8R	31:16	OC8R<31:0>																xxxx
		15:0																	xxxx
4E20	OC8RS	31:16	OC8RS<31:0>																xxxx
		15:0																	xxxx
5000	OC9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5010	OC9R	31:16	OC9R<31:0>																xxxx
		15:0																	xxxx
5020	OC9RS	31:16 15:0	OC9RS<31:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 22-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON	U-0 —	R/W-0 SIDL	R/W-0 IREN	R/W-0 RTSMD	U-0 —	R/W-0 UEN<1:0> ⁽¹⁾	R/W-0
7:0	R/W-0 WAKE	R/W-0 LPBACK	R/W-0 ABAUD	R/W-0 RXINV	R/W-0 BRGH	R/W-0 PDSEL<1:0>	R/W-0	R/W-0 STSEL

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit

1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits

0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue operation when device enters Idle mode

0 = Continue operation in Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit

1 = IrDA is enabled

0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit

1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode

0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits⁽¹⁾

11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register

10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used

01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register

00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ /UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit

1 = Wake-up enabled

0 = Wake-up disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit

1 = Loopback mode is enabled

0 = Loopback mode is disabled

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **Section 12.3 “Peripheral Pin Select (PPS)”** for more information).

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 23-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 5-2 **WAITM<3:0>**: Data Read/Write Strobe Wait States bits⁽¹⁾

1111 = Wait of 16 TPBCLK2

•
•
•

0001 = Wait of 2 TPBCLK2

0000 = Wait of 1 TPBCLK2 (default)

bit 1-0 **WAITE<1:0>**: Data Hold After Read/Write Strobe Wait States bits⁽¹⁾

11 = Wait of 4 TPBCLK2

10 = Wait of 3 TPBCLK2

01 = Wait of 2 TPBCLK2

00 = Wait of 1 TPBCLK2 (default)

For Read operations:

11 = Wait of 3 TPBCLK2

10 = Wait of 2 TPBCLK2

01 = Wait of 1 TPBCLK2

00 = Wait of 0 TPBCLK2 (default)

- Note 1:** Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK2 cycle for a write operation; WAITB = 1 TPBCLK2 cycle, WAITE = 0 TPBCLK2 cycles for a read operation.
- 2:** Address bits 14 and 15 are not subject to auto-increment/decrement if configured as Chip Select.
- 3:** The PMD<15:8> bits are not active if the MODE16 bit = 1.

PIC32MZ Embedded Connectivity (EC) Family

NOTES:

TABLE 29-2: CAN2 REGISTER SUMMARY FOR PIC32MZXXXECF AND PIC32MZXXXECH DEVICES

Virtual Address (BF88_#)	Register Name(d)	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
1000	C2CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480	
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>				0000		
1010	C2CFG	31:16	—	—	—	—	—	—	—	—	WAKFIL		—	—	—	SEG2PH<2:0>			0000	
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>					0000		
1020	C2INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000	
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000	
1030	C2VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>						0040		
1040	C2TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000	
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000	
1050	C2FSTAT	31:16	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16	0000	
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000	
1060	C2RXOVF	31:16	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000	
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000	
1070	C2TMR	31:16	CANTS<15:0>																0000	
		15:0	CANTSPRE<15:0>																0000	
1080	C2RXM0	31:16	SID<10:0>													MIDE			EID<17:16>	xxxx
		15:0	EID<15:0>																xxxx	
10A0	C2RXM1	31:16	SID<10:0>													MIDE			EID<17:16>	xxxx
		15:0	EID<15:0>																xxxx	
10B0	C2RXM2	31:16	SID<10:0>													MIDE			EID<17:16>	xxxx
		15:0	EID<15:0>																xxxx	
10B0	C2RXM3	31:16	SID<10:0>													MIDE			EID<17:16>	xxxx
		15:0	EID<15:0>																xxxx	
1010	C2FLTCON0	31:16	FLTEN3	MSEL3<1:0>			FSEL3<4:0>					FLTEN2	MSEL2<1:0>			FSEL2<4:0>				0000
		15:0	FLTEN1	MSEL1<1:0>			FSEL1<4:0>					FLTEN0	MSEL0<1:0>			FSEL0<4:0>				0000
10D0	C2FLTCON1	31:16	FLTEN7	MSEL7<1:0>			FSEL7<4:0>					FLTEN6	MSEL6<1:0>			FSEL6<4:0>				0000
		15:0	FLTEN5	MSEL5<1:0>			FSEL5<4:0>					FLTEN4	MSEL4<1:0>			FSEL4<4:0>				0000
10E0	C2FLTCON2	31:16	FLTEN11	MSEL11<1:0>			FSEL11<4:0>					FLTEN10	MSEL10<1:0>			FSEL10<4:0>				0000
		15:0	FLTEN9	MSEL9<1:0>			FSEL9<4:0>					FLTEN8	MSEL8<1:0>			FSEL8<4:0>				0000
10F0	C2FLTCON3	31:16	FLTEN15	MSEL15<1:0>			FSEL15<4:0>					FLTEN14	MSEL14<1:0>			FSEL14<4:0>				0000
		15:0	FLTEN13	MSEL13<1:0>			FSEL13<4:0>					FLTEN12	MSEL12<1:0>			FSEL12<4:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 29-9: C_iRXMN: CAN ACCEPTANCE FILTER MASK N REGISTER (N = 0, 1, 2 OR 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SID<10:3>							
23:16	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SID<2:0>			—	MIDE	—	EID<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-21 **SID<10:0>**: Standard Identifier bits

- 1 = Include bit, SID_x, in filter comparison
- 0 = Bit SID_x is 'don't care' in filter operation

bit 20 **Unimplemented**: Read as '0'

bit 19 **MIDE**: Identifier Receive Mode bit

- 1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
- 0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented**: Read as '0'

bit 17-0 **EID<17:0>**: Extended Identifier bits

- 1 = Include bit, EID_x, in filter comparison
- 0 = Bit EID_x is 'don't care' in filter operation

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (C_iCON<23:21>) = 100).

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-39: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS ^(2,5,6)			Standard Operating Conditions (see Notes 3,5): 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	62.5	—	1000	ns	—
Throughput Rate							
AD51	FTP	SH0 – SH4 (Class 1 Inputs)	—	—	—	—	SH0-SH4 functionality is not supported. Sampling must be performed on SH5 only. See Notes 3 and 4 .
		SH5 (Class 2 and 3 Inputs)	—	—	500	ksps	Single Class 2 or 3 input, 16 MHz ADC Clock, Source impedance ≤ 200 Ω, SAMC = 3 , Assumes there are no pending sample conversion operations at time of trigger. (See Notes 3 and 4 .)
		Conversion Pipeline	—	—	16	Msp/s	Not applicable
Timing Parameters							
AD60	TSAMP	Sample Time for SH0-SH4 (Class 1 Inputs)	—	—	—	TAD	SH0-SH4 functionality is not supported. Sampling must be performed on SH5 only.
		Sample Time for SH5 (Class 2 and 3 Inputs)	3 6 9 35 68 133 256	—	—	TAD	Source Impedance ≤ 200 Ω, 16 MHz ADC clock Source Impedance ≤ 500 Ω, 16 MHz ADC clock Source Impedance ≤ 1 KΩ, 16 MHz ADC clock Source Impedance ≤ 5 KΩ, 16 MHz ADC clock Source Impedance ≤ 10 KΩ, 16 MHz ADC clock Source Impedance ≤ 20 KΩ, 16 MHz ADC clock Source Impedance ≤ 35 KΩ, 16 MHz ADC clock
AD62	TCONV	Conversion Time (after sample time is complete)	—	—	10	TAD	SH0-SH4 functionality is not supported. Sampling must be performed on SH5 only. For SH5, TSAMP + TCONV provides Trigger to data ready timing;
AD64	TCAL	Calibration Time	—	160	—	TAD	—
AD65	TWAKE	Wake-up time from Low-Power Mode	—	2	—	TAD	—

Note 1: These parameters are not characterized, or tested in manufacturing.

2: The ADC module is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

3: Assuming correct PLL configuration (i.e., 192 MHz system clock).

4: Assuming 4x Oversampling mode.

5: Specifications are based on adherence to the requirements listed in **28.1 “ADC Configuration Requirements”**.

6: All data was collected using a dedicated external precision voltage source connected to VREF+ and with VREF- tied to external AVSS.