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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	98
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecm124-i-tl

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-22: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
JTAG							
TCK	27	38	B21	56	I	ST	JTAG Test Clock Input Pin
TDI	28	39	A26	57	I	ST	JTAG Test Data Input Pin
TDO	24	40	B22	58	O	—	JTAG Test Data Output Pin
TMS	23	17	A11	22	I	ST	JTAG Test Mode Select Pin
Trace							
TRCLK	57	89	A61	129	O	—	Trace Clock
TRD0	58	97	B55	141	O	—	Trace Data bits 0-3
TRD1	61	96	A65	140	O	—	
TRD2	62	95	B54	139	O	—	
TRD3	63	90	B51	130	O	—	
Programming/Debugging							
PGED1	16	25	A18	36	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	15	24	A17	35	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	18	27	A19	38	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	17	26	B14	37	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
MCLR	9	15	A10	20	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81 #)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0718	OFF118 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
071C	OFF119	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0720	OFF120	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0724	OFF121	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0728	OFF122	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
072C	OFF123	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0730	OFF124	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0734	OFF125 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0738	OFF126 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
073C	OFF127 ^(2,4,8)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0740	OFF128	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0744	OFF129	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0748	OFF130	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
074C	OFF131	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000
0750	OFF132	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	—	0000
		15:0	VOFF<15:1>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
 - 2: This bit or register is not available on 64-pin devices.
 - 3: This bit or register is not available on devices without a CAN module.
 - 4: This bit or register is not available on 100-pin devices.
 - 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
 - 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
 - 7: This bit or register is not available on devices without a Crypto module.
 - 8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
0754	OFF133	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0758	OFF134	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
075C	OFF135	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0760	OFF136	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0764	OFF137	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0768	OFF138	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
076C	OFF139	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0770	OFF140	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0774	OFF141	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0778	OFF142	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
077C	OFF143	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0780	OFF144	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0784	OFF145	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0788	OFF146	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
078C	OFF147	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
 - 2: This bit or register is not available on 64-pin devices.
 - 3: This bit or register is not available on devices without a CAN module.
 - 4: This bit or register is not available on 100-pin devices.
 - 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
 - 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
 - 7: This bit or register is not available on devices without a Crypto module.
 - 8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07CC	OFF163	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07D0	OFF164	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07D4	OFF165	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07D8	OFF166	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07DC	OFF167	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07E4	OFF169	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07E8	OFF170	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07EC	OFF171	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07F0	OFF172	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07F4	OFF173	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07F8	OFF174	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
07FC	OFF175	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0800	OFF176 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
0804	OFF177 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
 - 2: This bit or register is not available on 64-pin devices.
 - 3: This bit or register is not available on devices without a CAN module.
 - 4: This bit or register is not available on 100-pin devices.
 - 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
 - 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
 - 7: This bit or register is not available on devices without a Crypto module.
 - 8: This bit or register is not available on 124-pin devices.

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REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0> ⁽¹⁾				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	—	CRCCH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>**: CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (i.e., reverse source byte order)

00 = No swapping (i.e., source byte order)

bit 27 **WBO**: CRC Write Byte Order Selection bit⁽¹⁾

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO**: CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)

0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>**: Polynomial Length bits⁽¹⁾

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN**: CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

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NOTES:

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REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AUTOSET	ISO —	MODE	DMAREQEN	FRCDATTG	DMAREQMD	— DATAWEN	— DATATGGL
23:16	R/W-0, HS	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0	R/W-0, HS	R/W-0	R/W-0, HC
	INCOMPTX NAKTMOUT	CLRDT	SENTSTALL RXSTALL	SENDSTALL SETUPPKT	FLUSH	UNDERRUN ERROR	FIFONE	TXPKTRDY
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					TXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXMAXP<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **AUTOSET:** Auto Set Control bit
1 = TXPKTRDY will be automatically set when data of the maximum packet size (value in TXMAXP) is loaded into the TX FIFO. If a packet of less than the maximum packet size is loaded, then TXPKTRDY will have to be set manually.
0 = TXPKTRDY must be set manually for all packet sizes
- bit 30 **ISO:** Isochronous TX Endpoint Enable bit (Device mode)
1 = Enables the endpoint for Isochronous transfers
0 = Disables the endpoint for Isochronous transfers and enables it for Bulk or Interrupt transfers.
This bit only has an effect in Device mode. In Host mode, it always returns '0'.
- bit 29 **MODE:** Endpoint Direction Control bit
1 = Endpoint is TX
0 = Endpoint is RX
This bit only has any effect where the same endpoint FIFO is used for both TX and RX transactions.
- bit 28 **DMAREQEN:** Endpoint DMA Request Enable bit
1 = DMA requests are enabled for this endpoint
0 = DMA requests are disabled for this endpoint
- bit 27 **FRCDATTG:** Force Endpoint Data Toggle Control bit
1 = Forces the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.
0 = No forced behavior
- bit 26 **DMAREQMD:** Endpoint DMA Request Mode Control bit
1 = DMA Request Mode 1
0 = DMA Request Mode 0
This bit must not be cleared either before or in the same cycle as the above DMAREQEN bit is cleared.
- bit 25 **DATAWEN:** Data Toggle Write Enable bit (Host mode)
1 = Enable the current state of the TX Endpoint data toggle (DATATGGL) to be written
0 = Disables writing the DATATGGL bit
- bit 24 **DATATGGL:** Data Toggle Control bit (Host mode)
When read, this bit indicates the current state of the TX Endpoint data toggle. If DATAWEN = 1, this bit may be written with the required setting of the data toggle. If DATAWEN = 0, any value written to this bit is ignored.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 20-12: SQI1STAT1: SQI STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TXFIFOFREE<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXFIFOCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **TXFIFOFREE<7:0>:** Transmit FIFO Available Word Space bits

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXFIFOCNT<7:0>:** Number of words of read data in the FIFO

22.1 UART Control Registers

TABLE 22-1: UART1 THROUGH UART6 REGISTER MAP

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	U1MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2010	U1STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2040	U1BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	Baud Rate Generator Prescaler																0000
2200	U2MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2210	U2STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2220	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2230	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2240	U2BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	Baud Rate Generator Prescaler																0000
2400	U3MODE ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2410	U3STA ⁽¹⁾	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2420	U3TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2430	U3RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2440	U3BRG ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 23-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2 ⁽¹⁾	CS1 ⁽³⁾	ADDR<13:8>					
	ADDR15 ⁽²⁾	ADDR14 ⁽⁴⁾						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CS2:** Chip Select 2 bit⁽¹⁾

1 = Chip Select 2 is active

0 = Chip Select 2 is inactive

bit 15 **ADDR<15>:** Target Address bit 15⁽²⁾

bit 14 **CS1:** Chip Select 1 bit⁽³⁾

1 = Chip Select 1 is active

0 = Chip Select 1 is inactive

bit 14 **ADDR<14>:** Target Address bit 14⁽⁴⁾

bit 13-0 **ADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.

2: When the CSF<1:0> bits (PMCON<7:6>) = 00.

3: When the CSF<1:0> bits (PMCON<7:6>) = 10.

4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: If the DUALBUF bit (PMCON<17>) = 0, the bits in this register control both read and write target addressing. If the DUALBUF bit = 1, the bits in this register are not used. In this instance, use the PMRADDR register for Read operations and the PMWADDR register for Write operations.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 24-3: EBISMTx: EXTERNAL BUS INTERFACE STATIC MEMORY TIMING REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	PAGEMODE	TPRC<3:0> ⁽¹⁾				TBTA<2:0> ⁽¹⁾		
15:8	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
	TWP<5:0> ⁽¹⁾						TWR<1:0> ⁽¹⁾	
7:0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1
	TAS<1:0> ⁽¹⁾		TRC<5:0> ⁽¹⁾					

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **RDYMODE:** Data Ready Device Select bit

The device associated with register set 'x' is a data-ready device, and will use the EBIRDYx pin.

1 = EBIRDYx input is used

0 = EBIRDYx input is not used

bit 25-24 **PAGESIZE<1:0>:** Page Size for Page Mode Device bits

11 = 32-word page

10 = 16-word page

01 = 8-word page

00 = 4-word page

bit 23 **PAGEMODE:** Memory Device Page Mode Support bit

1 = Device supports Page mode

0 = Device does not support Page mode

bit 22-19 **TPRC<3:0>:** Page Mode Read Cycle Time bits⁽¹⁾

Read cycle time is TPRC + 1 clock cycle.

bit 18-16 **TBTA<2:0>:** Data Bus Turnaround Time bits⁽¹⁾

Clock cycles (0-7) for static memory between read-to-write, write-to-read, and read-to-read when Chip Select changes.

bit 15-10 **TWP<5:0>:** Write Pulse Width bits⁽¹⁾

Write pulse width is TWP + 1 clock cycle.

bit 9-8 **TWR<1:0>:** Write Address/Data Hold Time bits⁽¹⁾

Number of clock cycles to hold address or data on the bus.

bit 7-6 **TAS<1:0>:** Write Address Setup Time bits⁽¹⁾

Clock cycles for address setup time. A value of '0' is only valid in the case of SSRAM.

bit 5-0 **TRC<5:0>:** Read Cycle Time bits⁽¹⁾

Read cycle time is TRC + 1 clock cycle.

Note 1: Please refer to **Section 47. "External Bus Interface (EBI)"** (DS60001245) in the *"PIC32 Family Reference Manual"* for the EBI timing diagrams and additional information.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 25-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

bit 10-9 **RTCCLKSEL<1:0>**: RTCC Clock Select bits

When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

11 = Reserved

10 = Reserved

01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)

00 = RTCC uses the internal 32 kHz oscillator (LPRC)

bit 8-7 **RTCOUTSEL<1:0>**: RTCC Output Data Select bits⁽²⁾

11 = Reserved

10 = RTCC Clock is presented on the RTCC pin

01 = Seconds Clock is presented on the RTCC pin

00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered

bit 6 **RTCCLKON**: RTCC Clock Enable Status bit⁽⁵⁾

1 = RTCC Clock is actively running

0 = RTCC Clock is not running

bit 5-4 **Unimplemented**: Read as '0'

bit 3 **RTCWREN**: Real-Time Clock Value Registers Write Enable bit⁽³⁾

1 = Real-Time Clock Value registers can be written to by the user

0 = Real-Time Clock Value registers are locked out from being written to by the user

bit 2 **RTCSYNC**: Real-Time Clock Value Registers Read Synchronization bit

1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.

0 = Real-time clock value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC**: Half-Second Status bit⁽⁴⁾

1 = Second half period of a second

0 = First half period of a second

bit 0 **RTCOE**: RTCC Output Enable bit

1 = RTCC output is enabled

0 = RTCC output is not enabled

Note 1: The ON bit is only writable when RTCWREN = 1.

2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

3: The RTCWREN bit can be set only when the write sequence is enabled.

4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

5: This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

Note: This register is reset only on a Power-on Reset (POR).

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 25-4: RTCDATE: REAL-TIME CLOCK DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	MONTH10	MONTH01<3:0>			
15:8	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	DAY10<1:0>		DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	—	—	—	—	—	WDAY01<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **YEAR10<3:0>**: Binary-Coded Decimal Value of Years bits, tens digit

bit 27-24 **YEAR01<3:0>**: Binary-Coded Decimal Value of Years bits, ones digit

bit 23-21 **Unimplemented**: Read as '0'

bit 20 **MONTH10**: Binary-Coded Decimal Value of Months bit, tens digit; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>**: Binary-Coded Decimal Value of Months bits, ones digit; contains a value from 0 to 9

bit 15-14 **Unimplemented**: Read as '0'

bit 13-12 **DAY10<1:0>**: Binary-Coded Decimal Value of Days bits, tens digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>**: Binary-Coded Decimal Value of Days bits, ones digit; contains a value from 0 to 9

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **WDAY01<2:0>**: Binary-Coded Decimal Value of Weekdays bits, ones digit; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 25-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	MONTH10	MONTH01<3:0>			
15:8	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	DAY10<1:0>		DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	—	—	—	—	—	WDAY01<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MONTH10:** Binary Coded Decimal value of months bit, tens digit; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, ones digit; contains a value from 0 to 9

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAY10<1:0>:** Binary Coded Decimal value of days bits, tens digit; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, ones digit; contains a value from 0 to 9

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY01<2:0>:** Binary Coded Decimal value of weekdays bits, ones digit; contains a value from 0 to 6

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B0B8	AD1DATA0	31:16	ADC Output Register 0 <31:16>																0000
		15:0	ADC Output Register 0 <15:0>																0000
B0BC	AD1DATA1	31:16	ADC Output Register 1 <31:16>																0000
		15:0	ADC Output Register 1 <15:0>																0000
B0C0	AD1DATA2	31:16	ADC Output Register 2 <31:16>																0000
		15:0	ADC Output Register 2 <15:0>																0000
B0C4	AD1DATA3	31:16	ADC Output Register 3 <31:16>																0000
		15:0	ADC Output Register 3 <15:0>																0000
B0C8	AD1DATA4	31:16	ADC Output Register 4 <31:16>																0000
		15:0	ADC Output Register 4 <15:0>																0000
B0CC	AD1DATA5	31:16	ADC Output Register 5 <31:16>																0000
		15:0	ADC Output Register <15:0>																0000
B0D0	AD1DATA6	31:16	ADC Output Register 6 <31:16>																0000
		15:0	ADC Output Register 6 <15:0>																0000
B0D4	AD1DATA7	31:16	ADC Output Register 7 <31:16>																0000
		15:0	ADC Output Register 7 <15:0>																0000
B0D8	AD1DATA8	31:16	ADC Output Register 8 <31:16>																0000
		15:0	ADC Output Register 8 <15:0>																0000
B0DC	AD1DATA9	31:16	ADC Output Register 9 <31:16>																0000
		15:0	ADC Output Register 9 <15:0>																0000
B0E0	AD1DATA10	31:16	ADC Output Register 10 <31:16>																0000
		15:0	ADC Output Register 10 <15:0>																0000
B0E4	AD1DATA11	31:16	ADC Output Register 11 <31:16>																0000
		15:0	ADC Output Register 11 <15:0>																0000
B0E8	AD1DATA12	31:16	ADC Output Register 12 <31:16>																0000
		15:0	ADC Output Register 12 <15:0>																0000
B0EC	AD1DATA13	31:16	ADC Output Register 13 <31:16>																0000
		15:0	ADC Output Register 13 <15:0>																0000
B0F0	AD1DATA14	31:16	ADC Output Register 14 <31:16>																0000
		15:0	ADC Output Register 14 <15:0>																0000
B0F4	AD1DATA15	31:16	ADC Output Register 15 <31:16>																0000
		15:0	ADC Output Register 15 <15:0>																0000
B0F8	AD1DATA16	31:16	ADC Output Register 16 <31:16>																0000
		15:0	ADC Output Register 16 <15:0>																0000
B0FC	AD1DATA17	31:16	ADC Output Register 17 <31:16>																0000
		15:0	ADC Output Register 17<15:0>																0000
B100	AD1DATA18	31:16	ADC Output Register 18 <31:16>																0000
		15:0	ADC Output Register18 <15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 28-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)

bit 6-0 **ADCDIV<6:0>**: ADC Input Clock Divider bits⁽²⁾

These bits divide the selected clock source to derive the desired ADC clock rate (T_{AD}).

11111111 = $2 T_Q * (ADCDIV<6:0>) = 254 * T_Q = T_{AD}$

.

.

.

0000011 = $2 T_Q * (ADCDIV<6:0>) = 6 * T_Q = T_{AD}$

0000010 = $2 T_Q * (ADCDIV<6:0>) = 4 * T_Q = T_{AD}$

0000001 = $2 T_Q * (ADCDIV<6:0>) = 2 * T_Q = T_{AD}$

0000000 = $T_Q = T_{AD}$

Note 1: This bit is set to '0' when ADCEN (AD1CON1<15>) = 0.

2: These bits should be configured prior to enabling the ADC by setting the ADCEN bit (AD1CON1<15>) = 1.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 28-5: AD1GIRQEN1: ADC1 GLOBAL INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN31	AGIEN30	AGIEN29	AGIEN28	AGIEN27	AGIEN26	AGIEN25	AGIEN24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN23	AGIEN22	AGIEN21	AGIEN20	AGIEN19	AGIEN18	AGIEN17	AGIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **AGIENx:** Global ADC Interrupt Enable bits ('x' = 0-31)

1 = A data ready event (transition from 0 to 1 of the ARDYx bit) will generate a Global ADC interrupt
0 = No global interrupt is generated on a data ready event

The Global ADC Interrupt is enabled by setting a bit in the IECx registers (refer to **Section 7.0 “CPU Exceptions and Interrupt Controller”** for details).

- Note 1:** The enable bits do not affect assertion of the individual interrupt output. Interrupts generated for individual ARDY events are enabled in the IECx register.
- 2:** AGIENx = ANx, where 'x' = 0-31.

31.1 Comparator Control Registers

TABLE 31-1: COMPARATOR REGISTER MAP

Virtual Address (BF84_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>	—	—	CREF	—	—	CCH<1:0>	—	00C3
C010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>	—	—	CREF	—	—	CCH<1:0>	—	00C3
C060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-36: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode (Note 1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode (Note 1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 1)	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode (Note 1)	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode (Note 1)	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode (Note 1)	600	—	ns	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode (Note 1)	250	—	ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode (Note 1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode (Note 1)	0.5	—	μs	
IS50	Cb	Bus Capacitive Loading		—	—	pF	See parameter DO58

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

PIC32MZ Embedded Connectivity (EC) Family

TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ Feature
PLL Configuration	
The FNOSC<2:0> and NOSC<2:0> bits select between POSC and FRC. FNOSC<2:0> (DEVCFG1<2:0>) NOSC<2:0> (OSCCON<10:8>)	Selection of which input clock (POSC or FRC) is now done through the FPLLICK/PLLICK bits. FPLLICK (DEVCFG2<7>) PLLICK (SPLLCON<7>)
On PIC32MX devices, the input frequency to the PLL had to be between 4 MHz and 5 MHz. FPLLIDIV selected how to divide the input frequency to give it the appropriate range. FPLLIDIV<2:0> (DEVCFG2<2:0>) 111 = 12x divider 110 = 10x divider 101 = 6x divider 100 = 5x divider 011 = 4x divider 010 = 3x divider 001 = 2x divider 000 = 1x divider	On PIC32MZ devices, the input range for the PLL is wider (5 MHz to 64 MHz). The input divider values have changed, and new FPLLRRNG/PLLRRNG bits have been added to indicate under what range the input frequency falls. FPLLIDIV<2:0> (DEVCFG2<2:0>) PLLIDIV<2:0> (SPLLCON<2:0>) 111 = Divide by 8 110 = Divide by 7 101 = Divide by 6 100 = Divide by 5 011 = Divide by 4 010 = Divide by 3 001 = Divide by 2 000 = Divide by 1 FPLLRRNG<2:0> (DEVCFG2<6:4>) PLLRRNG<2:0> (SPLLCON<2:0>) 111 = Reserved 110 = Reserved 101 = 34-64 MHz 100 = 21-42 MHz 011 = 13-26 MHz 010 = 8-16 MHz 001 = 5-10 MHz 000 = Bypass
On PIC32MX devices, the output frequency of PLL is between 60 MHz and 120 MHz. The PLL multiplier and divider bits configure the PLL for this range. FPLLMUL<2:0> (DEVCFG2<6:4>) PLLMULT<2:0> (OSCCON<18:16>) 111 = 24x multiplier 110 = 21x multiplier 101 = 20x multiplier 100 = 19x multiplier 011 = 18x multiplier 010 = 17x multiplier 001 = 16x multiplier 000 = 15x multiplier FPLLODIV<2:0> (DEVCFG2<18:16>) PLLODIV<2:0> (OSCCON<29:27>) 111 = 24x multiplier 110 = 21x multiplier 101 = 20x multiplier 100 = 19x multiplier 011 = 18x multiplier 010 = 17x multiplier 001 = 16x multiplier 000 = 15x multiplier	The PLL multiplier and divider on PIC32MZ devices have a wider range to accommodate the wider PLL specification range of 10 MHz to 200 MHz. FPLLMULT<6:0> (DEVCFG2<14:8>) PLLMULT<6:0> (SPLLCON<22:16>) 1111111 = Multiply by 128 1111110 = Multiply by 127 1111101 = Multiply by 126 1111100 = Multiply by 125 • • • 0000000 = Multiply by 1 FPLLODIV<2:0> (DEVCFG2<18:16>) PLLODIV<2:0> (SPLLCON<26:24>) 111 = PLL Divide by 32 110 = PLL Divide by 32 101 = PLL Divide by 32 100 = PLL Divide by 16 011 = PLL Divide by 8 010 = PLL Divide by 4 001 = PLL Divide by 2 000 = PLL Divide by 2