# Microchip Technology - PIC32MZ2048ECM144-I/PH Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

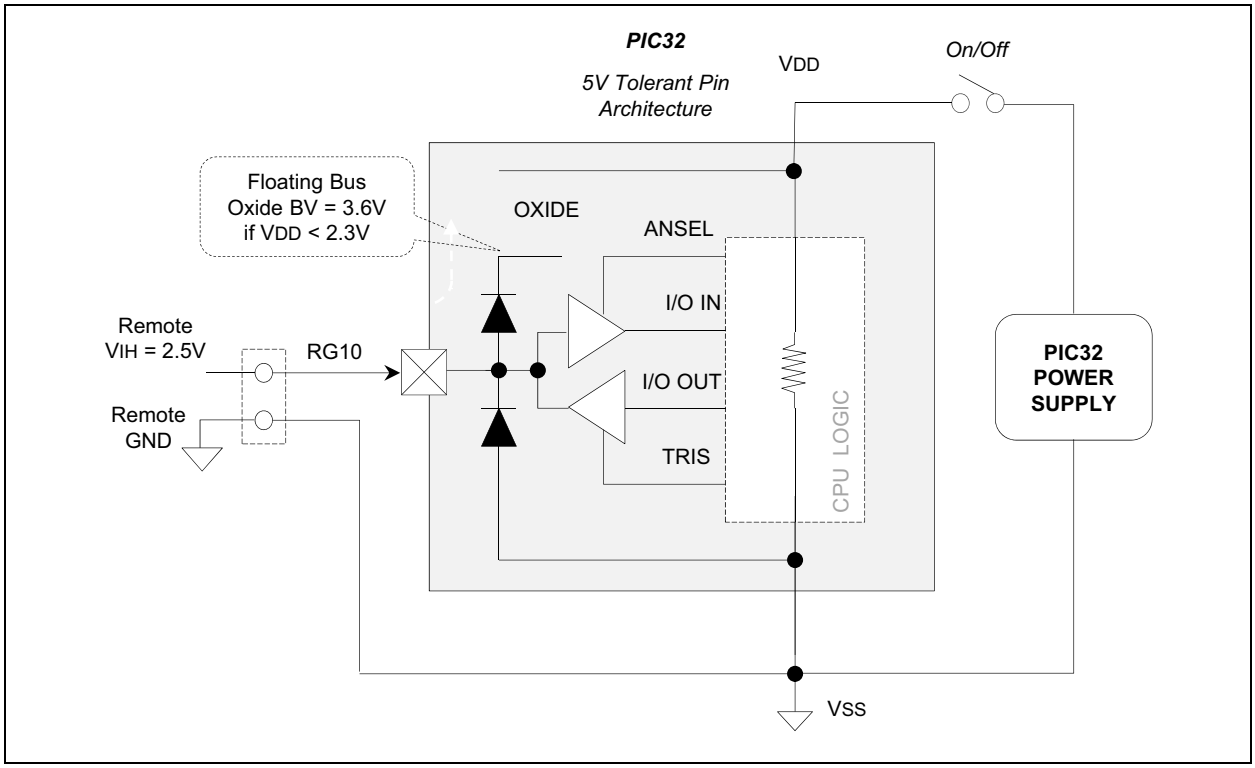
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® microAptiv™ |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, SPI, SQI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 48x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-TQFP |
| Supplier Device Package | 144-TQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecm144-i-ph |

### 2.10.2 5V TOLERANT INPUT PINS

The internal high side diode on 5V tolerant pins are bussed to an internal floating node, rather than being connected to VDD, as shown in Figure 2-7. Voltages on these pins, if VDD < 2.3V, should not exceed roughly 3.2V relative to VSS of the PIC32 device. Voltage of 3.6V or higher will violate the absolute maximum specification, and will stress the oxide layer separating the high side floating node, which impacts device reliability. If a remotely powered "digital-only" signal can be guaranteed to always be ≤ 3.2V relative to Vss on the PIC32 device side, a 5V tolerant pin could be used without the need for a digital isolator. This is assuming there is not a ground loop issue, logic ground of the two circuits not at the same absolute level, and a remote logic low input is not less than VSS - 0.3V.

**FIGURE 2-7: PIC32 5V TOLERANT PIN ARCHITECTURE EXAMPLE**



## 4.2 System Bus Arbitration

**Note:** The System Bus interconnect implements one or more instantiations of the SonicsSX® interconnect from Sonics, Inc. This document contains materials that are (c) 2003-2015 Sonics, Inc., and that constitute proprietary information of Sonics, Inc. SonicsSX is a registered trademark of Sonics, Inc. All such materials and trademarks are used under license from Sonics, Inc.

As shown in the PIC32MZ EC Family Block Diagram (see Figure 1-1), there are multiple initiator modules (I1 through I14) in the system that can access various target modules (T1 through T13). Table 4-4 illustrates which initiator can access which target. The System Bus supports simultaneous access to targets by initiators, so long as the initiators are accessing different targets. The System Bus will perform arbitration, if multiple initiators attempt to access the same target.

**REGISTER 5-6: NVMPWP: PROGRAM FLASH WRITE-PROTECT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-1 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | PWPULOCK | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PWP<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | PWP<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | PWP<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **PWPULOCK:** Program Flash Memory Page Write-protect Unlock bit
1 = Register is not locked and can be modified
0 = Register is locked and cannot be modified
This bit is only clearable and cannot be set except by any reset.

bit 30-24 **Unimplemented:** Read as '0'

bit 23-0 **PWP<23:0>:** Flash Program Write-protect (Page) Address bits
Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>. When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

**Note:** The bits in this register are only writable when the NVMKEY unlock sequence is followed.

**TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)**

| Virtual Address (BF81_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0660 | OFF072 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0664 | OFF073 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0668 | OFF074 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 066C | OFF075 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0670 | OFF076 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0674 | OFF077(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0678 | OFF078(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 067C | OFF079(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0680 | OFF080(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0684 | OFF081(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0688 | OFF082(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 068C | OFF083(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0690 | OFF084(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0694 | OFF085(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |
| 0698 | OFF086(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | VOFF<17:16> | | 0000 |
| | | 15:0 | VOFF<15:1> | | | | | | | | | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
**2:** This bit or register is not available on 64-pin devices.
**3:** This bit or register is not available on devices without a CAN module.
**4:** This bit or register is not available on 100-pin devices.
**5:** Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
**6:** Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
**7:** This bit or register is not available on devices without a Crypto module.
**8:** This bit or register is not available on 124-pin devices.

## 8.0 OSCILLATOR CONFIGURATION

**Note:** This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MZ EC oscillator system has the following modules and features:

- A total of five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown with dedicated Back-up FRC (BFRC)
- Dedicated On-Chip PLL for USB peripheral
- Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility

A block diagram of the oscillator system is provided in Figure 8-1. Table 8-1 shows the clock distribution.

**TABLE 11-1: USB REGISTER MAP (CONTINUED)**

| Virtual Address | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3340 | USB DPBFD | 31:16 | — | — | — | — | — | — | — | — | EP7TXD | EP6TXD | EP5TXD | EP4TXD | EP3TXD | EP2TXD | EP1TXD | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | EP7RXD | EP6RXD | EP5RXD | EP4RXD | EP3RXD | EP2RXD | EP1RXD | — | 0000 |
| 3344 | USB TMCON1 | 31:16 | THHSRTN<15:0> | | | | | | | | | | | | | | | | 05E6 |
| | | 15:0 | TUCH<15:0> | | | | | | | | | | | | | | | | 4074 |
| 3348 | USB TMCON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | THSBT<3:0> | | | | 0000 |
| 3360 | USB LPMR1 | 31:16 | — | — | LPM ERRIE | LPM RESIE | LPMACKIE | LPMNYIE | LPMSTIE | LPMTOIE | — | — | — | LPMNAK(1) | LPMEN<1:0> | | LPMRES | LPMXMT | 0000 |
| | | | | | | | | | | | | | | —(2) | —(2) | —(2) | | | 0000 |
| | | 15:0 | ENDPOINT<3:0> | | | | — | — | — | RMTWAK | HIRD<3:0> | | | | LNKSTATE<3:0> | | | | 0000 |
| 3364 | USB LMPR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | LPMFADDR<6:0> | | | | | | | — | — | LPMERR(1) | LPMRES | LPMNC | LPMACK | LPMNY | LPMST | 0000 |
| | | | | | | | | | | | | | —(2) | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Device mode.
**2:** Host mode.
**3:** Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
**4:** Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

**REGISTER 11-10: USBIENCSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 1-7)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXINTERV<7:0> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SPEED<1:0> | | PROTOCOL<1:0> | | TEP<3:0> | | | |
| 15:8 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | RXCNT<13:8> | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RXCNT<7:0> | | | | | | | |

| **Legend:** | HC = Hardware Clearable | HS = Hardware Settable | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **TXINTERV<7:0>:** Endpoint TX Polling Interval/NAK Limit bits (*Host mode*)

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and interpretation for these bits:

| Transfer Type | Speed | Valid Values (m) | Interpretation |
|---|---|---|---|
| Interrupt | Low/Full | 0x01 to 0xFF | Polling interval is 'm' frames. |
| | High | 0x01 to 0x10 | Polling interval is $2^{(m-1)}$ frames. |
| Isochronous | Full or High | 0x01 to 0x10 | Polling interval is $2^{(m-1)}$ frames/microframes. |
| Bulk | Full or High | 0x02 to 0x10 | NAK limit is $2^{(m-1)}$ frames/microframes. A value of '0' or '1' disables the NAK time-out function. |

bit 23-22 **SPEED<1:0>:** TX Endpoint Operating Speed Control bits (*Host mode*)
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-20 **PROTOCOL<1:0>:** TX Endpoint Protocol Control bits
11 = Interrupt
10 = Bulk
01 = Isochronous
00 = Control

bit 19-16 **TEP<3:0>:** TX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **RXCNT<13:0>:** Receive Count bits

The number of received data bytes in the endpoint RX FIFO. The value returned changes as the contents of the FIFO change and is only valid while RXPKTRDY is set.

**TABLE 12-1: INPUT PIN SELECTION**

| Peripheral Pin | [*pin name*]R SFR | [*pin name*]R bits | [*pin name*]R Value to RPn Pin Selection |
|---|---|---|---|
| INT3 | INT3R | INT3R<3:0> | 0000 = RPD2<br>0001 = RPG8<br>0010 = RPF4<br>0011 = RPD10<br>0100 = RPF1<br>0101 = RPB9<br>0110 = RPB10<br>0111 = RPC14<br>1000 = RPB5<br>1001 = Reserved<br>1010 = RPC1(1)<br>1011 = RPD14(1)<br>1100 = RPG1(1)<br>1101 = RPA14(1)<br>1110 = RPD6(2)<br>1111 = Reserved |
| T2CK | T2CKR | T2CKR<3:0> | |
| T6CK | T6CKR | T6CKR<3:0> | |
| IC3 | IC3R | IC3R<3:0> | |
| IC7 | IC7R | IC7R<3:0> | |
| U1RX | U1RXR | U1RXR<3:0> | |
| $\overline{\text{U2CTS}}$ | U2CTSR | U2CTSR<3:0> | |
| U5RX | U5RXR | U5RXR<3:0> | |
| $\overline{\text{U6CTS}}$ | U6CTSR | U6CTSR<3:0> | |
| SDI1 | SDI1R | SDI1R<3:0> | |
| SDI3 | SDI3R | SDI3R<3:0> | |
| SDI5(1) | SDI5R(1) | SDI5R<3:0>(1) | |
| $\overline{\text{SS6}}$(1) | SS6R(1) | SS6R<3:0>(1) | |
| REFCLKI1 | REFCLKI1R | REFCLKI1R<3:0> | |
| INT4 | INT4R | INT4R<3:0> | 0000 = RPD3<br>0001 = RPG7<br>0010 = RPF5<br>0011 = RPD11<br>0100 = RPF0<br>0101 = RPB1<br>0110 = RPE5<br>0111 = RPC13<br>1000 = RPB3<br>1001 = Reserved<br>1010 = RPC4(1)<br>1011 = RPD15(1)<br>1100 = RPG0(1)<br>1101 = RPA15(1)<br>1110 = RPD7(2)<br>1111 = Reserved |
| T5CK | T5CKR | T5CKR<3:0> | |
| T7CK | T7CKR | T7CKR<3:0> | |
| IC4 | IC4R | IC4R<3:0> | |
| IC8 | IC8R | IC8R<3:0> | |
| U3RX | U3RXR | U3RXR<3:0> | |
| $\overline{\text{U4CTS}}$ | U4CTSR | U4CTSR<3:0> | |
| SDI2 | SDI2R | SDI2R<3:0> | |
| SDI4 | SDI4R | SDI4R<3:0> | |
| C1RX(3) | C1RXR(3) | C1RXR<3:0>(3) | |
| REFCLKI4 | REFCLKI4R | REFCLKI4R<3:0> | |
| INT2 | INT2R | INT2R<3:0> | 0000 = RPD9<br>0001 = RPG6<br>0010 = RPB8<br>0011 = RPB15<br>0100 = RPD4<br>0101 = RPB0<br>0110 = RPE3<br>0111 = RPB7<br>1000 = Reserved<br>1001 = RPF12(1)<br>1010 = RPD12(1)<br>1011 = RPF8(1)<br>1100 = RPC3(1)<br>1101 = RPE9(1)<br>1110 = Reserved<br>1111 = Reserved |
| T3CK | T3CKR | T3CKR<3:0> | |
| T8CK | T8CKR | T8CKR<3:0> | |
| IC2 | IC2R | IC2R<3:0> | |
| IC5 | IC5R | IC5R<3:0> | |
| IC9 | IC9R | IC9R<3:0> | |
| $\overline{\text{U1CTS}}$ | U1CTSR | U1CTSR<3:0> | |
| U2RX | U2RXR | U2RXR<3:0> | |
| $\overline{\text{U5CTS}}$ | U5CTSR | U5CTSR<3:0> | |
| $\overline{\text{SS1}}$ | SS1R | SS1R<3:0> | |
| $\overline{\text{SS3}}$ | SS3R | SS3R<3:0> | |
| $\overline{\text{SS4}}$ | SS4R | SS4R<3:0> | |
| $\overline{\text{SS5}}$(1) | SS5R(1) | SS5R<3:0>(1) | |
| C2RX(3) | C2RXR(3) | C2RXR<3:0>(3) | |

**Note 1:** This selection is not available on 64-pin devices.

**2:** This selection is not available on 64-pin or 100-pin devices.

**3:** This selection is not available on devices without a CAN module.

**NOTES:**

**REGISTER 25-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | CAL<9:8> | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CAL<7:0> | | | | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | RTCCLKSEL<1:0> | | RTC OUTSEL<1>(2) |
| 7:0 | R/W-0 | R-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R/W-0 |
| | RTC OUTSEL<0>(2) | RTC CLKON(5) | — | — | RTC WREN(3) | RTC SYNC | HALFSEC(4) | RTCOE |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** Real-Time Clock Drift Calibration bits, which contain a signed 10-bit integer value
0111111111 = Maximum positive adjustment, adds 511 real-time clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 real-time clock pulse every one minute
0000000000 = No adjustment
1111111111 = Minimum negative adjustment, subtracts 1 real-time clock pulse every one minute
•
•
•
1000000000 = Maximum negative adjustment, subtracts 512 real-time clock pulses every one minute

bit 15 **ON:** RTCC On bit(1)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Disables RTCC operation when CPU enters Idle mode
0 = Continue normal operation when CPU enters Idle mode

bit 12-11 **Unimplemented:** Read as '0'

**Note 1:** The ON bit is only writable when RTCWREN = 1.
**2:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
**3:** The RTCWREN bit can be set only when the write sequence is enabled.
**4:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).
**5:** This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

**Note:** This register is reset only on a Power-on Reset (POR).

Figure 26-10 shows the Security Association control word structure.

The Crypto Engine fetches different structures for different flows and ensures that hardware fetches minimum words from SA required for processing. The structure is ready for hardware optimal data fetches.

**FIGURE 26-10: FORMAT OF SA_CTRL**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31-24 | — | — | VERIFY | — | NO_RX | OR_EN | ICVONLY | IRFLAG |
| 23-16 | LNC | LOADIV | FB | FLAGS | — | — | — | ALGO<6> |
| 15-8 | ALGO<5:0> | | | | | | ENC | KEY SIZE<1> |
| 7-0 | KEY SIZE<0> | MULTITASK<2:0> | | | CRYPTOALGO<3:0> | | | |

bit 31-30 **Reserved:** Do not use

bit 29 **VERIFY:** NIST Procedure Verification Setting
1 = NIST procedures are to be used
0 = Do not use NIST procedures

bit 28 **Reserved:** Do not use

bit 27 **NO_RX:** Receive DMA Control Setting
1 = Only calculate ICV for authentication calculations
0 = Normal processing

bit 26 **OR_EN:** OR Register Bits Enable Setting
1 = OR the register bits with the internal value of the CSR register
0 = Normal processing

bit 25 **ICVONLY:** Incomplete Check Value Only Flag
This affects the SHA-1 algorithm only. It has no effect on the AES algorithm.
1 = Only three words of the HMAC result are available
0 = All results from the HMAC result are available

bit 24 **IRFLAG:** Immediate Result of Hash Setting
This bit is set when the immediate result for hashing is requested.
1 = Save the immediate result for hashing
0 = Do not save the immediate result

bit 23 **LNC:** Load New Keys Setting
1 = Load a new set of keys for encryption and authentication
0 = Do not load new keys

bit 22 **LOADIV:** Load IV Setting
1 = Load the IV from this Security Association
0 = Use the next IV

bit 21 **FB:** First Block Setting
This bit indicates that this is the first block of data to feed the IV value.
1 = Indicates this is the first block of data
0 = Indicates this is not the first block of data

bit 20 **FLAGS:** Incoming/Outgoing Flow Setting
1 = Security Association is associated with an outgoing flow
0 = Security Association is associated with an incoming flow

bit 19-17 **Reserved:** Do not use

**REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BUFCNT<7:0>(1) | | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ETHBUSY(4,5) | TXBUSY(2,6) | RXBUSY(3,6) | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits(1)

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

**Note:** BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ETHBUSY:** Ethernet Module busy bit(4,5)

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction
0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

**Note 1:** This bit is only used for RX operations.
**2:** This bit is only affected by TX operations.
**3:** This bit is only affected by RX operations.
**4:** This bit is affected by TX and RX operations.
**5:** This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
**6:** This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

**REGISTER 30-36: EMAC1MIND: ETHERNET CONTROLLER MAC MII MANAGEMENT INDICATORS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | LINKFAIL | NOTVALID | SCAN | MIIMBUSY |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **LINKFAIL:** Link Fail bit

When '1' is returned - indicates link fail has occurred. This bit reflects the value last read from the PHY status register.

bit 2 **NOTVALID:** MII Management Read Data Not Valid bit

When '1' is returned - indicates an MII management read cycle has not completed and the Read Data is not yet valid.

bit 1 **SCAN:** MII Management Scanning bit

When '1' is returned - indicates a scan operation (continuous MII Management Read cycles) is in progress.

bit 0 **MIIMBUSY:** MII Management Busy bit

When '1' is returned - indicates MII Management module is currently performing an MII Management Read or Write cycle.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

## 32.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

**Note:** This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

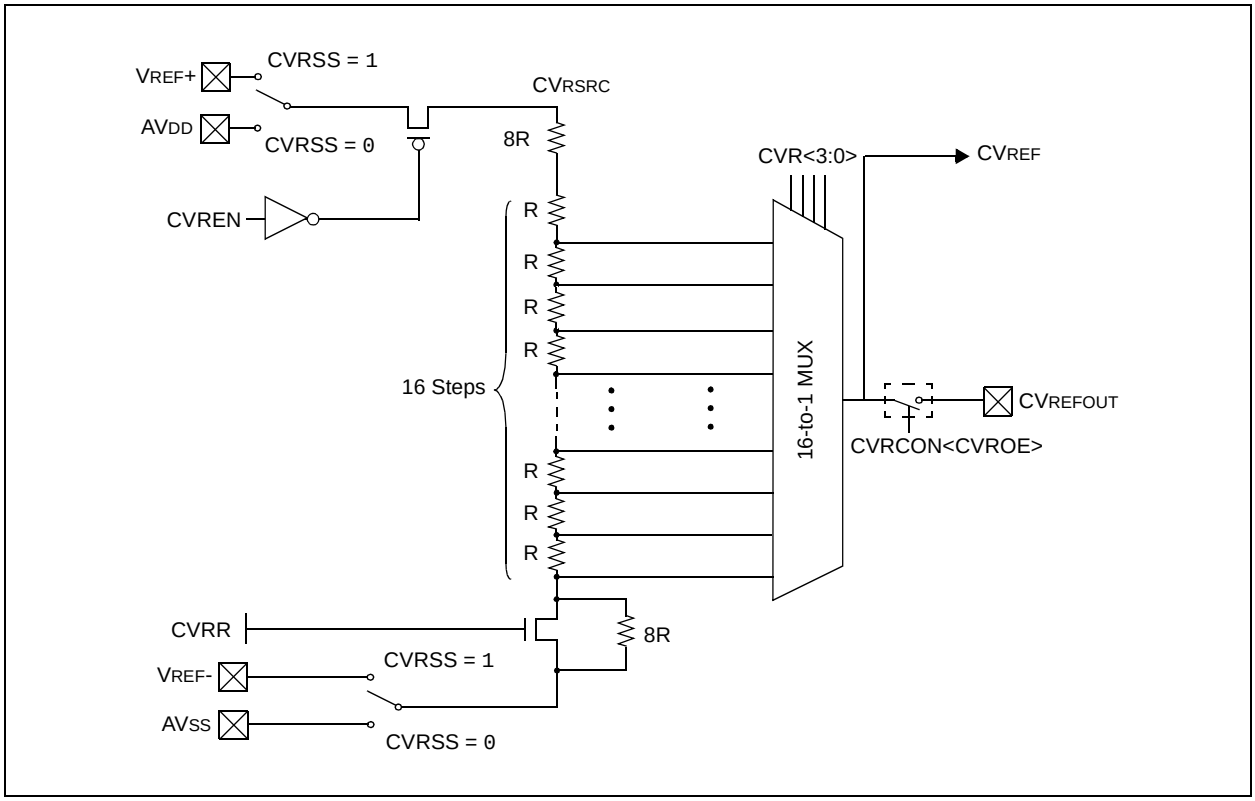
The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

A block diagram of the CVREF module is illustrated in Figure 32-1.

**FIGURE 32-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**



**NOTES:**

**REGISTER 34-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)**

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitoring Selection Configuration bits

11 = Clock switching is enabled and clock monitoring is enabled
10 = Clock switching is disabled and clock monitoring is enabled
01 = Clock switching is enabled and clock monitoring is disabled
00 = Clock switching is disabled and clock monitoring is disabled

bit 13-11 **Reserved:** Write as '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit

1 = CLKO output disabled
0 = CLKO output signal active on the OSC2 pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits

11 = POSC disabled
10 = HS Oscillator mode selected
01 = Reserved
00 = EC mode selected

bit 7 **IESO:** Internal External Switchover bit

1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **FSOSCEN:** Secondary Oscillator Enable bit

1 = Enable SOSC
0 = Disable SOSC

bit 5-3 **DMTINV<2:0>:** Deadman Timer Count Window Interval bits

111 = Window/Interval value is 127/128 counter value
110 = Window/Interval value is 63/64 counter value
101 = Window/Interval value is 31/32 counter value
100 = Window/Interval value is 15/16 counter value
011 = Window/Interval value is 7/8 counter value
010 = Window/Interval value is 3/4 counter value
001 = Window/Interval value is 1/2 counter value
000 = Window/Interval value is zero

**REGISTER 34-11: DEVID: DEVICE AND REVISION ID REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | VER<3:0>(1) | | | | DEVID<27:24>(1) | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | DEVID<23:16>(1) | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | DEVID<15:8>(1) | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | DEVID<7:0>(1) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID(1)

**Note 1:** See the *"PIC32 Flash Programming Specification"* (DS60001145) for a list of Revision and Device ID values.

**REGISTER 34-12: DEVADCx: DEVICE ADC CALIBRATION REGISTER 'x' ('x' = 1-5)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | ADCAL<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | ADCAL<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | ADCAL<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | ADCAL<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **ADCAL<31:0>:** Calibration Data for the ADC Module bits

This data must be copied to the corresponding AD1CALx register. Refer to **Section 28.0 "Pipelined Analog-to-Digital Converter (ADC)"** for more information.

**FIGURE 37-22: PARALLEL MASTER PORT READ TIMING DIAGRAM**

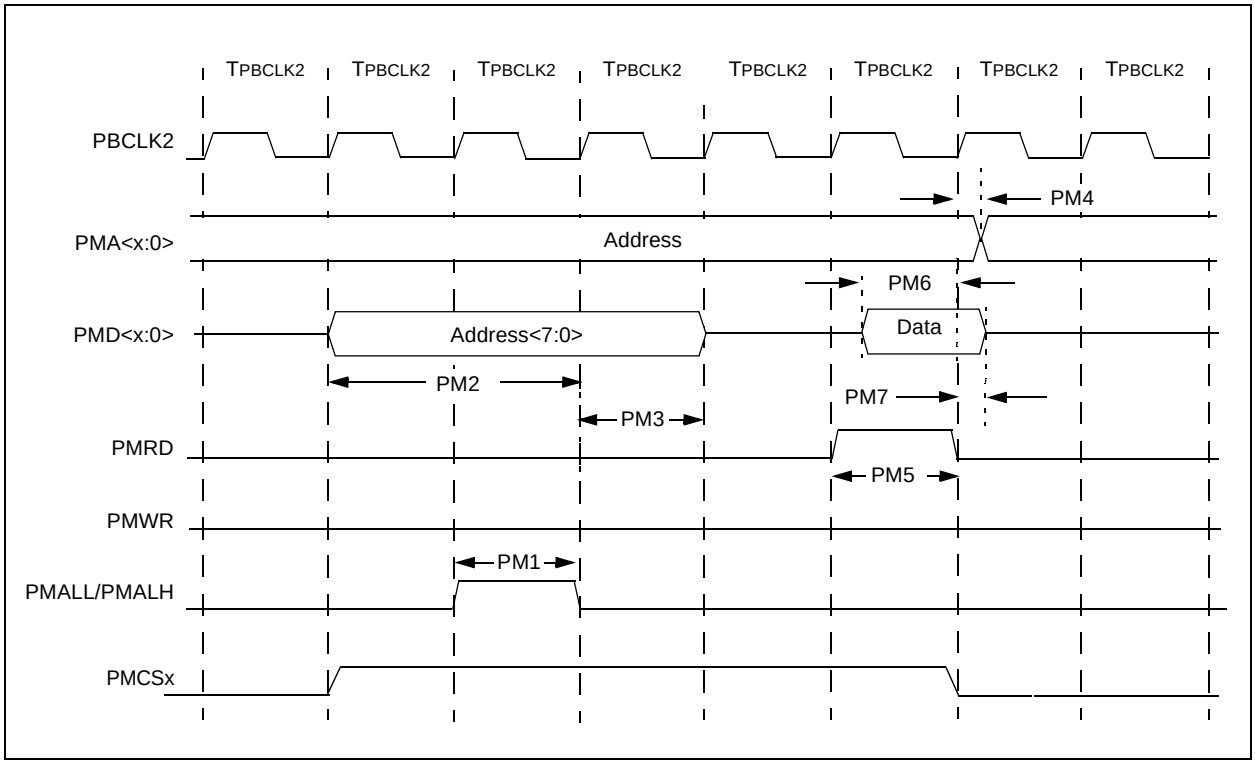



**TABLE 37-42: PARALLEL MASTER PORT READ TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PM1 | TLAT | PMALL/PMALH Pulse Width | — | 1 TPBCLK2 | — | — | — |
| PM2 | TADSU | Address Out Valid to PMALL/ PMALH Invalid (address setup time) | — | 2 TPBCLK2 | — | — | — |
| PM3 | TADHOLD | PMALL/PMALH Invalid to Address Out Invalid (address hold time) | — | 1 TPBCLK2 | — | — | — |
| PM4 | TAHOLD | PMRD Inactive to Address Out Invalid (address hold time) | 5 | — | — | ns | — |
| PM5 | TRD | PMRD Pulse Width | — | 1 TPBCLK2 | — | — | — |
| PM6 | TDSU | PMRD or PMENB Active to Data In Valid (data setup time) | 15 | — | — | ns | — |
| PM7 | TDHOLD | PMRD or PMENB Inactive to Data In Invalid (data hold time) | 5 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**TABLE 37-45: ETHERNET MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **MIIM Timing Requirements** | | | | | | |
| ET1 | MDC Duty Cycle | 40 | — | 60 | % | — |
| ET2 | MDC Period | 400 | — | — | ns | — |
| ET3 | MDIO Output Setup and Hold | 10 | — | 10 | ns | See Figure 37-24 |
| ET4 | MDIO Input Setup and Hold | 0 | — | 300 | ns | See Figure 37-25 |
| **MII Timing Requirements** | | | | | | |
| ET5 | TX Clock Frequency | — | 25 | — | MHz | — |
| ET6 | TX Clock Duty Cycle | 35 | — | 65 | % | — |
| ET7 | ETXDx, ETEN, ETXERR Output Delay | 0 | — | 25 | ns | See Figure 37-26 |
| ET8 | RX Clock Frequency | — | 25 | — | MHz | — |
| ET9 | RX Clock Duty Cycle | 35 | — | 65 | % | — |
| ET10 | ERXDx, ERXDV, ERXERR Setup and Hold | 10 | — | 30 | ns | See Figure 37-27 |
| **RMII Timing Requirements** | | | | | | |
| ET11 | Reference Clock Frequency | — | 50 | — | MHz | — |
| ET12 | Reference Clock Duty Cycle | 35 | — | 65 | % | — |
| ET13 | ETXDx, ETEN, Setup and Hold | 2 | — | 16 | ns | — |
| ET14 | ERXDx, ERXDV, ERXERR Setup and Hold | 2 | — | 16 | ns | — |

**FIGURE 37-24: MDIO SOURCED BY THE PIC32 DEVICE**

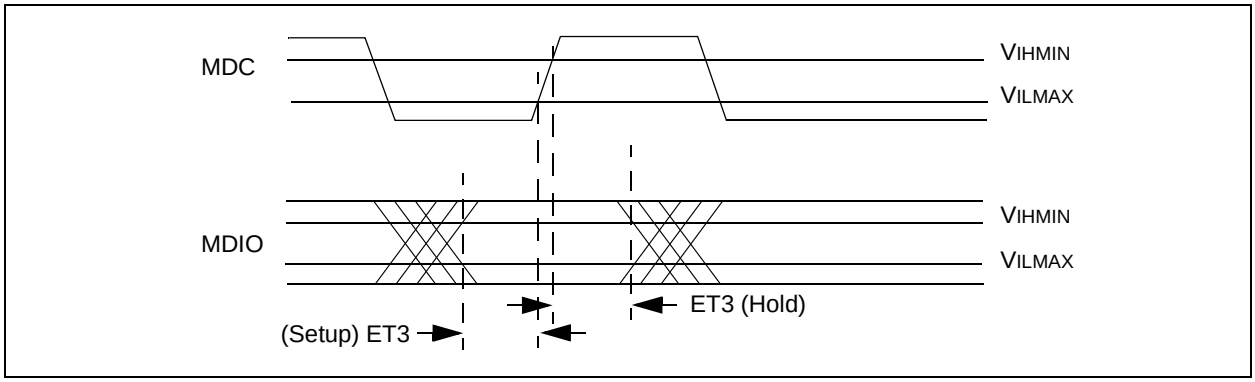



**FIGURE 37-25: MDIO SOURCED BY THE PHY**

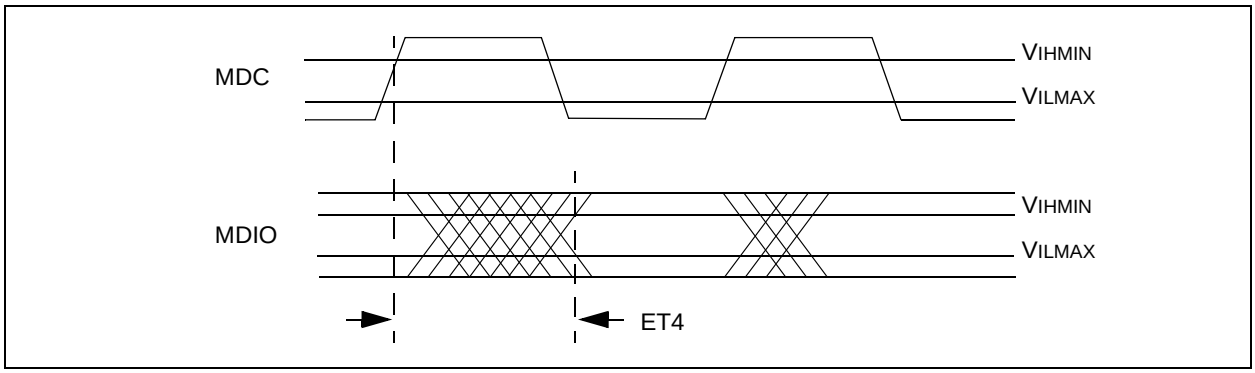


**TABLE B-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **28.0 "12-bit Pipelined Analog-to-Digital Converter (ADC)"** | Figure 28-1, Figure 28-2, and Figure 28-3 were updated.<br>Register names were updated in the ADC Register Map (see Table 28-1).<br>The OVRSAM<2:0> bit values were updated (see Register 28-14). |
| **34.0 "Special Features"** | The DEVCFG3/ADEVCFG3 register was updated (see Register 34-6). |
| **37.0 "Electrical Characteristics"** | Various electrical specifications were updated, including:<br>• The minimum value for parameter DC10 ($V_{DD}$) in the DC Temperature and Voltage Specifications was updated (see Table 37-4).<br>• The minimum and maximum values for parameter BO10 ($V_{BOR}$) were updated in the BOR Electrical Characteristics (see Table 37-4).<br>• Updated the third and fourth bullet list items in Note 2 in DC Characteristics: Operating Current ($I_{DD}$) (see Table 37-6).<br>• Updated the third and fourth bullet list items in Note 1 in DC Characteristics: Idle Current ($I_{IDLE}$) (see Table 37-7).<br>• Updated the third and fourth bullet list items in Note 1in DC Characteristics: Power-Down Current ($I_{PD}$) (see Table 37-8).<br>• Added Note 6 and updated parameters DI20, DI28a, DI28b, DI30, and DI31 in DC Characteristics: I/O Pin Input Specifications (see Table 37-9).<br>• Added DC Characteristics: I/O Pin Input Injection Current Specifications (see Table 37-10).<br>• Added parameter DO50 to Capacitive Loading Requirements on Output Pins (see Table 37-15).<br>• Note 3 was added and the Conditions were updated for parameter OS42 in the External Clock Timing Requirements (see Table 37-16).<br>• Updated the Minimum value for parameter OS51 ($F_{SYS}$) in the System Timing Requirements (see Table 37-17).<br>• Added parameter OS54a and updated the Maximum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 37-18).<br>• The Internal Backup FRC (BFRC) Accuracy specification was added (see Table 37-21).<br>• The SQI Input and Output Timing Characteristics diagram were updated (see Figure 37-14 and Figure 37-15).<br>• The SQI Timing Requirements were updated (see Table 37-33).<br>• Parameter AD13 was removed (see Table 37-37).<br>• The Min. and Max. values for parameter TS12 and the Conditions for parameter TS13 and TS14 in the Temperature Sensor Specifications were updated (see Table 36-39). |
| **38.0 "AC and DC Characteristics Graphs"** | Updated Typical Temperature Sensor Voltage (see Figure 38-7). |
| **Appendix A: "Migrating from PIC32MX5XX/6XX/7XX to PIC32MZ"** | New appendix for migrating to PIC32MZ devices was added. |