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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecm144-i-pl

TABLE 1: PIC32MZ EC FAMILY FEATURES

Device	Program Memory (KB)	Data Memory (KB)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals					Crypto	RNG	DMA Channels (Programmable/Dedicated)	ADC (Channels)	Analog Comparators	USB 2.0 HS OTG	I ² C	PMP	EBI	SQI	RTCC	Ethernet	I/O Pins	JTAG	Trace	
						Remappable Pins	Timers/ Capture/ Compare ⁽¹⁾	UART	SPI/I ² S	External Interrupts ⁽²⁾																CAN 2.0B
PIC32MZ1024ECG064	1024	512	64	TQFP, QFN	160	34	9/9/9	6	4	5	0	N	Y	8/12	24	2	Y	4	Y	N	Y	Y	Y	46	Y	Y
PIC32MZ1024ECH064											2	N	Y	8/16												
PIC32MZ1024ECM064											2	Y	Y	8/18												
PIC32MZ2048ECG064	2048										0	N	Y	8/12												
PIC32MZ2048ECH064											2	N	Y	8/16												
PIC32MZ2048ECM064											2	Y	Y	8/18												
PIC32MZ1024ECG100	1024	512	100	TQFP	160	51	9/9/9	6	6	5	0	N	Y	8/12	40	2	Y	5	Y	Y	Y	Y	78	Y	Y	
PIC32MZ1024ECH100											2	N	Y	8/16												
PIC32MZ1024ECM100											2	Y	Y	8/18												
PIC32MZ2048ECG100	2048										0	N	Y	8/12												
PIC32MZ2048ECH100											2	N	Y	8/16												
PIC32MZ2048ECM100											2	Y	Y	8/18												
PIC32MZ1024ECG124	1024	512	124	VTLA	160	53	9/9/9	6	6	5	0	N	Y	8/12	48	2	Y	5	Y	Y	Y	Y	97	Y	Y	
PIC32MZ1024ECH124											2	N	Y	8/16												
PIC32MZ1024ECM124											2	Y	Y	8/18												
PIC32MZ2048ECG124	2048										0	N	Y	8/12												
PIC32MZ2048ECH124											2	N	Y	8/16												
PIC32MZ2048ECM124											2	Y	Y	8/18												
PIC32MZ1024ECG144	1024	512	144	LQFP, TQFP	160	53	9/9/9	6	6	5	0	N	Y	8/12	48	2	Y	5	Y	Y	Y	Y	120	Y	Y	
PIC32MZ1024ECH144											2	N	Y	8/16												
PIC32MZ1024ECM144											2	Y	Y	8/18												
PIC32MZ2048ECG144	2048										0	N	Y	8/12												
PIC32MZ2048ECH144											2	N	Y	8/16												
PIC32MZ2048ECM144											2	Y	Y	8/18												

Note 1: Eight out of nine timers are remappable.
Note 2: Four out of five external interrupts are remappable.

PIC32MZ Embedded Connectivity (EC) Family

A block diagram of the PIC32MZ EC family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MZ EC FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM

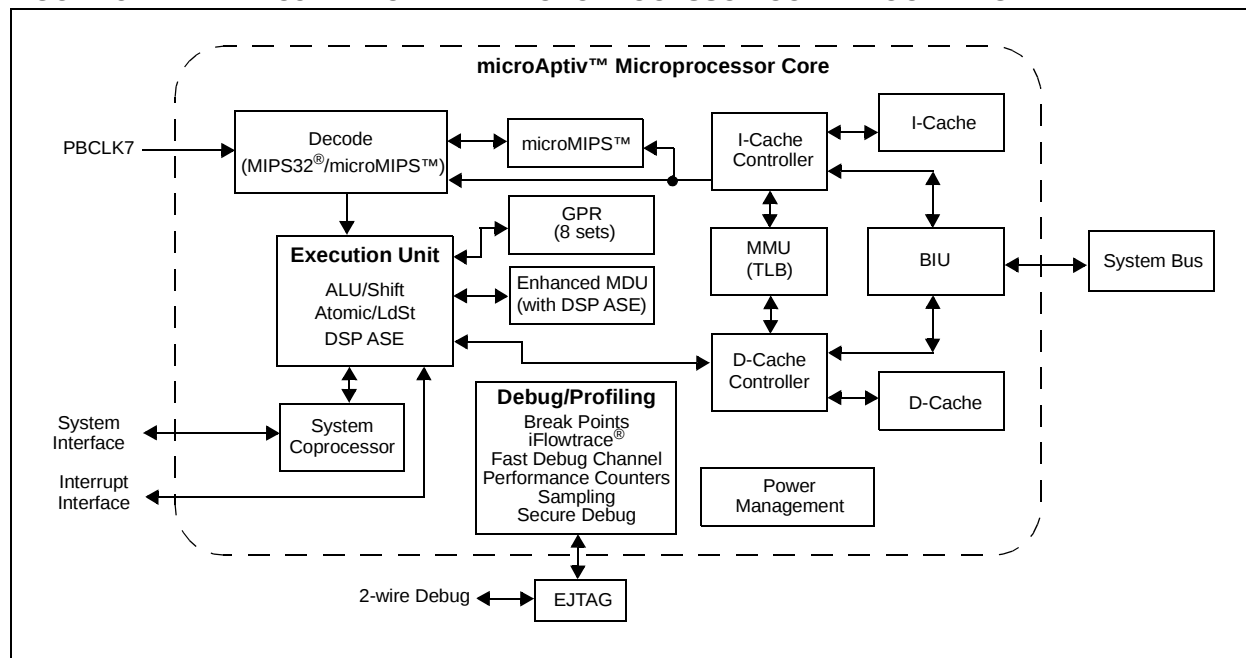


TABLE 4-6: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS

Target Number	Target Description ⁽⁵⁾	SBTxREGy Register							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
0	System Bus	SBT0REG0	R	0x1F8F0000	R	64 KB	—	0	SBT0RD0	R/W ⁽¹⁾	SBT0WR0	R/W ⁽¹⁾
		SBT0REG1	R	0x1F8F8000	R	32 KB	—	3	SBT0RD1	R/W ⁽¹⁾	SBT0WR1	R/W ⁽¹⁾
1	Flash Memory ⁽⁶⁾ : Program Flash Boot Flash Prefetch Module	SBT1REG0	R	0x1D000000	R ⁽⁴⁾	R ⁽⁴⁾	—	0	SBT1RD0	R/W ⁽¹⁾	SBT1WR0	0, 0, 0, 0
		SBT1REG2	R	0x1F8E0000	R	4 KB	1	2	SBT1RD2	R/W ⁽¹⁾	SBT1WR2	R/W ⁽¹⁾
		SBT1REG3	R/W	R/W	R/W	R/W	1	2	SBT1RD3	R/W ⁽¹⁾	SBT1WR3	0, 0, 0, 0
		SBT1REG4	R/W	R/W	R/W	R/W	1	2	SBT1RD4	R/W ⁽¹⁾	SBT1WR4	0, 0, 0, 0
		SBT1REG5	R/W	R/W	R/W	R/W	1	2	SBT1RD5	R/W ⁽¹⁾	SBT1WR5	0, 0, 0, 0
		SBT1REG6	R/W	R/W	R/W	R/W	1	2	SBT1RD6	R/W ⁽¹⁾	SBT1WR6	0, 0, 0, 0
		SBT1REG7	R/W	R/W	R/W	R/W	0	1	SBT1RD7	R/W ⁽¹⁾	SBT1WR7	0, 0, 0, 0
		SBT1REG8	R/W	R/W	R/W	R/W	0	1	SBT1RD8	R/W ⁽¹⁾	SBT1WR8	0, 0, 0, 0
2	RAM Bank 1 Memory	SBT2REG0	R	0x00000000	R ⁽⁴⁾	R ⁽⁴⁾	—	0	SBT2RD0	R/W ⁽¹⁾	SBT2WR0	R/W ⁽¹⁾
		SBT2REG1	R/W	R/W	R/W	R/W	—	3	SBT2RD1	R/W ⁽¹⁾	SBT2WR1	R/W ⁽¹⁾
		SBT2REG2	R/W	R/W	R/W	R/W	0	1	SBT2RD2	R/W ⁽¹⁾	SBT2WR2	R/W ⁽¹⁾
3	RAM Bank 2 Memory	SBT3REG0	R ⁽⁴⁾	R ⁽⁴⁾	R ⁽⁴⁾	R ⁽⁴⁾	—	0	SBT3RD0	R/W ⁽¹⁾	SBT3WR0	R/W ⁽¹⁾
		SBT3REG1	R/W	R/W	R/W	R/W	—	3	SBT3RD1	R/W ⁽¹⁾	SBT3WR1	R/W ⁽¹⁾
		SBT3REG2	R/W	R/W	R/W	R/W	0	1	SBT3RD2	R/W ⁽¹⁾	SBT3WR2	R/W ⁽¹⁾
4	External Memory via EBI and EBI Module ⁽⁶⁾	SBT4REG0	R	0x20000000	R	64 MB	—	0	SBT4RD0	R/W ⁽¹⁾	SBT4WR0	R/W ⁽¹⁾
		SBT4REG2	R	0x1F8E1000	R	4 KB	0	1	SBT4RD2	R/W ⁽¹⁾	SBT4WR2	R/W ⁽¹⁾
5	Peripheral Set 1: System Control Flash Control DMT/WDT RTCC CVR PPS Input PPS Output Interrupts DMA	SBT5REG0	R	0x1F800000	R	128 KB	—	0	SBT5RD0	R/W ⁽¹⁾	SBT5WR0	R/W ⁽¹⁾
		SBT5REG1	R/W	R/W	R/W	R/W	—	3	SBT5RD1	R/W ⁽¹⁾	SBT5WR1	R/W ⁽¹⁾
		SBT5REG2	R/W	R/W	R/W	R/W	0	1	SBT5RD2	R/W ⁽¹⁾	SBT5WR2	R/W ⁽¹⁾

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

- Note**
- Reset values for these bits are '0', '1', '1', '1', respectively.
 - The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.
 - The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)} \times 1024$ bytes. For read-only bits, this value is set by hardware on Reset.
 - Refer to the Device Memory Maps (Figure 4-1 through Figure 4-4) for specific device memory sizes and start addresses.
 - See Table 4-1 for information on specific target memory size and start addresses.
 - The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

TABLE 4-7: SYSTEM BUS REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0510	SBFLAG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	T13PGV	T12PGV	T11PGV	T10PGV	T9PGV	T8PGV	T7PGV	T6PGV	T5PGV	T4PGV	T3PGV	T2PGV	T1PGV	T0PGV	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: SYSTEM BUS TARGET 0 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
8020	SBT0ELOG1	31:16	MULTI	—	—	—	CODE<3:0>			—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000
8024	SBT0ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8028	SBT0ECON	31:16	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8030	SBT0ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8038	SBT0ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8040	SBT0REG0	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
8050	SBT0RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8058	SBT0WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8060	SBT0REG1	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
8070	SBT0RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
8078	SBT0WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1240	RCON	31:16	—	—	—	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	—	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR	0000
1250	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
1260	RNMICON	31:16	—	—	—	—	—	—	DMTO	WDTO	SWNMI	—	—	—	—	—	CF	WDTS	0000
		15:0	—	—	—	—	—	—	—	—	NMICNT<7:0>								0000
1270	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VREGS	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	RW-0, HS	R/W-0, HS	U-0	U-0
	—	—	—	—	BCFGERR	BCFGFAIL	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	U-0
	—	—	—	—	—	—	CMR	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR ⁽¹⁾	POR ⁽¹⁾

Legend:

R = Readable bit

-n = Value at POR

HS = Hardware Set

W = Writable bit

'1' = Bit is set

HC = Hardware Cleared

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit

1 = An error occurred during a read of the primary configuration registers

0 = No error occurred during a read of the primary configuration registers

bit 26 **BCFGFAIL:** Primary/Secondary Configuration Registers Error Flag bit

1 = An error occurred during a read of the primary and alternate configuration registers

0 = No error occurred during a read of the primary and alternate configuration registers

bit 25-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit

1 = A Configuration Mismatch Reset has occurred

0 = A Configuration Mismatch Reset has not occurred

bit 8 **Unimplemented:** Read as '0'

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin Flag bit

1 = Master Clear (pin) Reset has occurred

0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit

1 = Software Reset was executed

0 = Software Reset was not executed

bit 5 **DMTO:** Deadman Timer Time-out Flag bit

1 = A DMT time-out has occurred

0 = A DMT time-out has not occurred

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit

1 = WDT Time-out has occurred

0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit

1 = Device was in Sleep mode

0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit

1 = Device was in Idle mode

0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit⁽¹⁾

1 = Brown-out Reset has occurred

0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit⁽¹⁾

1 = Power-on Reset has occurred

0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view the next detection.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC1 Data 43	_ADC1_DATA43_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
ADC1 Data 44	_ADC1_DATA44_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	Yes
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
Core Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes
System Bus Protection Violation	_SYSTEM_BUS_PROTECTION_VECTOR	106	OFF106<17:1>	IFS3<10>	IEC3<10>	IPC26<20:18>	IPC26<17:16>	Yes
Crypto Engine Event	_CRYPTO_VECTOR	107	OFF107<17:1>	IFS3<11>	IEC3<11>	IPC26<28:26>	IPC26<25:24>	Yes
Reserved	—	108	—	—	—	—	—	—
SPI1 Fault	_SPI1_FAULT_VECTOR	109	OFF109<17:1>	IFS3<13>	IEC3<13>	IPC27<12:10>	IPC27<9:8>	Yes
SPI1 Receive Done	_SPI1_RX_VECTOR	110	OFF110<17:1>	IFS3<14>	IEC3<14>	IPC27<20:18>	IPC27<17:16>	Yes
SPI1 Transfer Done	_SPI1_TX_VECTOR	111	OFF111<17:1>	IFS3<15>	IEC3<15>	IPC27<28:26>	IPC27<25:24>	Yes
UART1 Fault	_UART1_FAULT_VECTOR	112	OFF112<17:1>	IFS3<16>	IEC3<16>	IPC28<4:2>	IPC28<1:0>	Yes
UART1 Receive Done	_UART1_RX_VECTOR	113	OFF113<17:1>	IFS3<17>	IEC3<17>	IPC28<12:10>	IPC28<9:8>	Yes
UART1 Transfer Done	_UART1_TX_VECTOR	114	OFF114<17:1>	IFS3<18>	IEC3<18>	IPC28<20:18>	IPC28<17:16>	Yes
I2C1 Bus Collision Event	_I2C1_BUS_VECTOR	115	OFF115<17:1>	IFS3<19>	IEC3<19>	IPC28<28:26>	IPC28<25:24>	Yes
I2C1 Slave Event	_I2C1_SLAVE_VECTOR	116	OFF116<17:1>	IFS3<20>	IEC3<20>	IPC29<4:2>	IPC29<1:0>	Yes
I2C1 Master Event	_I2C1_MASTER_VECTOR	117	OFF117<17:1>	IFS3<21>	IEC3<21>	IPC29<12:10>	IPC29<9:8>	Yes
PORTA Input Change Interrupt ⁽²⁾	_CHANGE_NOTICE_A_VECTOR	118	OFF118<17:1>	IFS3<22>	IEC3<22>	IPC29<20:18>	IPC29<17:16>	Yes
PORTB Input Change Interrupt	_CHANGE_NOTICE_B_VECTOR	119	OFF119<17:1>	IFS3<23>	IEC3<23>	IPC29<28:26>	IPC29<25:24>	Yes
PORTC Input Change Interrupt	_CHANGE_NOTICE_C_VECTOR	120	OFF120<17:1>	IFS3<24>	IEC3<24>	IPC30<4:2>	IPC30<1:0>	Yes
PORTD Input Change Interrupt	_CHANGE_NOTICE_D_VECTOR	121	OFF121<17:1>	IFS3<25>	IEC3<25>	IPC30<12:10>	IPC30<9:8>	Yes
PORTE Input Change Interrupt	_CHANGE_NOTICE_E_VECTOR	122	OFF122<17:1>	IFS3<26>	IEC3<26>	IPC30<20:18>	IPC30<17:16>	Yes
PORTF Input Change Interrupt	_CHANGE_NOTICE_F_VECTOR	123	OFF123<17:1>	IFS3<27>	IEC3<27>	IPC30<28:26>	IPC30<25:24>	Yes
PORTG Input Change Interrupt	_CHANGE_NOTICE_G_VECTOR	124	OFF124<17:1>	IFS3<28>	IEC3<28>	IPC31<4:2>	IPC31<1:0>	Yes
PORTH Input Change Interrupt ^(2,3)	_CHANGE_NOTICE_H_VECTOR	125	OFF125<17:1>	IFS3<29>	IEC3<29>	IPC31<12:10>	IPC31<9:8>	Yes
PORTJ Input Change Interrupt ^(2,3)	_CHANGE_NOTICE_J_VECTOR	126	OFF126<17:1>	IFS3<30>	IEC3<30>	IPC31<20:18>	IPC31<17:16>	Yes
PORTK Input Change Interrupt ^(2,3,4)	_CHANGE_NOTICE_K_VECTOR	127	OFF127<17:1>	IFS3<31>	IEC3<31>	IPC31<28:26>	IPC31<25:24>	Yes
Parallel Master Port	_PMP_VECTOR	128	OFF128<17:1>	IFS4<0>	IEC4<0>	IPC32<4:2>	IPC32<1:0>	Yes

- Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EC Family Features”** for the list of available peripherals.
- 2:** This interrupt source is not available on 64-pin devices.
- 3:** This interrupt source is not available on 100-pin devices.
- 4:** This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
0808	OFF178 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
080C	OFF179	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0810	OFF180	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0814	OFF181	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0818	OFF182	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
081C	OFF183	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0820	OFF184	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0824	OFF185 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0828	OFF186 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
082C	OFF187 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0830	OFF188	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0834	OFF189	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—
0838	OFF190	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>	0000
		15:0	VOFF<15:1>															—

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note 1:** All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
- 2:** This bit or register is not available on 64-pin devices.
- 3:** This bit or register is not available on devices without a CAN module.
- 4:** This bit or register is not available on 100-pin devices.
- 5:** Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6:** Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7:** This bit or register is not available on devices without a Crypto module.
- 8:** This bit or register is not available on 124-pin devices.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO ⁽¹⁾	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0> ⁽¹⁾				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP ⁽¹⁾	CRCTYP	—	—	CRCCH<2:0>		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits

11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)

10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)

01 = Endian byte swap on word boundaries (i.e., reverse source byte order)

00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit⁽¹⁾

1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>

0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)

0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)

0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits⁽¹⁾

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit

1 = CRC module is enabled and channel transfers are routed through the CRC module

0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 VBUSERRIE	R/W-0 SESSRQIE	R/W-0 DISCONIE	R/W-0 CONNIE	R/W-0 SOFIE	R/W-1 RESETIE	R/W-1 RESUMEIE	R/W-0 SUSPIE
23:16	R-0, HS VBUSERRIF	R-0, HS SESSRQIF	R-0, HS DISCONIF	R-0, HS CONNIF	R-0, HS SOFIF	R-0, HS RESETIF	R-0, HS RESUMEIF	R-0, HS SUSPIF
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/W-1 EP7RXIE	R/W-1 EP6RXIE	R/W-1 EP5RXIE	R/W-1 EP4RXIE	R/W-1 EP3RXIE	R/W-1 EP2RXIE	R/W-1 EP1RXIE	U-0 —

Legend:

R = Readable bit

-n = Value at POR

HS = Hardware Settable

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **VBUSERRIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled
- bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled
- bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled
- bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled
- bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled
- bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled
- bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled
- bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled
- bit 23 **VBUSERRIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt
- bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected
- bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected
- bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7) (CONTINUED)

- bit 23 **INCOMPTX**: Incomplete TX Status bit (Device mode)
1 = For high-bandwidth Isochronous endpoint, a large packet has been split into two or three packets for transmission but insufficient IN tokens have been received to send all the parts
0 = Normal operation
In anything other than isochronous transfers, this bit will always return '0'.
- NAKTMOUT**: NAK Time-out status bit (Host mode)
1 = TX endpoint is halted following the receipt of NAK responses for longer than the NAKLIM setting
0 = Written by software to clear this bit
- bit 22 **CLRDT**: Clear Data Toggle Control bit
1 = Resets the endpoint data toggle to '0'
0 = Do not clear the data toggle
- bit 21 **SENTSTALL**: STALL handshake transmission status bit (Device mode)
1 = STALL handshake is transmitted. The FIFO is flushed and the TXPKTRDY bit is cleared.
0 = Written by software to clear this bit
- RXSTALL**: STALL receipt bit (Host mode)
1 = STALL handshake is received. Any DMA request in progress is stopped, the FIFO is completely flushed and the TXPKTRDY bit is cleared.
0 = Written by software to clear this bit
- bit 20 **SENDSTALL**: STALL handshake transmission control bit (Device mode)
1 = Issue a STALL handshake to an IN token
0 = Terminate stall condition
This bit has no effect when the endpoint is being used for Isochronous transfers.
- SETUPPKT**: Definition bit (Host mode)
1 = When set at the same time as the TXPKTRDY bit is set, send a SETUP token instead of an OUT token for the transaction. This also clears the Data Toggle.
0 = Normal OUT token for the transaction
- bit 19 **FLUSH**: FIFO Flush control bit
1 = Flush the latest packet from the endpoint TX FIFO. The FIFO pointer is reset, TXPKTRDY is cleared and an interrupt is generated.
0 = Do not flush the FIFO
- bit 18 **UNDERRUN**: Underrun status bit (Device mode)
1 = An IN token has been received when TXPKTRDY is not set.
0 = Written by software to clear this bit.
- ERROR**: Handshake failure status bit (Host mode)
1 = Three attempts have been made to send a packet and no handshake packet has been received
0 = Written by software to clear this bit.
- bit 17 **FIFONE**: FIFO Not Empty status bit
1 = There is at least 1 packet in the TX FIFO
0 = TX FIFO is empty
- bit 16 **TXPKTRDY**: TX Packet Ready Control bit
The software sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. This bit is also automatically cleared prior to loading a second packet into a double-buffered FIFO.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXINTERV<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **RXFIFOSZ<3:0>**: Receive FIFO Size bits

1111 = Reserved

1110 = Reserved

1101 = 8192 bytes

1100 = 4096 bytes

•

•

•

0011 = 8 bytes

0010 = Reserved

0001 = Reserved

0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 27-24 **TXFIFOSZ<3:0>**: Transmit FIFO Size bits

1111 = Reserved

1110 = Reserved

1101 = 8192 bytes

1100 = 4096 bytes

•

•

•

0011 = 8 bytes

0010 = Reserved

0001 = Reserved

0000 = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 23-16 **Unimplemented**: Read as '0'

PIC32MZ Embedded Connectivity (EC) Family

NOTES:

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 20-4: SQ1CON: SQI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	DASSERT	DEVSEL<1:0>	DEVSEL<1:0>	LANEMODE<1:0>	LANEMODE<1:0>	CMDINIT<1:0>	CMDINIT<1:0>
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **DASSERT:** Chip Select Assert bit

1 = Chip Select is deasserted after transmission or reception of the specified number of bytes

0 = Chip Select is not deasserted after transmission or reception of the specified number of bytes

bit 21-20 **DEVSEL<1:0>:** SQI Device Select bits

11 = Reserved

10 = Reserved

01 = Select Device 1

00 = Select Device 0

bit 19-18 **LANEMODE<1:0>:** SQI Lane Mode Select bits

11 = Reserved

10 = Quad Lane mode

01 = Dual Lane mode

00 = Single Lane mode

bit 17-16 **CMDINIT<1:0>:** Command Initiation Mode Select bits

If it is Transmit, commands are initiated based on a write to the transmit register or the contents of TX FIFO. If CMDINIT is Receive, commands are initiated based on reads to the read register or RX FIFO availability.

11 = Reserved

10 = Receive

01 = Transmit

00 = Idle

bit 15-0 **TXRXCOUNT<15:0>:** Transmit/Receive Count bits

These bits specify the total number of bytes to transmit or received (based on CMDINIT)

26.1 Crypto Engine Control Registers

TABLE 26-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E-#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>			START	ACTIVE	0000	
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>							0000	
5024	CETRLLN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	TRLRLN<7:0>							0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 28-13: AD1CMPn: ADC1 DIGITAL COMPARATOR REGISTER 'n' ('n' = 1, 2, 3, 4, 5 OR 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPhi<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPhi<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPLo<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCMPLo<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-16 **ADCMPhi<15:0>**: Digital Analog Comparator High Limit Value bits
These bits store the high limit value, which is used for comparisons with the analog-to-digital conversion data. The user is responsible for formatting the data as signed or unsigned to match the data format as specified by the SHxMOD<1:0> bits for the associated S&H circuit and the FRACT bit.
- bit 15-0 **ADCMPLo<15:0>**: Digital Analog Comparator Low Limit Value bits
These bits store the low limit value, which is used for comparisons with the analog-to-digital conversion data. The user is responsible for formatting the data as signed or unsigned to match the data format as specified by the SHxMOD<1:0> bits for the associated S&H circuit and the FRACT bit.

Note: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 29-21: C*i*FIFOINT*n*: CAN FIFO INTERRUPT REGISTER (n = 0 THROUGH 31)

- bit 9 **TXHALFIF**: FIFO Transmit FIFO Half Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a Transmit Buffer)
 1 = FIFO is $\leq$ half full
 0 = FIFO is $>$ half full
 TXEN = 0: (FIFO configured as a Receive Buffer)
 Unused, reads '0'
- bit 8 **TXEMPTYIF**: Transmit FIFO Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a Transmit Buffer)
 1 = FIFO is empty
 0 = FIFO is not empty, at least 1 message queued to be transmitted
 TXEN = 0: (FIFO configured as a Receive Buffer)
 Unused, reads '0'
- bit 7-4 **Unimplemented**: Read as '0'
- bit 3 **RXOVFLIF**: Receive FIFO Overflow Interrupt Flag bit
 TXEN = 1: (FIFO configured as a Transmit Buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a Receive Buffer)
 1 = Overflow event has occurred
 0 = No overflow event occurred
- bit 2 **RXFULLIF**: Receive FIFO Full Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a Transmit Buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a Receive Buffer)
 1 = FIFO is full
 0 = FIFO is not full
- bit 1 **RXHALFIF**: Receive FIFO Half Full Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a Transmit Buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a Receive Buffer)
 1 = FIFO is $\geq$ half full
 0 = FIFO is $<$ half full
- bit 0 **RXEMPTYIF**: Receive Buffer Not Empty Interrupt Flag bit⁽¹⁾
 TXEN = 1: (FIFO configured as a Transmit Buffer)
 Unused, reads '0'
 TXEN = 0: (FIFO configured as a Receive Buffer)
 1 = FIFO is not empty, has at least 1 message
 0 = FIFO is empty

Note 1: This bit is read-only and reflects the status of the FIFO.

TABLE 34-3: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽²⁾	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
0000	CFGCON	31:16	—	—	—	—	—	—	DMAPRI	CPUPRI	—	—	—	—	—	—	ICACLK	OCACLK	0000	
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	USBSEN	—	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN	000B	
0020	DEVID	31:16	VER<3:0>					DEVID<27:16>											XXXX	
		15:0	DEVID<15:0>																	XXXX
0030	SYSKEY	31:16	SYSKEY<31:0>																	0000
		15:0	SYSKEY<31:0>																	0000
00C0	CFGEBIA ⁽²⁾	31:16	EBIPINEN	—	—	—	—	—	—	—	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN	0000	
		15:0	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN	0000	
00D0	CFGEBIC ⁽²⁾	31:16	—	EBI RDYINV3	EBI RDYINV2	EBI RDYINV1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—	—	—	—	—	—	EBI RDYLV1	EBIRPEN	0000	
		15:0	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0	0000	
00E0	CFGPG	31:16	—	—	—	—	—	CRYPTPG<1:0>			FCPG<1:0>		SQI1PG<1:0>		—	—	ETHPG<1:0>		0000	
		15:0	CAN2PG<1:0>			CAN1PG<1:0>			—	—	USBPG<1:0>			—	—	DMPAG<1:0>		—	—	CPUPG<1:0>

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

2: This register is not available on 64-pin devices.

TABLE 34-4: DEVICE ADC CALIBRATION SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	DEVADC1	31:16	ADC Calibration Data <31:16>																XXXX
		15:0	ADC Calibration Data <15:0>																XXXX
4004	DEVADC2	31:16	ADC Calibration Data <31:16>																XXXX
		15:0	ADC Calibration Data <15:0>																XXXX
4008	DEVADC3	31:16	ADC Calibration Data <31:16>																XXXX
		15:0	ADC Calibration Data <15:0>																XXXX
400C	DEVADC4	31:16	ADC Calibration Data <31:16>																XXXX
		15:0	ADC Calibration Data <15:0>																XXXX
4010	DEVADC5	31:16	ADC Calibration Data <31:16>																XXXX
		15:0	ADC Calibration Data <15:0>																XXXX

Legend: x = unknown value on Reset.

Note 1: Reset values are dependent on the device variant.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 37-7: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T _A ≤ +85°C for Industrial	
Parameter No.	Typical ⁽²⁾	Maximum	Units	Conditions
Idle Current (I_{IDLE}): Core Off, Clock on Base Current (Note 1)				
DC30a	7	22	mA	4 MHz (Note 3)
DC31a	8	24	mA	10 MHz
DC32a	13	32	mA	60 MHz (Note 3)
DC33a	21	42	mA	130 MHz (Note 3)
DC34	26	48	mA	180 MHz (Note 3)
DC35	28	52	mA	200 MHz

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL is disabled (USBPMD = 1), VUSB3v3 is connected to Vss, PBCLKx divisor = 1:128 ('x' ≠ 7)
 - CPU is in Idle mode (CPU core Halted)
 - L1 Cache and Prefetch modules are disabled
 - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared (except USBPMD)
 - WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to Vss
 - MCLR = V_{DD}
 - RTCC and JTAG are disabled
- 2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** This parameter is characterized, but not tested in manufacturing.

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