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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® microAptiv™
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, SPI, SSI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 48x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048ecm144t-i-ph

PIC32MZ Embedded Connectivity (EC) Family

TABLE 4: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)		A17	B13	B29	A34
PIC32MZ0512EC(E/F/K)124 PIC32MZ1024EC(G/H/M)124 PIC32MZ1024EC(E/F/K)124 PIC32MZ2048EC(G/H/M)124			B1	B56	B41
		A1			A51
		Polarity Indicator		A68	
Package Pin #	Full Pin Name		Package Pin #	Full Pin Name	
B1	EBIA5/AN34/PMA5/RA5		B29	Vss	
B2	EBID6/AN16/PMD6/RE6		B30	D+	
B3	EBIA6/AN22/RPC1/PMA6/RC1		B31	RPF2/SDA3/RF2	
B4	AN36/ETXD1/RJ9		B32	ERXD0/RH8	
B5	EBIWE/AN20/RPC3/PMWR/RC3		B33	ECOL/RH10	
B6	AN14/C1IND/RPG6/SCK2/RG6		B34	EBIRDY1/SDA2/RA3	
B7	EBIA3/AN12/C2IND/RPG8/SCL4/PMA3/RG8		B35	VDD	
B8	VDD		B36	EBIA9/RPF4/SDA5/PMA9/RF4	
B9	EBIA2/AN11/C2INC/RPG9/PMA2/RG9		B37	RPA14/SCL1/RA14	
B10	AN25/RPE8/RE8		B38	EBIA15/RPD9/PMCS2/PMA15/RD9	
B11	AN45/C1INA/RPB5/RB5		B39	EMDC/RPD11/RD11	
B12	AN37/ERXCLK/EREFCLK/RJ11		B40	ERXDV/ECRSRV/RH13	
B13	Vss		B41	SOSCI/RPC13/RC13	
B14	PGEC2/AN46/RPB6/RB6		B42	EBID14/RPD2/PMD14/RD2	
B15	VREF-/CVREF-/AN27/RA9		B43	EBID12/RPD12/PMD12/RD12	
B16	AVDD		B44	ETXERR/RJ0	
B17	AN38/ETXD2/RH0		B45	EBIRDY3/RJ2	
B18	EBIA10/AN48/RPB8/PMA10/RB8		B46	SQICS1/RPD5/RD5	
B19	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10		B47	ETXCLK/RPD7/RD7	
B20	Vss		B48	Vss	
B21	TCK/EBIA19/AN29/RA1		B49	EBID10/RPF1/PMD10/RF1	
B22	TDO/EBIA17/AN31/RPF12/RF12		B50	EBID8/RPG0/PMD8/RG0	
B23	AN8/RB13		B51	TRD3/SQID3/RA7	
B24	EBIA0/AN10/RPB15/OCFB/PMA0/RB15		B52	EBID0/PMD0/RE0	
B25	VDD		B53	VDD	
B26	AN41/ERXD1/RH5		B54	TRD2/SQID2/RG14	
B27	AN32/AETXD0/RPD14/RD14		B55	TRD0/SQID0/RG13	
B28	OSC1/CLKI/RC12		B56	EBID3/RPE3/PMD3/RE3	

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 “Peripheral Pin Select (PPS)”** for restrictions.
 - 2: Every I/O port pin (RAX-RJx) can be used as a change notification pin (CNAX-CNJx). See **Section 12.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.
 - 4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTA							
RA0	—	17	A11	22	I/O	ST	PORTA is a bidirectional I/O port
RA1	—	38	B21	56	I/O	ST	
RA2	—	59	A41	85	I/O	ST	
RA3	—	60	B34	86	I/O	ST	
RA4	—	61	A42	87	I/O	ST	
RA5	—	2	B1	2	I/O	ST	
RA6	—	89	A61	129	I/O	ST	
RA7	—	90	B51	130	I/O	ST	
RA9	—	28	B15	39	I/O	ST	
RA10	—	29	A20	40	I/O	ST	
RA14	—	66	B37	95	I/O	ST	
RA15	—	67	A45	96	I/O	ST	
PORTB							
RB0	16	25	A18	36	I/O	ST	PORTB is a bidirectional I/O port
RB1	15	24	A17	35	I/O	ST	
RB2	14	23	A16	34	I/O	ST	
RB3	13	22	A14	31	I/O	ST	
RB4	12	21	A13	26	I/O	ST	
RB5	11	20	B11	25	I/O	ST	
RB6	17	26	B14	37	I/O	ST	
RB7	18	27	A19	38	I/O	ST	
RB8	21	32	B18	47	I/O	ST	
RB9	22	33	A23	48	I/O	ST	
RB10	23	34	B19	49	I/O	ST	
RB11	24	35	A24	50	I/O	ST	
RB12	27	41	A27	59	I/O	ST	
RB13	28	42	B23	60	I/O	ST	
RB14	29	43	A28	61	I/O	ST	
RB15	30	44	B24	62	I/O	ST	
PORTC							
RC1	—	6	B3	6	I/O	ST	PORTC is a bidirectional I/O port
RC2	—	7	A6	11	I/O	ST	
RC3	—	8	B5	12	I/O	ST	
RC4	—	9	A7	13	I/O	ST	
RC12	31	49	B28	71	I/O	ST	
RC13	47	72	B41	105	I/O	ST	
RC14	48	73	A49	106	I/O	ST	
RC15	32	50	A33	72	I/O	ST	

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-14: USB PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
VBUS	33	51	A35	73	I	Analog	USB bus power monitor
VUSB3V3	34	52	A36	74	P	—	USB internal transceiver supply. If the USB module is <i>not</i> used, this pin must be connected to Vss. When connected, the shared pin functions on USBID will <i>not</i> be available.
D+	37	55	B30	77	I/O	Analog	USB D+
D-	36	54	A37	76	I/O	Analog	USB D-
USBID	38	56	A38	78	I	ST	USB OTG ID detect

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer

Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select

P = Power
 I = Input

TABLE 1-15: CAN1 AND CAN2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
C1TX	PPS	PPS	PPS	PPS	O	—	CAN1 Bus Transmit Pin
C1RX	PPS	PPS	PPS	PPS	I	ST	CAN1 Bus Receive Pin
C2TX	PPS	PPS	PPS	PPS	O	—	CAN2 Bus Transmit Pin
C2RX	PPS	PPS	PPS	PPS	I	ST	CAN2 Bus Receive Pin

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer

Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select

P = Power
 I = Input

PIC32MZ Embedded Connectivity (EC) Family

TABLE 1-16: ETHERNET MII I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
ERXD0	61	41	B32	81	I	ST	Ethernet Receive Data 0
ERXD1	58	42	B26	66	I	ST	Ethernet Receive Data 1
ERXD2	57	43	A31	67	I	ST	Ethernet Receive Data 2
ERXD3	56	44	A40	82	I	ST	Ethernet Receive Data 3
ERXERR	64	35	A30	65	I	ST	Ethernet Receive Error Input
ERXDV	62	12	B40	101	I	ST	Ethernet Receive Data Valid
ERXCLK	63	16	B12	27	I	ST	Ethernet Receive Clock
ETXD0	2	86	A5	7	O	—	Ethernet Transmit Data 0
ETXD1	3	85	B4	8	O	—	Ethernet Transmit Data 1
ETXD2	43	79	B17	43	O	—	Ethernet Transmit Data 2
ETXD3	46	80	A22	44	O	—	Ethernet Transmit Data 3
ETXERR	50	87	B44	114	O	—	Ethernet Transmit Error
ETXEN	1	77	A57	120	O	—	Ethernet Transmit Enable
ETXCLK	51	78	B47	121	I	ST	Ethernet Transmit Clock
ECOL	44	10	B33	83	I	ST	Ethernet Collision Detect
ECRS	45	11	A47	100	I	ST	Ethernet Carrier Sense
EMDC	30	70	B39	99	O	—	Ethernet Management Data Clock
EMDIO	49	71	A55	115	I/O	—	Ethernet Management Data

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

TABLE 1-17: ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Ethernet MII Interface							
ERXD0	61	41	B32	81	I	ST	Ethernet Receive Data 0
ERXD1	58	42	B26	66	I	ST	Ethernet Receive Data 1
ERXERR	64	35	A30	65	I	ST	Ethernet Receive Error Input
ETXD0	2	86	A5	7	O	—	Ethernet Transmit Data 0
ETXD1	3	85	B4	8	O	—	Ethernet Transmit Data 1
ETXEN	1	77	A57	120	O	—	Ethernet Transmit Enable
EMDC	30	70	B39	99	O	—	Ethernet Management Data Clock
EMDIO	49	71	A55	115	I/O	—	Ethernet Management Data
EREFCLK	63	16	B12	27	I	ST	Ethernet Reference Clock
ECRSDV	62	12	B40	101	I	ST	Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

PIC32MZ Embedded Connectivity (EC) Family

2.11 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-9 and Figure 2-10.

FIGURE 2-9: AUDIO PLAYBACK APPLICATION

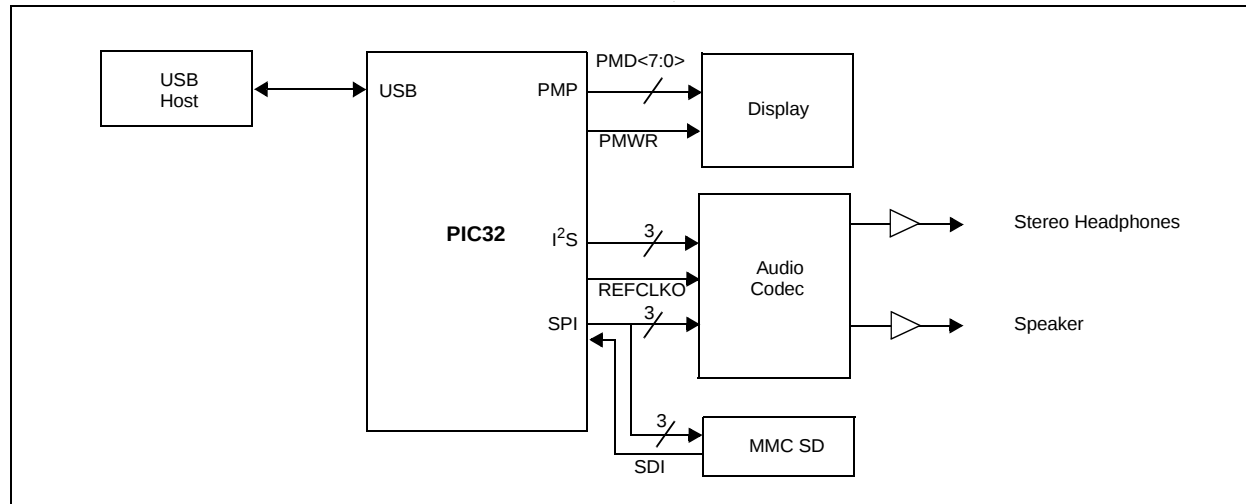


FIGURE 2-10: LOW-COST CONTROLLERLESS (LCC) GRAPHICS APPLICATION WITH PROJECTED CAPACITIVE TOUCH

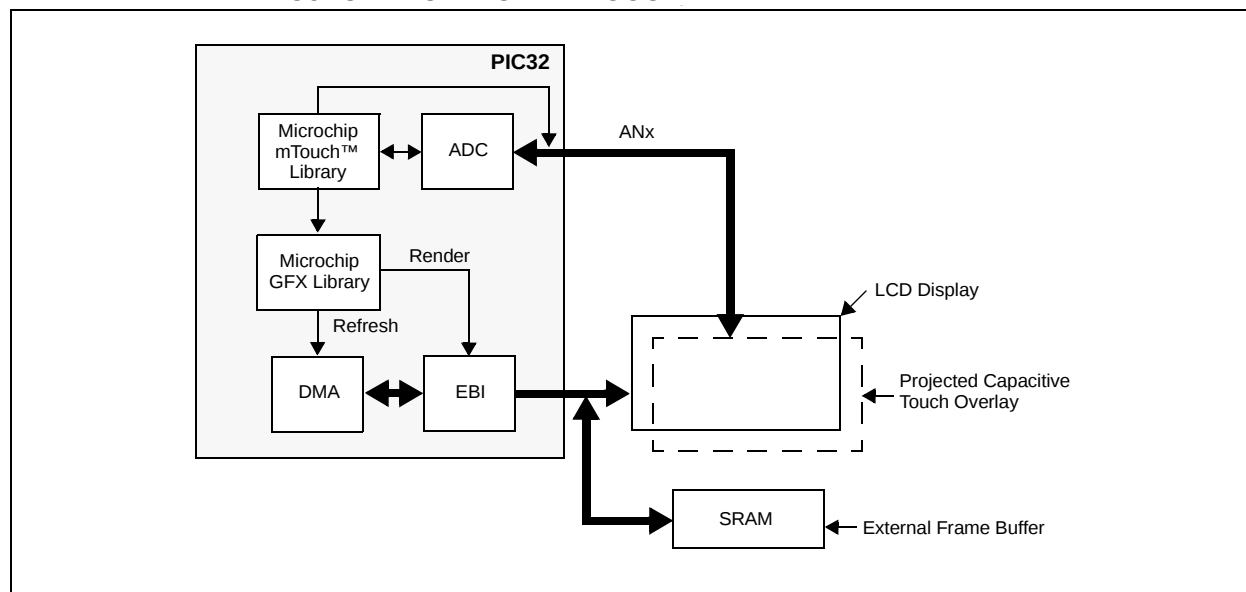


TABLE 4-10: SYSTEM BUS TARGET 2 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
8820	SBT2ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000	
8824	SBT2ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>			0000	
8828	SBT2ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
8830	SBT2ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000	
8838	SBT2ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000	
8840	SBT2REG0	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8850	SBT2RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX	
8858	SBT2WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX	
8860	SBT2REG1	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8870	SBT2RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX	
8878	SBT2WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX	
8880	SBT2REG2	31:16	BASE<21:6>															XXXX	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	XXXX	
8890	SBT2RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX	
8898	SBT2WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	XXXX	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000	
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>			0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx	
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx	
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx	
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMTO	WDTO
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	SWNMI	—	—	—	—	—	CF	WDTS
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DMTO:** Deadman Timer Time-out Flag bit

1 = DMT time-out has occurred and caused a NMI

0 = DMT time-out has not occurred

Setting this bit will cause a DMT NMI event, and NMICNT will begin counting.

bit 24 **WDTO:** Watchdog Timer Time-Out Flag bit

1 = WDT time-out has occurred and caused a NMI

0 = WDT time-out has not occurred

Setting this bit will cause a WDT NMI event, and NMICNT will begin counting.

bit 23 **SWNMI:** Software NMI Trigger.

1 = An NMI will be generated

0 = An NMI will not be generated

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **CF:** Clock Fail Detect bit

1 = FSCM has detected clock failure and caused an NMI

0 = FSCM has not detected clock failure

Setting this bit will cause a CF NMI event, but will not cause a clock switch to the BFRC.

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit

1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep

0 = WDT time-out has not occurred during Sleep mode

Setting this bit will cause a WDT NMI.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NMICNT<7:0>:** NMI Reset Counter Value bits

These bits specify the reload value used by the NMI reset counter.

11111111-00000001 = Number of SYSCLK cycles before a device Reset occurs⁽¹⁾

00000000 = No delay between NMI assertion and device Reset event

Note 1: When a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is triggered the NMICNT will start decrementing. When NMICNT reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the "PIC32 Family Reference Manual" for details.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
069C	OFF087 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06A0	OFF088 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06A4	OFF089 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06A8	OFF090 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06AC	OFF091 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06B0	OFF092 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06B4	OFF093 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06B8	OFF094 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06BC	OFF095 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06C0	OFF096 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06C4	OFF097 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06C8	OFF098 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06CC	OFF099 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06D0	OFF100 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—
06D4	OFF101 ^(2,4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>																—

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP

Virtual Address (BF81_#)	Register Name(i)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1060	DCH0CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	—	0000
1070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0	CHSSA<31:0>																0000
10A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0	CHDSA<31:0>																0000
10B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
10C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
10D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
10E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
10F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1120	DCH1CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	—	0000
1130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0	CHSSA<31:0>																0000
1160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0	CHDSA<31:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

PIC32MZ Embedded Connectivity (EC) Family

12.1 Parallel I/O (PIO) Ports

All port pins have ten registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

12.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

Refer to the pin name tables (Table 2 through Table 5) for the available pins and their functionality.

12.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

12.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an NOP.

12.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MZ EC devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note: Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

An additional control register (CNCONx) is shown in Register 12-3.

12.2 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

TABLE 12-21: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1488	U5RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U5RXR<3:0>				0000
148C	U5CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U5CTSR<3:0>				0000
1490	U6RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U6RXR<3:0>				0000
1494	U6CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U6CTSR<3:0>				0000
149C	SDI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI1R<3:0>				0000
14A0	SS1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS1R<3:0>				0000
14A8	SDI2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI2R<3:0>				0000
14AC	SS2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS2R<3:0>				0000
14B4	SDI3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI3R<3:0>				0000
14B8	SS3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS3R<3:0>				0000
14C0	SDI4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI4R<3:0>				0000
14C4	SS4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS4R<3:0>				0000
14CC	SDI5R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI5R<3:0>				0000
14D0	SS5R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS5R<3:0>				0000
14D8	SDI6R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI6R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
2: This register is not available on devices without a CAN module.

PIC32MZ Embedded Connectivity (EC) Family

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON ⁽¹⁾	—	SIDL ⁽²⁾	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE ⁽¹⁾	TCKPS<2:0> ⁽¹⁾			T32 ⁽³⁾	—	TCS ⁽¹⁾	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit⁽¹⁾

1 = Module is enabled

0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit⁽²⁾

1 = Discontinue operation when device enters Idle mode

0 = Continue operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽¹⁾

When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits⁽¹⁾

111 = 1:256 prescale value

110 = 1:64 prescale value

101 = 1:32 prescale value

100 = 1:16 prescale value

011 = 1:8 prescale value

010 = 1:4 prescale value

001 = 1:2 prescale value

000 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timer Mode Select bit⁽³⁾

1 = Odd numbered and even numbered timers form a 32-bit timer

0 = Odd numbered and even numbered timers form a separate 16-bit timer

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

21.1 I²C Control Registers

TABLE 21-1: I2C1 THROUGH I2C5 REGISTER MAP

Virtual Address (BF82_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0010	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0020	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Address Register							0000
0030	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Address Mask Register							0000
0040	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Baud Rate Generator Register							0000
0050	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Transmit Register							0000
0060	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Receive Register							0000
0200	I2C2CON ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0210	I2C2STAT ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0220	I2C2ADD ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Address Register							0000
0230	I2C2MSK ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Address Mask Register							0000
0240	I2C2BRG ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Baud Rate Generator Register							0000
0250	I2C2TRN ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Transmit Register							0000
0260	I2C2RCV ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Receive Register							0000
0400	I2C3CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0410	I2C3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0420	I2C3ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	Address Register							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

2: This register is not available on 64-pin devices.

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REGISTER 24-1: EBICSx: EXTERNAL BUS INTERFACE CHIP SELECT REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **CSADDR<15:0>**: Base Address for Device bits

Address in physical memory, which will select the external device.

bit 15-0 **Unimplemented**: Read as '0'

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REGISTER 28-11: AD1CMPCONn: ADC1 DIGITAL COMPARATOR CONTROL REGISTER 'n'
(‘n’ = 1, 2, 3, 4, 5, OR 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	AINID<4:0>				
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN ⁽¹⁾	DCMPED	IEBTWN ⁽¹⁾	IEHIHI ⁽¹⁾	IEHILO ⁽¹⁾	IELOHI ⁽¹⁾	IELOLO ⁽¹⁾

Legend:	HS = Hardware Set	HC = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12-8 **AINID<4:0>:** Analog Input Identification (ID) bits

When a digital comparator event occurs, these read-only bits contain the analog input identification number. AINID = ANx, where ‘x’ = 0-31.

bit 7 **ENDCMP:** Digital Comparator Enable bit

1 = Digital Comparator is enabled

0 = Digital Comparator is not enabled, and the DCMPEP status bit is cleared

bit 6 **DCMPGIEN:** Digital Comparator Global ADC Interrupt Enable bit⁽¹⁾

1 = A Digital Comparator Event (DCMPED transitions from ‘0’ to ‘1’) will generate a Global ADC interrupt.

0 = A Digital Comparator Event will not generate a Global ADC interrupt.

bit 5 **DCMPED:** Digital Comparator Event Detected Status bit

1 = This bit is set by the digital comparator hardware when a comparison event is detected. An interrupt will be generated if the appropriate bit in the IECx register is set or if enabled for the ADC Global interrupt in the DCMPEP bit.

0 = This bit is cleared by reading the AINID<4:0> bits or when the ADC module is disabled

bit 4 **IEBTWN:** Between Low/High Digital Comparator Event bit⁽¹⁾

1 = Generate a digital comparator event when ADCMPLO<15:0> ≤ DATA<31:0> < ADCMPHI<15:0>

0 = Do not generate a digital comparator event

bit 3 **IEHIHI:** High/High Digital Comparator Event bit⁽¹⁾

1 = Generate a Digital Comparator Event when ADCMPHI<15:0> ≤ DATA<31:0>

0 = Do not generate a digital comparator event when ADCMPHI<15:0> ≤ DATA<31:0>

bit 2 **IEHILO:** High/Low Digital Comparator Event bit⁽¹⁾

1 = Generate a Digital Comparator Event when DATA<31:0> < ADCMPHI<15:0>

0 = Do not generate a digital comparator event when DATA<31:0> < ADCMPHI<15:0>

bit 1 **IELOHI:** Low/High Digital Comparator Event bit⁽¹⁾

1 = Generate a Digital Comparator Event when ADCMPLO<15:0> ≤ DATA<31:0>

0 = Do not generate a digital comparator event when ADCMPLO<15:0> ≤ DATA<31:0>

bit 0 **IELOLO:** Low/Low Digital Comparator Event bit⁽¹⁾

1 = Generate a Digital Comparator Event when DATA<31:0> < ADCMPLO<15:0>

0 = Do not generate a digital comparator event when DATA<31:0> < ADCMPLO<15:0>

Note 1: Changing these bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

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30.0 ETHERNET CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ Embedded Connectivity (EC) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 35. "Ethernet Controller"** (DS60001155), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Ethernet controller is a bus master module that interfaces with an off-chip Physical Layer (PHY) to implement a complete Ethernet node in a system.

Key features of the Ethernet Controller include:

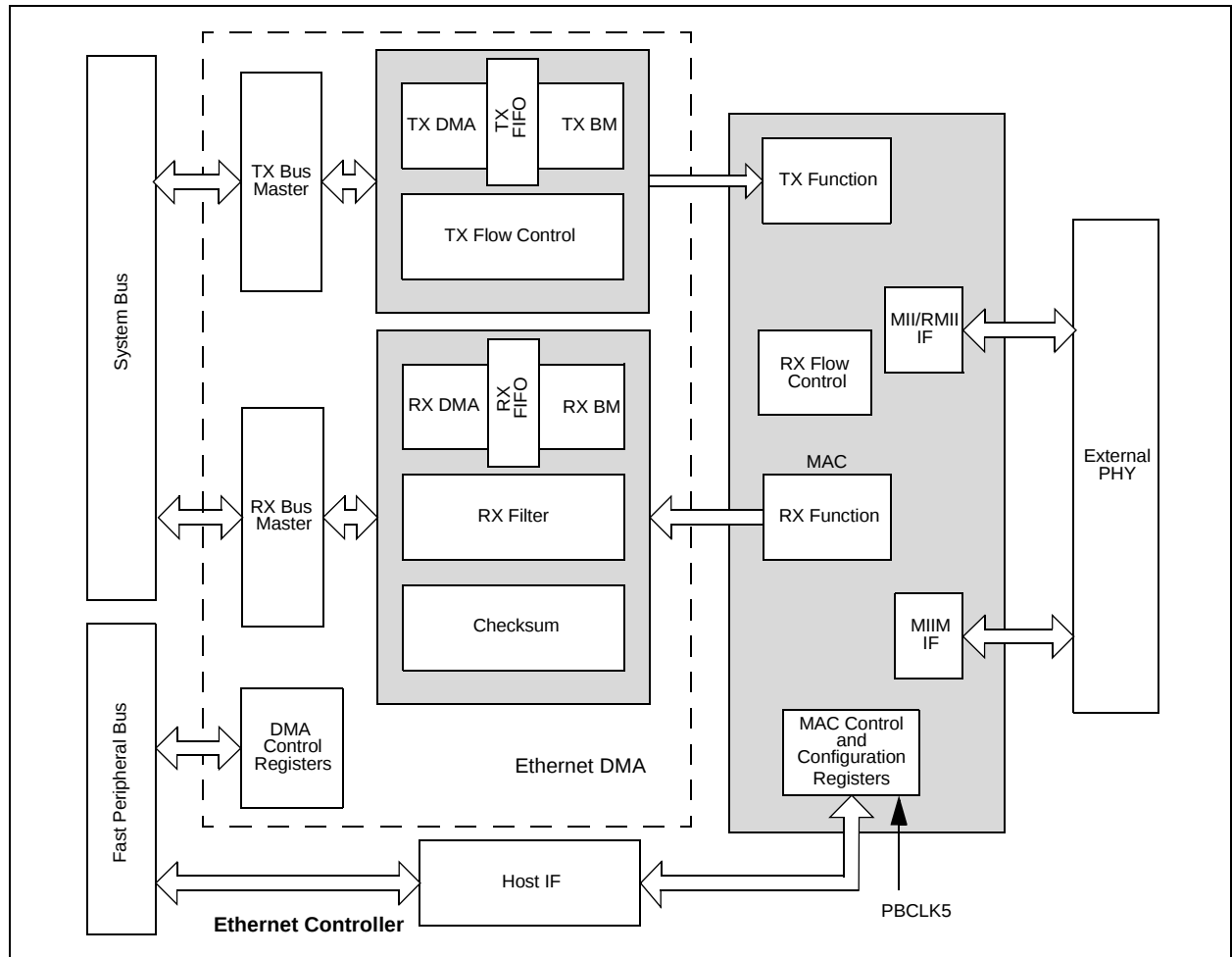
- Supports 10/100 Mbps data transfer rates
- Supports full-duplex and half-duplex operation
- Supports RMII and MII PHY interface
- Supports MIIM PHY management interface

- Supports both manual and automatic Flow Control
- RAM descriptor-based DMA operation for both receive and transmit path
- Fully configurable interrupts
- Configurable receive packet filtering
 - CRC check
 - 64-byte pattern match
 - Broadcast, multi-cast and uni-cast packets
 - Magic Packet™
 - 64-bit hash table
 - Runt packet
- Supports packet payload checksum calculation
- Supports various hardware statistics counters

Figure 30-1 illustrates a block diagram of the Ethernet controller.

Note: To avoid cache coherency problems on devices with L1 cache, Ethernet buffers must only be allocated or accessed from the KSEG1 segment.

FIGURE 30-1: ETHERNET CONTROLLER BLOCK DIAGRAM



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36.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

36.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

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TABLE 37-45: ETHERNET MODULE SPECIFICATIONS

AC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param. No.	Characteristic	Min.	Typ.	Max.	Units	Conditions
MIIM Timing Requirements						
ET1	MDC Duty Cycle	40	—	60	%	—
ET2	MDC Period	400	—	—	ns	—
ET3	MDIO Output Setup and Hold	10	—	10	ns	See Figure 37-24
ET4	MDIO Input Setup and Hold	0	—	300	ns	See Figure 37-25
MII Timing Requirements						
ET5	TX Clock Frequency	—	25	—	MHz	—
ET6	TX Clock Duty Cycle	35	—	65	%	—
ET7	ETXDx, ETEN, ETXERR Output Delay	0	—	25	ns	See Figure 37-26
ET8	RX Clock Frequency	—	25	—	MHz	—
ET9	RX Clock Duty Cycle	35	—	65	%	—
ET10	ERXDx, ERXDV, ERXERR Setup and Hold	10	—	30	ns	See Figure 37-27
RMII Timing Requirements						
ET11	Reference Clock Frequency	—	50	—	MHz	—
ET12	Reference Clock Duty Cycle	35	—	65	%	—
ET13	ETXDx, ETEN, Setup and Hold	2	—	16	ns	—
ET14	ERXDx, ERXDV, ERXERR Setup and Hold	2	—	16	ns	—

FIGURE 37-24: MDIO SOURCED BY THE PIC32 DEVICE

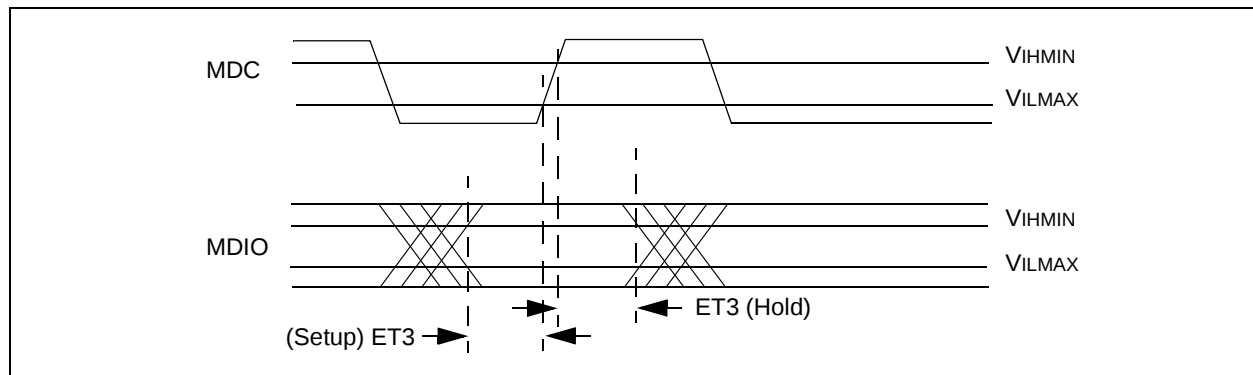
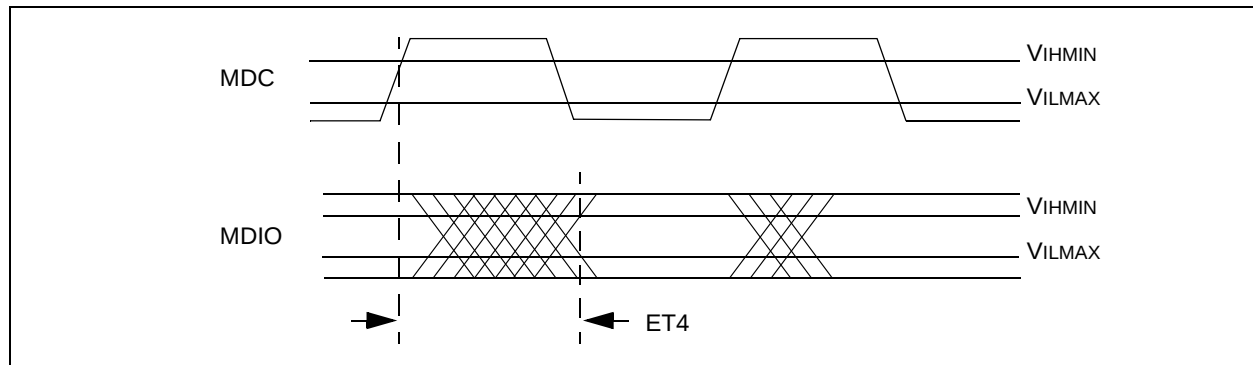


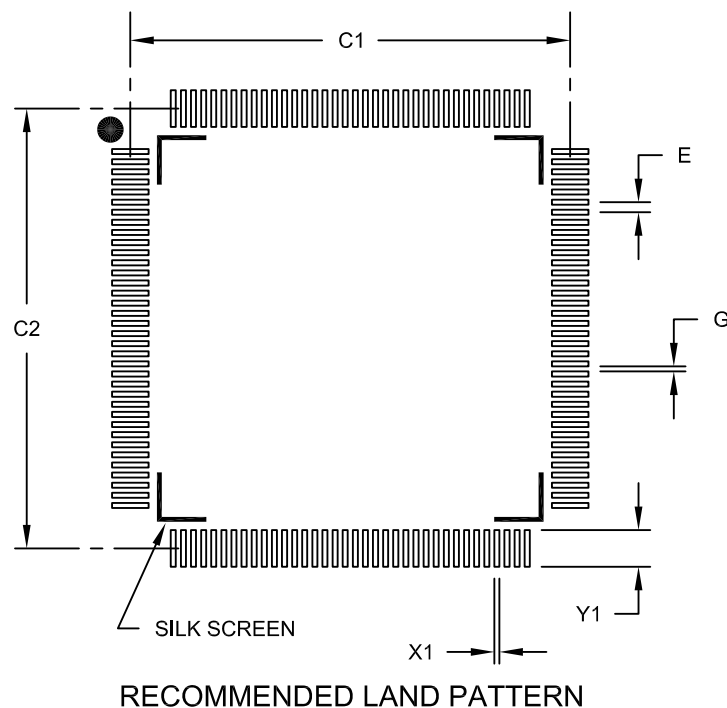
FIGURE 37-25: MDIO SOURCED BY THE PHY



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144-Lead Plastic Thin Quad Flat Pack (PH) - 16x16 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Contact Pad Spacing	C1		17.40	
Contact Pad Spacing	C2		17.40	
Contact Pad Width (X144)	X1			0.20
Contact Pad Length (X144)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2155B